Thermal-Based Millimeter-Wave Power Sensor Concept for Automotive Radar Applications

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Zusammenfassung

Die präzise Messung von absoluter Signalleistung im Frequenzbereich um 80 GHz erweist sich als sehr herausfordernde Aufgabe. Dies liegt in erster Linie daran, dass ein Messaufbau nicht ohne Fehlanpassung realisiert werden kann. Verstärkt wird dieses Problem noch dadurch, dass sich beim Verbinden der Millimeterwellenschaltung mit dem Messgerät je nach individueller Benutzung unterschiedliche Fehlanpassung einstellt. Selbst mit einem automatisierten Messaufbau lassen sich diese Effekte nicht eliminieren, wodurch sich eine schlechte Wiederholbarkeit ergibt. Speziell für Produkte, welche in hohem Volumen gefertigt und nach Automobilstandards getestet werden müssen, ist diese Unsicherheit ein Problem. Um die Testzeit und Komplexität für jeden einzelnen Baustein auf ein Minimum zu reduzieren werden stets neue Konzepte erarbeitet, bei welchen Signale bereits auf dem Baustein selbst getestet werden - mit Hilfe sogenannter Built-In Self-Test Schaltungen.

Gegenstand dieser Arbeit ist die Konzeptionierung, Entwicklung und Verifikation einer thermisch basierten Methode zur Leistungsmessung. Hierbei kommt ein über die Temperatur veränderlicher Widerstand (auch Thermistor genannt) zum Einsatz, welcher keine zusätzlichen Fertigungsschritte benötigt und somit problemlos in etablierte Fertigungsprozesse integriert werden kann. Potentielles Hauptanwendungsgebiet des Sensors werden Sende-Empfangsbausteine für Automobilradar-Anwendungen im Frequenzbereich um 80 GHz sein.

Eine detaillierte Beschreibung von vier verschiedenen Prototypen zeigt auf, welche Implementierungsmöglichkeiten es für den thermisch basierten Sensor in modernen Sende- und Empfangsbausteinen gibt. Die erzielten Ergebnisse sind vielversprechend und bieten die ideale Grundlage für eine Integration des Sensors in Produkte, welche in hohem Volumen gefertigt werden.

Abstract

The precise measurement of absolute signal power in the frequency range around 80 GHz is a challenging task. This is mainly caused by the measurement devices and the required connectors which do have relatively loose specifications resulting in limited accuracy. The variation of insertion loss when connecting the device under test to the measurement equipment, further contributes to the inaccuracy of the measurement. Even automated measurement setups cannot eliminate this effect, which results in a bad repeatability of the test. Especially for products which are manufactured in high volumes, and need to be tested according to automotive quality standards, this inaccuracy is problematic. This results in a need for new concepts of so called Built-In Self-Test circuitry, to reduce the test time and complexity of the devices.

It is part of this thesis to investigate, develop and verify a thermal-based method for on-chip power measurement. A temperature dependent resistor (also known as thermistor), which does not require any additional manufacturing steps is used for implementation. This allows straight forward integration in existing manufacturing processes. Potential field of use for the thermistor sensor will be transceiver devices for automotive radar applications in the frequency range around 80 GHz.

A detailed design description of four different prototypes shows the implementation possibilities for the thermal-based sensor in state of the art transceiver devices. The achieved results are promising and give the ideal basis for further integration of the sensor in products manufactured in high volume.

Publications and Patents

The following list shows the patents and publications which are authored or co-authored by Jonas Kammerer throughout the doctoral research time.

Please note that the author - Jonas Kammerer - got married while working on this thesis and decided to give up his maiden name which is Jonas Wursthorn. Depending on the date of publication either one of the names is mentioned in the list.

Patents

- J. Kammerer, H. Knapp and H. Li, *Power Sensor for Integrated Circuits*, U.S. Patent 10 466 339 B2, Nov 05, 2019

- J. Wursthorn, H. Knapp and H. Li, *Power Sensor for Integrated Circuits*, U.S. Patent 10 145 938 B2, Dec 04, 2018

- K. Dominizi, O. Frank, H. Jaeger, H. Knapp, F. Starzer, R. Stuhlberger and J. Wursthorn, *RF Front-End with Power Sensor Calibration*, U.S. Patent 10 128 962 B2, Nov 13, 2018

- H. Knapp and J. Wursthorn, *Millimeter-Wave Transmitter on a Chip, Method of Calibration thereof and Millimeter-wave Power Sensor on a Chip*, U.S. Patent 9 667 357 B2, May 30, 2017

Publications

- J. Wursthorn, H. Knapp, J. Al-Eryani, K. Aufinger, and L. Maurer. *Absolute mm-Wave Power Sensor Using a Switching Quad Output Stage.* In 2017 IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), Jan 2017.

- J. Wursthorn, H. Knapp, J. Al-Eryani, K. Aufinger, S. Majied, S. Boguth, H. Li, R. Lachner, and L. Maurer. *SiGe Power Amplifier for Automotive Radar Applications from 76 to 81 GHz.* In 2016 IEEE

MTT-S International Conference on Microwaves for Intelligent Mobility (ICMIM), May 2016.

- J. Wursthorn, H. Knapp, K. Aufinger, R. Lachner, J. Al-Eryani and L. Maurer. *A True-RMS Integrated Power Sensor for On-Chip Calibration.* In 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Sep 2014

- J. Al-Eryani, H. Knapp, J. Wursthorn, H. Li, K. Aufinger and L. Maurer. *Fully Integrated Single-Chip 305–375-GHz Transceiver With On-Chip Antennas in SiGe BiCMOS.* In 2018 IEEE Transactions of Terahertz Science and Technology, Vol. 8, Issue 3.

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Abbreviations

AC	Alternating Current. 6, 9, 10, 24, 33, 45, 46, 48, 49, 85
AMUX	Analog Multiplexer. 71, 74
ATE	Automatic Test Equipment. 79
Balun	Balanced-Unbalanced. 59, 80, 81, 85, 93, 95
BB	Baseband. 71
BiCMOS	Bipolar CMOS. 21–23, 28, 36
BIST	Built-In Self-Test. 1, 5, 21, 25
CML	Current Mode Logic. 28, 36, 58
CMOS	Complementary Metal-Oxide-Semiconductor. 21–23, 27, 28, 36, 54, 58, 105, 106
DC	Direct Current. 5, 6, 8–10, 13, 15, 17, 18, 20, 23, 40, 43–45, 48, 53, 59, 62–69, 71, 76, 77, 79, 80, 82, 85, 86, 88, 89, 91, 92, 95, 96, 98–100, 106, 107
DFT	Design For Test. 1
DMM	Digital Multi Meter. 62
DTI	Deep Trench Isolation. 31
DUT	Device Under Test. 18, 62, 64, 67, 71, 72, 74, 76, 81, 82, 84–87, 92, 93, 95–97, 99, 106
EBL	Epitaxial Base Link. 31, 32
EEB	Elevated Epitaxial Base. 31
EMC	Electromagnetic Compatibility. 5
EuroNCAP	European New Car Assessment Programme. 29
eWLB	embedded Wafer Level Ball Grid Array. 24, 32

FMCW Frequency Modulated Continuous Wave. 22

G1G Growth in One Go. 31
GaAs Gallium Arsenide. 21
GSG Ground-Signal-Ground. 15, 60, 62, 64, 85, 86, 95, 97
GSGSG Ground-Signal-Ground-Signal-Ground. 75, 77

HBT Heterojunction Bipolar Transistor. 10, 28–32, 34, 36, 54, 57, 84, 91
HS High Speed. 34, 36
HV High Voltage. 34, 36

IC Integrated Circuit. 5, 21, 23–25, 27, 33, 39, 40, 43, 52, 54, 55, 58–63, 66, 71–77, 80, 84, 86, 91, 93, 95, 105, 106
IGBT Insulated Gate Bipolar Transistor. 27
IL Insertion Loss. 53

JCAP Junction Capacitor. 33

KPI Key Performance Indicator. 101

LO Local Oscillator. 71

MIM Metal-Insulator-Metal. 33, 49, 75, 81
MMIC Monolithic Microwave Integrated Circuit. 1, 2, 18, 20, 22, 23, 58, 79
MS Medium Speed. 36

NIM National Institute of Metrology. 8
NIST National Institute of Standards and Technology. 8
NSEG Non-Selective Epitaxial Growth. 31
NTC Negative Temperature Coefficient. 17

P-Cell Parameterizable Cell. 33, 35
PA Power Amplifier. 34, 37, 53, 55, 58, 59, 62, 64, 69, 73, 75, 77, 86, 88, 95, 99
PAE Power Added Efficiency. 82
PCB Printed Circuit Board. 23, 24, 71
PDK Process Design Kit. 33, 40
PLL Phase Locked Loop. 58, 74
PTC Positive Temperature Coefficient. 17

RDL Redistribution Layer. 24
RF Radio Frequency. 8–10, 12, 13, 16–18, 20–25, 31–34, 36, 39, 40, 45, 48, 49, 51–55, 57–60, 62, 64–69, 71, 73, 75, 77, 79–82, 84–86, 88, 89, 91–100, 106, 107
RMS Root Mean Square. 7, 12, 22, 47
RX Receiver. 23, 71

SEG Selective Epitaxial Growth. 31
SIC Selectively Implanted Collector. 31
SiGe Silicon Germanium. 28–32, 34, 36
SPDT Single Pole Double Throw. 81, 82, 84, 85, 87–89, 91, 93, 101–103, 106
SPI Serial Peripheral Interface. 58, 60, 62, 77
STI Shallow Trench Isolation. 30
SWR Standing Wave Ratio. 62

TaN Tantalum Nitride. 33, 34, 49, 59
TC Temperature Coefficient. 17, 18, 41, 42, 105
TX Transmitter. 23, 24, 39, 51–54, 57, 58, 64, 66, 71

UHS Ultra High Speed. 34, 35

VCO Voltage Controlled Oscillator. 28, 29, 33, 34, 36, 37, 51, 58, 60, 62, 71, 74, 77

Symbols

A_0	A_0 Cell Gain		13–16, 22
BV_{CB}	Collector-Base Breakdown Voltage	V	34–36
BV_{CE}	Collector-Emitter Breakdown Voltage	V	34–36
C_{BCi}	Inner Base-Collector Capacitance	F	30
C_{BCo}	Outer Base-Collector Capacitance	F	30
C_{BC}	Base-Collector Capacitance	F	28
C_{BEi}	Inner Base-Emitter Capacitance	F	29
C_{BEo}	Outer Base-Emitter Capacitance	F	29
C_{RF}	RF Bypass Capacitance	F	9
C_{off}	Off-State Capacitance	F	81
C_{th}	Thermal Capacitance	Ω	40, 43–46, 105
E	Electric Field	$\mathrm{V} \cdot \mathrm{m}^{-1}$	20
I_{DC}	DC Current	A	6
I_{Q}	Heat Transfer	W	43, 44
I_{S}	Saturation Current	A	9, 10
I_{p}	Peak Current Value	A	7
I_{rms}	Root Mean Square Current Value	A	7
I	Current	A	43, 44
J_{C}	Collector Current Density	$\mathrm{A} \cdot \mu\mathrm{m}^{-2}$	28
M	Line Gradient		13
N	X-Axis Intersection Point		13, 15
P_{DC}	DC Power	W	6
P_{d}	Dissipated Power	W	43
P_{in}	Input Power	W	9
P_{out}	Output Power	W	39
P	Real Power	W	5–7, 16, 47
Q	Reactive Power	VAR	5, 6
R_{Bi}	Inner Base Resistance	Ω	30
R_{Blink}	Baselink Resistance	Ω	30, 31
R_{Bo}	Outer Base Resistance	Ω	30
R_{B}	Base Resistance	Ω	28

R_{C}	Collector Resistance	Ω	30
R_{E}	Emitter Resistance	Ω	30
R_{M}	Matching Resistance	Ω	9
R_{on}	On-State Resistance	Ω	81
$R_{\mathrm{sh,silB11}}$	Rsil Sheet Resistance in B11HFC	$\Omega \cdot \square^{-1}$	42
$R_{\mathrm{sh,silB7}}$	Rsil Sheet Resistance in B7HF200	$\Omega \cdot \square^{-1}$	42
R_{th}	Thermal Resistance	Ω	40, 43–47, 105
R	Resistance	Ω	6, 41, 43, 44, 47
S	Apparent Power	W	5, 6
$TC_{1,\mathrm{silB11}}$	Rsil First Order TC in B11HFC	K^{-1}	42
$TC_{1,\mathrm{silB7}}$	Rsil First Order TC in B7HF200	K^{-1}	42
TC_1	First Order Temp. Coefficient	K^{-1}	35, 36, 41, 42, 44, 47
T_{P}	Time Period	s	6, 7, 10
T	Absolute Temperature	K	9, 10, 44
V_{CC}	Supply Voltage	V	10, 60
V_{DC}	DC voltage	V	6
V_{T}	Temperature Voltage	V	10, 11
V_{det}	Detected Voltage Level	V	9–15, 39
V_{p}	Peak Voltage Value	V	7, 10, 11
V_{ref}	Reference Voltage	V	15
V_{rms}	Root Mean Square Voltage Value	V	7
V	Voltage	V	43
Z_{L}	Characteristic Line Impedance	Ω	8, 33, 59
Z	Characteristic Impedance	Ω	9
ΔT	Temperature Difference	K	41, 43, 44
$\bar{P}$	Average Power	W	6
$\bar{i_{\mathrm{D}}}$	Average Diode Current	A	10
ρ	Density	$\mathrm{g} \cdot \mathrm{m}^{-1}$	46
τ_{GD}	Transistor Gate Delay	s	28, 29, 35
τ_{th}	Thermal Time Constant	s	46, 47
θ_{iv}	Phase Shift between i(t) and v(t)	$^\circ$	7
c	Specific Heat	$\mathrm{J} \cdot \mathrm{kg}^{-1} \cdot \mathrm{K}^{-1}$	46
d_1	Divider Ratio 1st Stage		58
d_2	Divider Ratio 2nd Stage		58
f_0	Fundamental Frequency	Hz	58, 74
f_{T}	Maximum Transit Frequency	Hz	28, 29, 31, 35–37
f_{max}	Maximum Oscillation Frequency	Hz	28, 29, 35–37

h	Height	m	46
$i(t)$	Instantaneous Current	A	6–8
i_{D}	Diode Current	A	9
k	Boltzmann Constant	$\mathrm{J} \cdot \mathrm{K}^{-1}$	9, 10
l	Length	m	46
$p(t)$	Instantaneous Power	W	6, 8
q	Electron Charge	C	9, 10
$v(t)$	Instantaneous Voltage	V	6–8
v_{D}	Diode Voltage	V	9, 10
v_{rf}	RF Signal Voltage	V	9, 10, 12, 13, 17, 18
v	Volume	m	46
w	Width	m	46

Chapter 1

Introduction

Recent developments show a growing market for integrated circuits using millimeter wave signals. The strong drivers behind this trend are spectroscopy, imaging, communications, and radar applications. Especially the last two segments potentially offer a high-volume market. The communication applications are pushed by the consumer market including the upcoming fifth generation of mobile communications. The driver behind the radar application is the automotive sector where the trend goes towards driver assistance systems and autonomous driving.

The fact that autonomous emergency breaking systems are included in the *European New Car Assessment Programme* rating since 2014 [Ratingen 16] forces car manufacturers to use radar systems not only in their upper class vehicles, but also in the broad medium class segment. Semiconductor suppliers like Infineon Technologies AG deliver Monolithic Microwave Integrated Circuits (MMICs) containing whole transceivers for such applications in silicon-based technologies.

In order to fulfill automotive quality standards with the automotive radar circuits, it is required to test the functionality of every single device before delivery. This leads to a massive increase in test effort and accordingly test time. For automotive radar integrated circuits the test time is a limiting factor and contributes up to 30 % to the overall price of the device.

To keep the product price for automotive radar ICs at a competitive level, it is beneficial to think about testability already in the design phase, and implement as many Design For Test (DFT) features as possible. The design of such features at 80 GHz is challenging and requires additional design effort. However, if Built-In Self-Test (BIST) features work as expected they can bring advantages compared to competitors solutions.

One critical parameter during production test is the output power of the transmit signal. A minimum level needs to be checked, in order to fulfill

the specification towards the customer and reach the signal to noise ratio for targets which are far away. Additionally, a maximum power level shall not be exceeded due to legal constraints. The setup for an output power measurement at the operating frequency however, is fragile and time consuming. Measurement setups for millimeter waves in general are complex and require detailed know-how which is undesirable for automated test environments. Furthermore, the measurement devices and connectors are expensive compared to DC or low frequency equipment.

To circumvent the power measurement at the operating frequency, it is required to implement a reliable on-chip power detector. Usually, these detectors are affected by process variation and therefore require a certain margin to make sure the MMIC fulfills the specification. A higher margin usually results in less yield and accordingly higher effective manufacturing costs. A calibration of the power detector for every individual IC however will reduce the required margin and minimize process variation.

The subject of this work is to investigate the possibilities for accurate on-chip measurement of absolute signal power around 80 GHz. In this context, mainly a thermal-based sensor is investigated in detail. The developed thermistor power sensor relies on its DC power substitution principle which allows straight forward integration in automated test routines.

First, the basics of power measurements are explained and highlighted with examples. Furthermore, the different methods of millimeter wave power measurements are described. It turns out that a thermal-based solution shows the highest potential for on-chip implementation as it has low dependency on process variation.

Afterwards, a closer look on the recent development of high speed silicon germanium transistors is given. The properties and limitations thereof are explained in detail. Furthermore, it is described how the two used technologies of Infineon Technologies AG look like and how they differ. Cross sections of transistors and metal stacks are used to highlight the details.

Next, the state of the art in on-chip power detection circuitry and the problems thereof are shown. First measurement results of the resistor layers proof that it is possible to realize a thermistor with sufficient sensitivity in the available technologies. In addition, it is explained what is necessary to extend the existing resistor model by a thermal domain to represent self-heating accurately for simulation purposes.

After that, the possibilities to integrate the sensor in a multi channel transmitter are highlighted. It is explained how the overall accuracy of the on-chip power measurement is increased by the thermistor calibration. Furthermore, it is shown why the proposed calibration does not require an external measurement at the operating frequency of around 80 GHz any more.

Finally, the devices which are developed for testing the thermistor concept are analyzed. In this context a detailed view on the circuit design and layout is given, as well as on the measurements for verification and the according setups. The advantages and challenges of the particular devices are discussed and rated. The thesis is closed with a conclusion which contains the most relevant results and achievements.

Within this work, it is shown how the thermistor power sensor can be implemented and used in a product-like environment. Several prototypes are designed, layouted and measured to verify the working principle of the sensor. For an output power level above 0 dBm an error of less than ± 0.6 dB is achieved. For the most promising calibration approaches patents have been filed and granted.

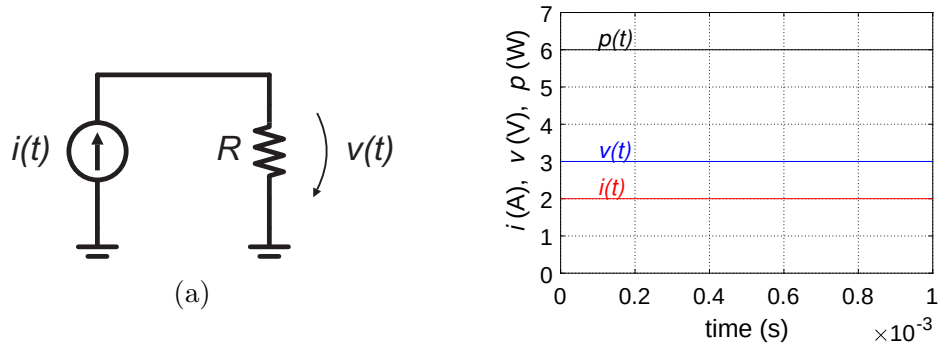
Chapter 2

Power Detection of Millimeter Wave Signals

Accurate power measurements of millimeter wave signals are important for several reasons. One aspect is that there are regulations on the maximum allowed power radiation of wireless signals which are given by law. If a new product enters the market it needs to stick to the limitations in the operating frequency range as well as all the other defined frequencies to meet the Electromagnetic Compatibility (EMC) requirements. Usually, this is verified in absorption chambers for a few reference samples of a product. The measurement setup is highly accurate and requires complex mechanical installation to generate antenna diagrams.

Another important topic for millimeter wave power measurement has its origin in automotive quality standards. To meet these standards it is required to ensure the functionality of every delivered Integrated Circuit (IC). In order to keep the price at a competitive level it is desirable to have BIST structures on the IC to reduce the testing time of each die. Depending on the application these structures can be reused as monitoring features during operation detecting degradation errors or faulty behavior reliably. Obviously, the requirements on on-chip power sensors differ from the requirements on power measurements in a laboratory environment. Nevertheless, the operating principles of the sensor can have a lot in common. In the later sections the principles of electrical based and thermal based approaches will be explained in more detail but first of all there is a short summary on the definition of power and the limitations of commonly used power sensors for Direct Current (DC) and low frequencies.

The apparent electrical power S consists of two power components namely the real power P which is transferred into work or heat and the reactive power Q which is stored energy in the system. The mathematical relation between



(a) (b)

Figure 2.1: DC power measurement setup (a) and current, voltage, power behavior vs. time (b).

these forms of power is shown in Equation 2.1.

$$S^2 = P^2 + Q^2 \tag{2.1}$$

For power measurements usually the real power P is most interesting as it defines how long a battery will last or how much a consuming device heats up during operation.

The instantaneous power $p(t)$ at a specific time is calculated from the product of the instantaneous current $i(t)$ and voltage $v(t)$. As the instantaneous power varies over time for alternating signals a more practical approach is to sum up $p(t)$ and average over a time period T_P. This is expressed in Equation 2.2.

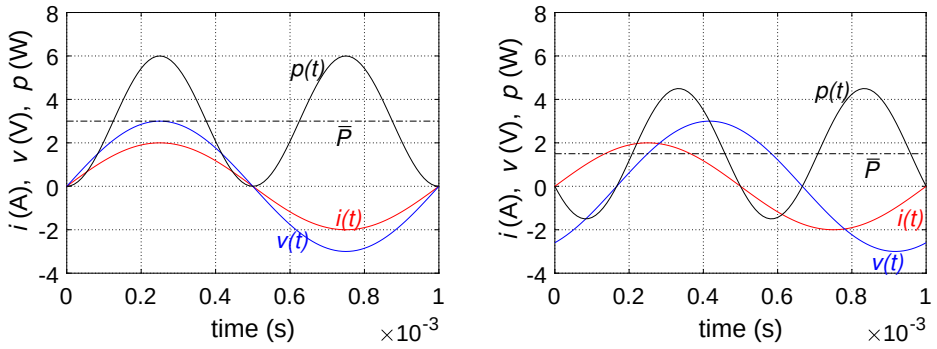
$$\bar{P} = \frac{1}{T_\mathrm{P}} \int_0^{T_\mathrm{P}} i(t)v(t)dt \tag{2.2}$$

For DC signals the current $i(t)$ and the voltage $v(t)$ are constant within T_P. The formula to calculate the dissipated DC power P_DC then simplifies to

$$P_\mathrm{DC} = V_\mathrm{DC} I_\mathrm{DC} \tag{2.3}$$

For a resistive load R the formula can be adapted accordingly using Ohm's Law. The setup for a typical DC power measurement on a resistor R is shown in Figure 2.1a. Figure 2.1b shows $i(t)$, $v(t)$ and $p(t)$ over time.

For the average power of sinusoidal continuous wave Alternating Current (AC) signals it is sufficient to investigate one complete cycle. $i(t)$ and $v(t)$ are replaced by the following expressions assuming no phase shift between



(a) $\theta_{\mathrm{iv}} = 0°$ (b) $\theta_{\mathrm{iv}} = 60°$

Figure 2.2: Instantaneous current, voltage and power behavior vs. time.

current and voltage at a purely resistive load.

$$i(t) = I_{\mathrm{p}} \sin(\omega t)$$

$$v(t) = V_{\mathrm{p}} \sin(\omega t)$$

Here I_{p} and V_{p} are the peak current and voltage of the sinusoidal signals. Assuming these values are constant Equation 2.2 can be rewritten as follows:

$$P = \frac{I_{\mathrm{p}} V_{\mathrm{p}}}{T_{\mathrm{P}}} \int_0^{T_{\mathrm{P}}} \sin^2(\omega t) dt \tag{2.4}$$

Solving the integral using $\int_0^x \sin^2 x dx = \frac{x}{2} - \frac{\sin x \cos x}{2}$ leads to the following result:

$$P = \frac{I_{\mathrm{p}} V_{\mathrm{p}}}{2} = \frac{I_{\mathrm{p}}}{\sqrt{2}} \frac{V_{\mathrm{p}}}{\sqrt{2}} = I_{\mathrm{rms}} V_{\mathrm{rms}} \tag{2.5}$$

In Equation 2.5 I_{rms} and V_{rms} represent the Root Mean Square (RMS) values of the sinusoidal signals. The average power and instantaneous power, current and voltage for one cycle are shown in Figure 2.2a. Note that the resulting power signal is always positive and oscillates with twice the frequency of current and voltage.

If the power is dissipated in a load which is not purely resistive, but also shows a reactive behavior, then there will be a phase shift θ_{iv} between current and voltage. If $\theta_{\mathrm{iv}} \neq 0$ the average real power will be reduced compared to the purely resistive load. This is shown in Equation 2.6.

$$P = I_{\mathrm{rms}} V_{\mathrm{rms}} \cos(\theta_{\mathrm{iv}}) \tag{2.6}$$

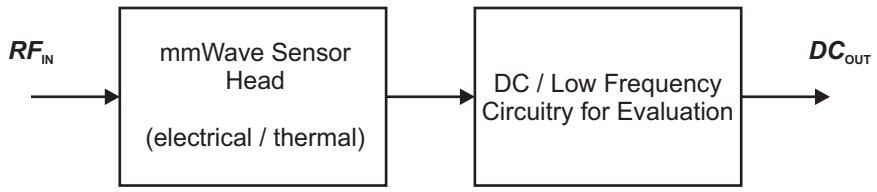


Figure 2.3: Working principle of millimeter wave power detectors.

Figure 2.2b shows $i(t)$, $v(t)$ and $p(t)$ over one time period. In addition, the average power is shown. Note that $p(t)$ can even get negative for a passive network. During this time the energy is stored in the circuit. This energy is not converted to work.

Looking at millimeter wave signals, the detection of instantaneous current $i(t)$ and voltage $v(t)$ for power calculation is difficult. Therefore, it is more common to measure the voltage at a defined load impedance. State of the art oscilloscopes offer active $50\,\Omega$ probes for transient voltage detection. Nevertheless, it is not possible to detect signals above 100 GHz. Furthermore, these oscilloscopes are expensive and complex systems.

Transmission line theory brings up another topic why conventional voltage detection is not useful at millimeter wave signals. It teaches that the voltage along a transmission line which is not terminated by Z_L varies between a minimum and a maximum value because of standing waves. Depending on the voltage probe location along the transmission line, the power could be anywhere between its minimum and its maximum.

Finally, it is more convenient to detect the power directly instead of measuring current and voltage. To perform these power measurements, there are different methods available, which can roughly be separated into electrical based and thermal based measurements. The common goal of all of these sensors is to detect a millimeter wave signal and transform it into a DC or low frequency signal which is proportional to the Radio Frequency (RF) power which is applied to the detector (see Figure 2.3). No matter if electrical or thermal based sensor principles are used, they have to be calibrated on a regular basis. The calibration standards which vendors use to verify the accuracy of the sensor are derived from a microcalorimeter standard at the National Institute of Standards and Technology (NIST) [Weidman 81]. The NIST offers certified calibrations up to the WR10 waveguide band (75 GHz to 110 GHz). The National Institute of Metrology (NIM) of China lately also published developments on this topic [Cui 16].

The following sections deal with the commonly used sensor concepts in detail and explain the working principal.

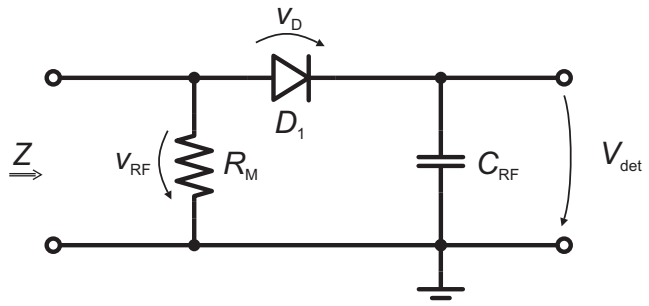


Figure 2.4: Simplified Diode Detector Circuit. Drawing based on [Wetenkamp 83].

2.1 Electrical Based Sensors

Electrical based power sensors evaluate an electrical signal like current or voltage to measure the RF power. A basic requirement to the detecting element is the conversion of the RF input signal to a low frequency or DC output which is proportional to the power of the input signal P_{in}. If the power sensor is matched to the impedance of the system Z the voltage can be substituted by a power level in dBm.

2.1.1 Diode Power Detector

Diode based power detectors use the non-linear current-voltage characteristic of a diode for rectification. This results in a transformation of an RF input signal v_{rf} to a DC output voltage level V_{det}. Figure 2.4 shows a simplified schematic of a diode based power detector. The matching resistance R_{M} is used to create a proper matching to the system impedance Z and generate a defined voltage drop v_{rf} at the input of the detector. Furthermore, it is used to set the bias level for the diode. The voltage drop across the diode v_{D} and the resulting diode current i_{D} are rectified and result in an increased DC output voltage across the bypass capacitor C_{RF}.

The diode current i_{D} at any time can be calculated as

$$i_{\text{D}} = I_{\text{S}} \left(\mathrm{e}^{\frac{v_{\text{D}} q}{kT}} - 1 \right) \tag{2.7}$$

where i_{D} is the diode current, I_{S} is the reverse saturation current, v_{D} is the voltage across the diode, q is the charge of an electron, k is the Boltzmann constant and T the absolute temperature.

The following derivations are based on the work of [Wetenkamp 83]. Assuming that the ideal bypass capacitor C_{RF} suppresses any AC signal from

the output, the integration over one time period results in the average diode current $\bar{i_{\mathrm{D}}}$.

$$\bar{i_{\mathrm{D}}} = I_{\mathrm{S}} \frac{1}{T_{\mathrm{P}}} \int_0^{T_{\mathrm{P}}} \left(\mathrm{e}^{\frac{v_{\mathrm{D}} q}{kT}} - 1 \right) dt \tag{2.8}$$

The diode voltage v_{D} can be calculated from V_{det} and $v_{\mathrm{rf}} = V_{\mathrm{p}} \cos(\omega t)$ where V_{p} is the voltage peak value of the RF signal. Assuming that the detector output is connected to circuitry with a high impedance the average diode current is 0. This leads to a detector voltage which can be written as follows.

$$V_{\mathrm{det}} = \frac{kT}{q} \ln \left[B_0 \left(\frac{qV_{\mathrm{p}}}{kT} \right) \right] \tag{2.9}$$

In this equation B_0 is a Bessel function of the first order.

Based on Equation 2.9 the limit values of the formula can be analyzed. For small amplitudes at the input the following equation can be found

$$V_{\mathrm{det}} \sim \frac{V_{\mathrm{p}}^2}{4V_{\mathrm{T}}} \tag{2.10}$$

where $V_{\mathrm{T}} = kT/q$. It can be observed that the detector output is proportional to the square of the peak input voltage. The same behavior is valid for the power and therefore V_{det} is a measure of the real power level.

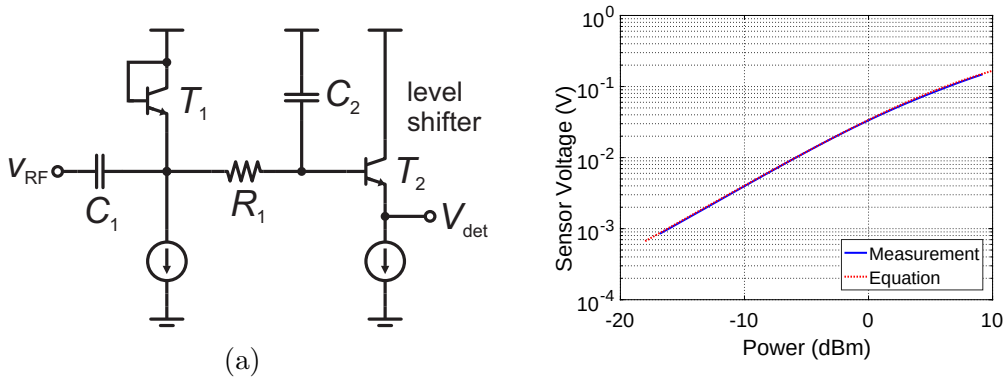
For large signals, Equation 2.9 can be simplified to the following equation.

$$V_{\mathrm{det}} \sim V_{\mathrm{p}} - \frac{V_{\mathrm{T}}}{2} \ln \left[\frac{2\pi V_{\mathrm{p}}}{V_{\mathrm{T}}} \right] \tag{2.11}$$

In this region the detector output voltage is almost proportional to V_{p}. The detector therefore operates in peak detection mode. For medium input signals the output characteristic is in a transition region between the two extremes.

Figure 2.5a shows a simplified schematic of a power detector which can for example be implemented in Infineons' in-house technologies (see Chapter 3). The circuitry is referred to the supply domain V_{CC} to reduce the parasitic capacitance at the RF node as the emitter of the Heterojunction Bipolar Transistor (HBT) (T_1) is connected to it instead of the collector. Transistor T_1 is current biased by I_1 and connected in diode configuration to rectify the input signal v_{rf}. R_1 and C_2 act as a low-pass filter and provide a DC signal to the succeeding level shifter transistor T_2 which is biased by I_2. C_1 is required to split the DC biasing from the AC path.

The measured output characteristic of the power detector is shown in Figure 2.5b (blue). A square-law behavior for small input signals and a peak detection behavior for large signals can be observed. The red line represents



(a) (b)

Figure 2.5: Example of a diode detector schematic (a) and the according characteristic over input power (b)

the results from Equation 2.9 including some modifications to meet the absolute measured values. Both traces show good agreement which verifies that the derived formula including simplifications from [Wetenkamp 83] suit well for the output characteristic of diode based power sensors.

2.1.2 Transistor Power Detector

The transistor power detector developed by Robert G. Meyer (also known as Meyer detector) is originally published as a peak voltage detector [Meyer 95]. Hence, the equation derived for the large signal operating mode is identical to the one of the diode detector (see Equation 2.11).

$$V_{\mathrm{det}} \sim V_{\mathrm{p}} - \frac{V_{\mathrm{T}}}{2} \ln\left[\frac{2\pi V_{\mathrm{p}}}{V_{\mathrm{T}}}\right] \tag{2.12}$$

As already observed for the diode detector, the Meyer detector output voltage directly depends on V_{p}. The influence of the additional error term is reduced for higher input signal levels due to the ln function. Note that V_{det} also depends on the absolute temperature.

Also for small input signals the Meyer detector shows a square-law behavior similar to the diode power detector. Root cause for this is that the transistor detector is also based on the non-linear characteristic between voltage and current. A formula for the small signal behavior of the Meyer detector is derived in [Zhang 04].

$$V_{\mathrm{det}} \sim \frac{V_{\mathrm{p}}^2}{4V_{\mathrm{T}}} \tag{2.13}$$

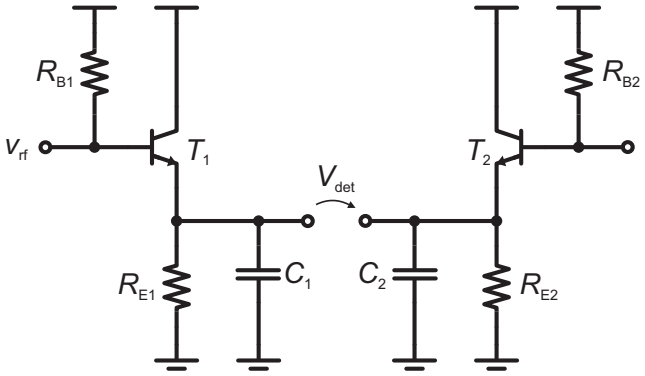


Figure 2.6: Schematic of the Meyer detector. Drawing based on [Meyer 95].

Equation 2.13 shows that the detector output is proportional to the square of the input voltage. This indicates RMS power detection. The sensor itself is also temperature dependent for small input voltages.

Figure 2.6 shows the schematic of a Meyer detector. Transistor T_1 acts as the rectifying element for the RF signal v_{rf}. Transistor T_2 is used as a reference element. It is identical in size and orientation to T_1 thus leading to a detector output voltage V_{det} of zero if no input signal is applied. The resistors R_{Bx} and R_{Ex} are biasing the transistors and furthermore can be used for input matching purposes. Capacitor C_1 filters the the rectified signal. It is designed that the ripple on the output node is minimized within one cycle of v_{rf} but still allows a reasonable settling time of the detector output voltage V_{det}.

One drawback of the original Meyer detector is the rather large transition region between the square-law and the linear behavior of $\sim 30\,\mathrm{mV}$ to $100\,\mathrm{mV}$ [Zhang 04]. In this region it is difficult to predict the detector behavior by simplified equations like 2.12 and 2.13. The fact that the transition region usually covers the operating region of the detector makes it even worse. It is shown that the transition region on the traditional Meyer detector can be reduced by feeding a small portion of the input signal to the base of the reference transistor to increase the linear detection region [Zhang 04].

Another disadvantage is the limited range in which the original Meyer detector can be operated as an RMS detector. In [Zhang 06] a modification of the detector is presented which overcomes this issue. Several resistive attenuator stages are used to increase the RMS range. Therefore the loss in each attenuator has to be known precisely to re-calculate the power level at the input.

2.1.3 Logarithmic Amplifier

Logarithmic amplifiers can be used for a wide range of on-chip signal preprocessing. Especially in applications where a high dynamic range has to be covered the logarithmic amplifier benefits from its logarithmic compression of the applied input signal. The two types of logarithmic amplifiers are called true type and demodulating type.

The true type logarithmic amplifier compresses the amplitude of the input signal while preserving the phase and frequency information which can be evaluated by succeeding stages. The demodulating type provides a low-frequency or DC output signal which is proportional to the input signal in decibel [Analog Devic 99]. As this behavior is often the desired one for a level detector the demodulating type is the preferred architecture for further discussion.

The dashed black line in Figure 2.7 represents an ideal logarithmic curve which appears as a straight line in a semi-logarithmic plot. It illustrates the linear relation between an input signal (logarithmic) and the output voltage V_{det}(linear). The behavior can be described using the following formula

$$V_{\mathrm{det}} = M \log \left[\frac{|v_{\mathrm{rf}}|}{N} \right] \tag{2.14}$$

where M represents the gradient, N is the intersection point with the x-axis and v_{rf} is the RF input signal.

The goal of the logarithmic amplifier is to approximate the ideal characteristic in piecewise steps as good as possible. Therefore, identical gain stages are cascaded as shown in the block diagram in Figure 2.8. The gain stages are identical cells with a defined small signal gain of A_0. If the input voltage at a stage reaches a certain value the output voltage of this stage is limited as indicated on the left side in Figure 2.8. Depending on the amplitude of the input signal the number of stages which are driven into limitation varies.

For small signals all stages are operated in their small signal region. Increasing the input signal leads to limitation in the stages starting from the right (stage N). The node voltages between the A_0 cells are being rectified (indicated by the diode symbols in Figure 2.8) and summed up to the detector output voltage V_{det}. To further extend the upper end of the dynamic range additional stages including attenuators can be used [Analog Devic 99]. The solid red line in Figure 2.7 represents the behavior of a multiple stage logarithmic amplifier. For small input signals left of Ⓐ none of the N stages reaches the gain limit. At point Ⓐ the last stage reached its limit and does not contribute any gain when increasing the input signal amplitude. Further increasing v_{rf} will progressively lead to a similar behavior in the preceding

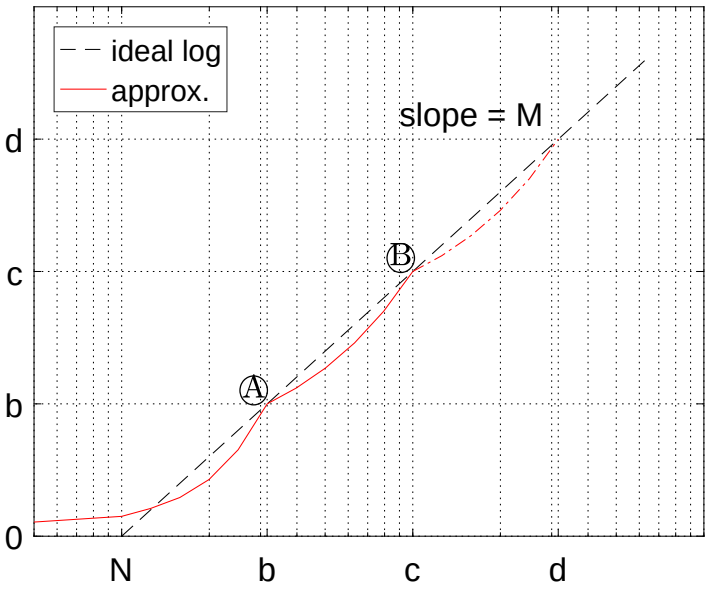


Figure 2.7: Behavior of the Logarithmic Amplifier. Drawing based on [Analog Devic 99].

stages (point Ⓑ and so on). It is observed that the deviation between the two lines in Figure 2.7 reaches a minimum just when another stage starts to limit. In between there is a systematical error which is called the logarithmic error [Analog Devic 99]. The number of used stages is adjusted according to the requirements of the application.

The performance of a logarithmic amplifier in the frequency range around 80 GHz in Infineons' B11HFC technology is investigated and a test circuit has been designed in [Hammerl 12]. It consists of five A_0 stages each having a gain of 5 dB resulting in a dynamic range of 25 dB. Each A_0 cell consists of a differential common emitter stage with a resonant load in the target frequency range. Furthermore, the stage is current biased and employs neutralization capacitors for increased bandwidth.

For rectification of the signals between the stages the succeeding differential pair can be used. The common emitter node automatically carries the rectified signal of the previous output. An additional stage is added after the stage N for rectification of the last node. This also ensures similar loads to all relevant stages. A summing amplifier is used to generate the final output signal V_{det}.

Figure 2.9 shows a micro photograph of the logarithmic amplifier which is described in [Hammerl 12]. The input signal is fed from the left through

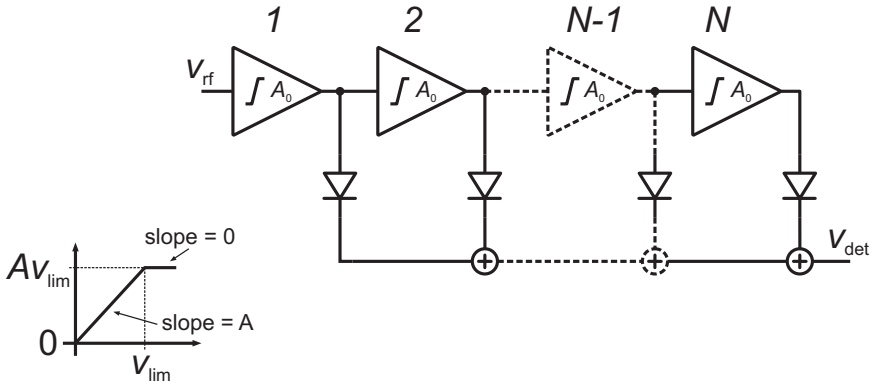


Figure 2.8: Block diagram of the Logarithmic Amplifier. Drawing based on [Analog Devic 99].

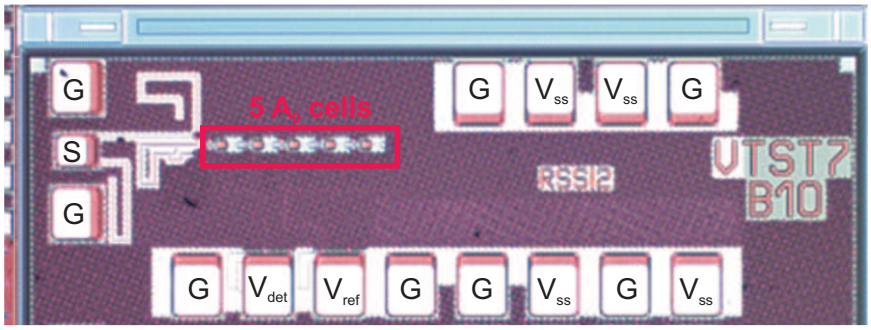


Figure 2.9: Micro photograph of the logarithmic amplifier in B11HFC.

the Ground-Signal-Ground (GSG) pad structure with the small signal pad in the middle. The transmission lines after the pads are used for impedance matching. The five identical A_0 cells including the resonance inductance are lined up further to the right. The two marked pads in the bottom row are used to measure the detector output voltage V_{det} compared to an on-chip reference voltage level V_{ref}. The additional pads are for (redundant) DC supply.

The measurement results of the logarithmic amplifier are shown in Figure 2.10. As mentioned above, output voltage is measured as the difference between the detector voltage V_{det} and the voltage reference V_{ref}. For small input signal levels the offset between the reference and the signal output has been eliminated resulting in all curves starting from 0 V.

The expected linear dynamic range of the amplifier can be calculated from the number of stages N and the gain in A_0 in decibel.

$$DynamicRange = NA_0 = 25\,\mathrm{dB} \tag{2.15}$$

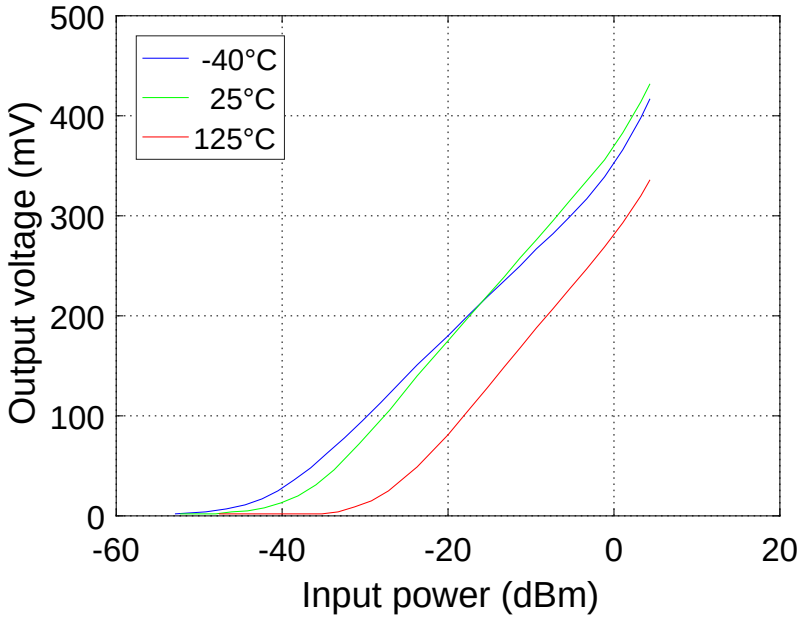


Figure 2.10: Measurement results of the logarithmic amplifier in B11HFC.

The expectation agrees well with the observed results as the curve shows a linear relation between the logarithmic input signal and the linear output signal across more than 25 dB. In this range the voltage detector responds with approximately 100 mV/decade. The dynamic range can be extended by using additional A_0 cells.

Furthermore, it is observed that the output signal as well as the slope of the curve are depending on temperature. This effect is mainly caused by the gain variation of each stage over temperature.

2.2 Thermal Based Sensors

The detection of electrical signals (voltage and current) to calculate the power level becomes increasingly difficult at higher frequencies. To circumvent this difficulty thermal based sensors are employed to measure the power directly. Often, voltage and current measurements at mm-wave frequencies are even derived from the thermal based power measurement [Mäusl 74].

The thermal based power measurement concept relies on the conversion of electrical power into heat. As only real power P contributes to the heat conversion, a thermal based power sensor is per se a good candidate for RF power measurements of any kind of waveform.

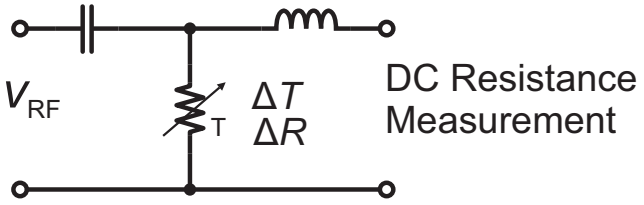


Figure 2.11: Simplified thermistor setup.

For power detection, the RF signal is fed to an absorber which heats up accordingly. The change in temperature then results in a change of the physical property of the sensor element, which can for example be a resistor with a temperature coefficient. The change of the electrical parameter is evaluated by additional circuitry like measurement bridges. An advantage of conventional thermal based power measurements is the DC substitution capability.

Thermal based power sensors can be split in three general groups named thermistors, calorimeters and thermocouples. The functionality and operating principles of these groups are explained in the following sections in more detail.

2.2.1 Thermistor

The thermistor provides the simplest solution amongst the thermal based power sensors. It is basically a resistor with a significant temperature dependency as the name already indicates. The most popular materials for thermistors are thin metallic wires (also referred to as barretter [Keysight Tec 14]) and semiconductors.

Figure 2.11 shows a simplified thermistor power sensor setup. The RF signal v_{rf} is applied to the resistor which converts the electric power to heat. Due to the Temperature Coefficient (TC) the resistance either increases (Positive Temperature Coefficient (PTC)) or decreases (Negative Temperature Coefficient (NTC)) with applied power. This means that the thermistor acts as the absorber and the sensing element at the same time. The change in resistance is detected and gives a measure of the applied RF power. The coupling capacitor and inductor indicate, that there is further circuitry required to isolate the RF signal path from the DC measurement path.

If the thermistor is the termination for an RF circuit, it is required that the resistance matches the system impedance to minimize reflections and absorb as much power as possible. In this application the DC substitution capability is beneficial. The resistance can be pre-loaded with a DC current

in a way that it matches the system impedance. Once RF power is added as well, the DC power can be reduced to keep the resistance at the same value. The amount of DC power represents the RF power very precisely and can be calculated with low effort.

A change in ambient temperature during the RF measurement will have an impact on the accuracy of the results. Therefore, it is recommended to use an additional reference circuit nearby. The reference circuit should be close enough to see the same ambient temperature change as the sensor element, but at the same time be electromagnetically isolated from it.

Prerequisite for the implementation of a thermistor within a standard MMIC process is the availability of a material with a significant TC. Infineons' automotive radar technologies (described in detail in Chapter 3) do offer a variety of different materials and devices. For the following section the TC of the most promising material is investigated.

Figure 2.12 shows the behavior of a p-type polysilicon resistor over temperature in the B7HF200 technology. For the measurements, the temperature of the Device Under Test (DUT) is controlled from the wafer backside with a thermo chuck. This implies that the resistive material is heated up passively without any self-heating effects. It is observed, that the resistor has a TC of $958 \cdot 10^{-6}\,\mathrm{K}^{-1}$. A more detailed analysis of the TCs of the materials in B7HF200 and B11HFC is given in Chapter 4.

2.2.2 Calorimeter

The calorimeter power sensor for millimeter wave applications converts electric power to heat, similar to the thermistor approach. The main difference between the two is that for the calorimeter the absorber is separated from the sensor element.

A simplified illustration of a calorimetric power sensor is shown in Figure 2.13. The RF signal v_{rf} is applied to the absorber element - which can again be a resistor matched to the system impedance - leading to power dissipation and accordingly heat. The absorber, which is a heat source now, will lead to a temperature rise in the thermally coupled surroundings also affecting the resistive sensor element. The resistance of the sensor element is detected and gives a direct measure of the applied RF power level.

Compared to the thermistor approach, no additional circuitry is required to separate the RF path from the DC measurement path, but instead the sensor element has to be electromagnetically isolated from the absorber. This requirement is challenging to realize in standard MMICs.

Per se, the shown calorimeter has no DC substitution capability. If this feature is required, additional circuitry is required to separate the RF path

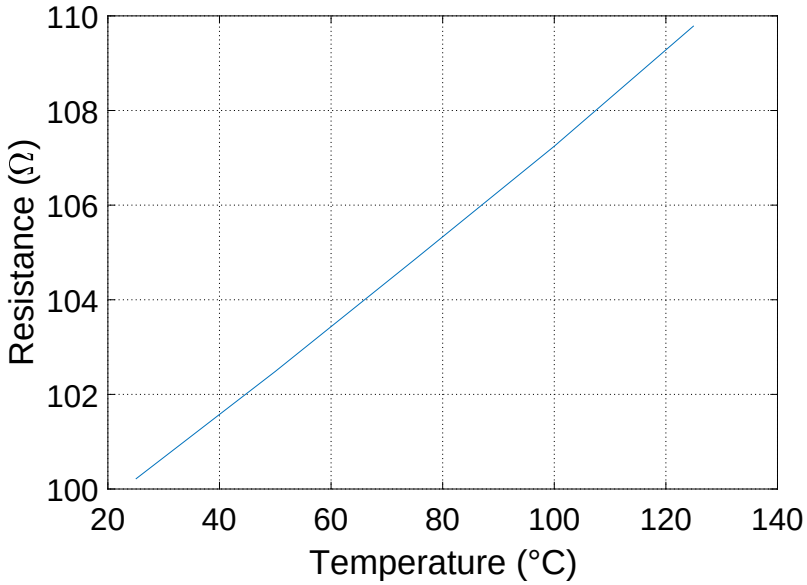


Figure 2.12: Behavior of a polysilicon resistor (p-type) versus temperature in B7HF200.

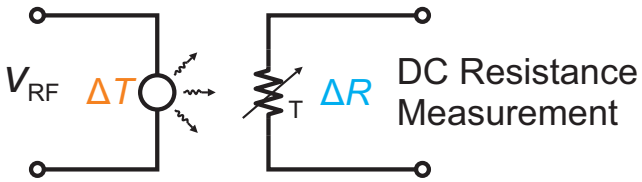


Figure 2.13: Simplified calorimeter setup.

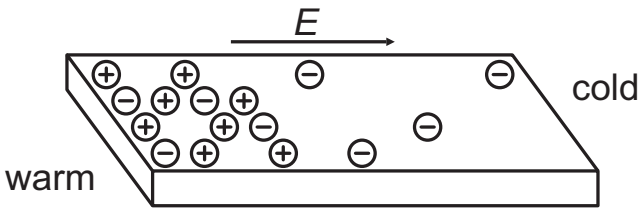


Figure 2.14: Electric field generation due to heat in a thermocouple. Drawing based on [Keysight Tec 14].

from the DC measurement path similar to the thermistor. To circumvent the challenge of changing ambient temperature drift, a reference sensor can be employed.

2.2.3 Thermocouple

Thermocouple sensors are usually made of metallic and/or semiconductor materials. The principle is based on the fact that a piece of metal or semiconductor generate a voltage from one end to the other, if there is a temperature difference from one end to the other. The temperature rise at one end of the material is caused by the RF signal and forces additional free electrons. As the amount of free electrons is now higher at the warm end of the material, there will be statistical diffusion from electrons to the cold side. An illustration of this behavior is shown in Figure 2.14. The positive ions are bound to the atom lattice and cannot move freely within the material. They will generate a force upon the free electrons according to Coulomb's law. A static condition is given, when the forces caused by Coulomb's law and the diffusion are equal. The force caused by Coulomb's law can be represented by an electric field E as indicated in Figure 2.14. An integration of the electric field along the material will result in a voltage. This effect is also known as Thomson electromotive force [Keysight Tec 14].

A similar diffusion behavior as already explained above, is observed at the contact edge of two different materials which again result in an electromotive force also known as the Seebeck effect.

A thermocouple is often implemented as a loop of different materials as shown in Figure 2.15. The contact of the two different materials acts as the absorber and heats up. The result for a closed loop is a current flow. If the loop is broken the net thermoelectric voltage can be measured with a sensitive volt meter [Keysight Tec 14].

The implementation of thermocouple detectors in MMICs is cumbersome. Usually, existing technologies do not offer the required materials to form ef-

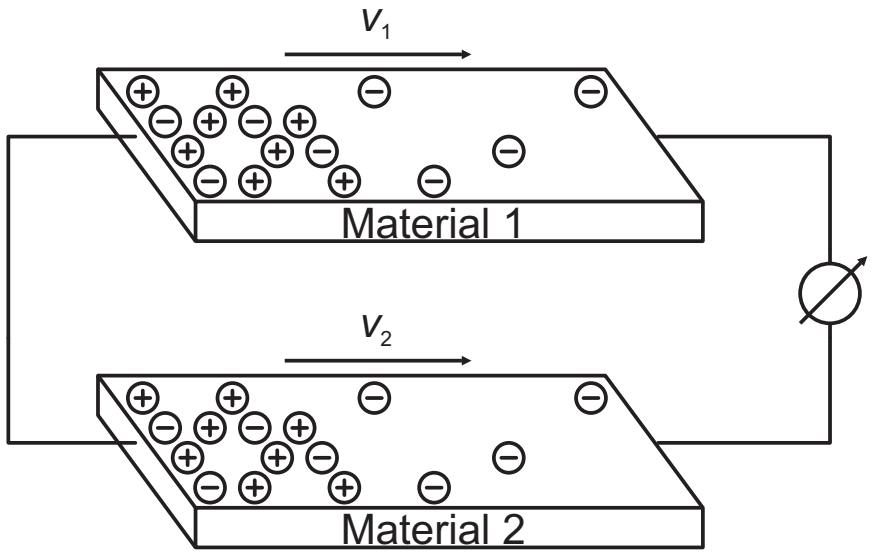


Figure 2.15: Thermocouple loop. Drawing based on [Keysight Tec 14].

ficient thermocouples. Nevertheless, there is an approach reported where a standard Complementary Metal-Oxide-Semiconductor (CMOS) technology is extended by an additional etching step to form an on-chip thermocouple without additional lithography [Milanovic 97]. However, the presented results have only been demonstrated in the laboratory and not for high volume production.

[Szakmany 17] investigates a thermocouple sensor at frequencies around 600 GHz. Therefore, antennas are processed on a silicon wafer which will heat up if RF power is applied from a horn antenna to the IC. The thermocouple element is also processed on the silicon substrate but uses rather exotic materials to increase the thermoelectric effect.

Furthermore, there are publications on thermocouples in Gallium Arsenide (GaAs) technologies [Zhang 15] [Zhang 17]. These solutions employ micromechanical processing steps in a laboratory environment to achieve the required thermoelectric behavior.

To the best knowledge of the author, there are no state of the art publications on thermocouple sensors in modern CMOS/Bipolar CMOS (BiCMOS) foundry technologies available.

2.3 Comparison

The goal of this work is to investigate new BIST mechanisms for power detection. The uppermost criterion is that the sensor concept can be integrated in

modern silicon based technologies, more precisely the technologies described in Chapter 3. This requirement is already taken into account in the following comparison of the earlier mentioned detector types. Table 2.1 lists the different sensor types and points out what the strengths and weaknesses of the particular sensor is, compared to the others.

The main advantage that all electrical based power sensor concepts have compared to the thermal based approaches is the dynamic range. The diode and Meyer detector benefit here from their non-linear characteristic and the dynamic range of the logarithmic amplifier can be extended by using multiple stages.

Furthermore, the response time of the electrical detectors is usually smaller than for thermal based solutions [Brush 07]. However, for the power measurement of continuous wave sinusoidal signals like in Frequency Modulated Continuous Wave (FMCW) radar systems the response time is not a critical parameter.

One drawback for diode based power detectors is that they act as peak detectors for moderate to high input power levels. If the RMS average value of the RF signal is required, the user needs to know about the peak-to-average-power ratio of the waveform to calculate the power. Another disadvantage is that a calibration of the sensor is necessary for precise measurements of absolute power levels. The mentioned drawbacks are also existent for the Meyer detector, however, with some modifications (added attenuators) it is also possible to operate it as an RMS detector over a relatively wide range [Zhang 06].

The logarithmic amplifier does by default detect the RMS value of the RF signal. The approximation error (log error) can be reduced by using multiple stages but the A_0 cells are facing other challenges at around 80 GHz. One of them is the temperature dependence of the gain, which leads to a strong temperature dependence of the whole detector. Another one is the silicon area which is consumed by the inductive loads (see Section 2.1.3 and [Hammerl 12]).

The thermal based power detectors do all have in common that they are RMS detectors per se. For the implementation in a standard CMOS/BiCMOS semiconductor process however, they are facing some challenges. Especially the standard calorimeter and thermocouple approaches are difficult to integrate. The calorimeter which has separate elements for the RF termination and the sensor element, requires electromagnetic isolation between these elements, which is challenging in MMIC design. The sensitivity of the thermocouple sensor strongly depends on how pronounced the thermoelectric effect is in the used material. Standard processes usually do not offer the required manufacturing steps and materials to form efficient thermocouple sensors. In

Table 2.1: Comparison table of discussed power sensor concepts.

	Diode	*Meyer*	*LogAmp*	*Thermistor*	*Calorimeter*	*Thermocouple*
Detection Principle	peak	peak	rms	rms	rms	rms
Response Time	+	○		○	○	○
Implementation Effort	+	○	○	○	○	–
Temp. Dependency	○	○	–	○	○	○
DC Substitution	–	–	–	+	○	○
Calibration needed?	yes	yes		no	no	no

contrast to this, the thermistor power sensor implementation is quite straight forward. The termination and sensor element are combined in one temperature dependent layer. Process variations can be compensated by applied DC power leading to a precise termination (i.e. 50 Ω).

Another advantage for thermal based sensors (and especially for thermistors) is the DC power substitution possibility. This opens up the door for accurate absolute power measurements, without additional calibration effort or measurements at the operating frequency.

2.4 State of the Art in Automotive Radar Applications

One core part of modern automotive radar modules is the transceive MMIC. These ICs usually contain at least an RF signal source, a mixer in the Receiver (RX) part and a high performance power amplifier in the Transmitter (TX) part.

From an application point of view it is also necessary to have a power monitoring unit at the output of each TX channel to determine how much power is actually delivered to the Printed Circuit Board (PCB). For this scenario a combination of a directional coupler and diode-based power sensors has become the state of the art solution for bipolar and BiCMOS [Knapp 12] as well as for CMOS technologies [Texas Instru 17]. Lately, it has been demonstrated that this approach can be used up to frequencies of 200 GHz

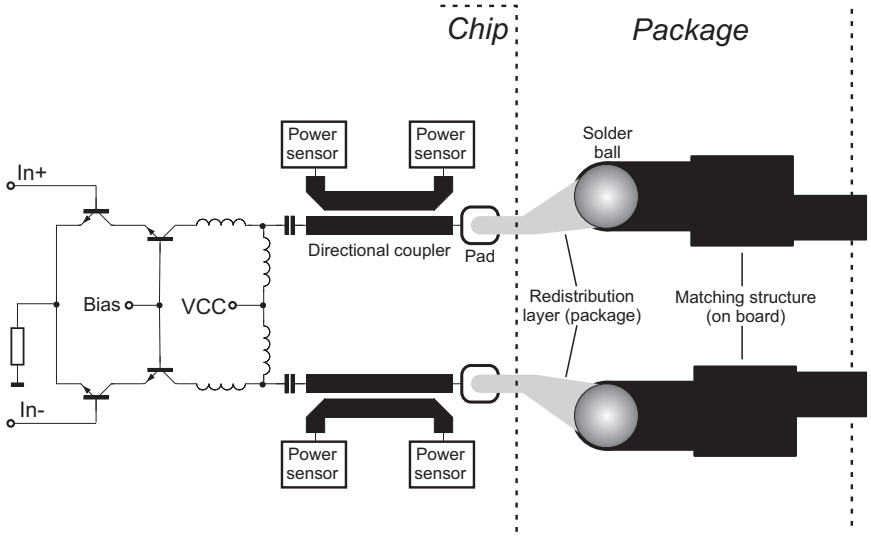


Figure 2.16: State of the art TX power sensor concept [Knapp 12].

[Stärke 18].

Figure 2.16 shows a simplified block diagram of a product-like TX output. On the IC, there is a differential cascode power amplifier stage which is AC coupled to the directional coupler. This four port coupler is designed to deliver a small portion of the forward traveling signal to one port, and a portion of the reflected signal (which is ideally zero) to the other port. The coupling factor is around $-15\,\mathrm{dB}$ to have minimum impact (losses) on the transmitted signal power. The power sensors connected to the coupled ports need good sensitivity to detect signals in the range of $-5\,\mathrm{dBm}$ and below. Therefore, diode based sensors are used in this case.

The transceiver IC is packaged with a state of the art embedded Wafer Level Ball Grid Array (eWLB) process, which suits for millimeter wave applications [Brunnbauer 06] [Böck 15,b]. The figure shows the package transition including the Redistribution Layer (RDL), the solder balls and the passive matching structures on the PCB.

Obviously, the power sensor for the forward direction gives a direct measure for the transmitted RF power. This can be used to verify the functionality of the IC and to reduce the power for efficiency reasons if possible. The reverse sensor suits well for the PCB matching network design. It can be optimized until the reverse sensor output is minimized.

As earlier mentioned, the diode power sensors are only able to perform a relative power measurement and need to be calibrated. To get a relation between the absolute RF output power and the sensor output voltage it is necessary to perform a measurement at the operating frequency around

80 GHz. From a volume testing point of view, this has to be avoided to keep the price at a competitive level. One possibility is to characterize selected samples from time to time at the operating frequency. Assuming that the process variation of the sensors from IC to IC and over time is less than a certain value, a margin for the sensor accuracy can be defined to circumvent RF measurements for every single IC. However, the smaller the defined margin is for the sensors, the more flexibility is given for applications which use the sensor.

The margin of the sensor characteristic can be reduced, if the power sensors can be calibrated individually for every single IC. Therefore, a BIST structure has to be able to measure the absolute RF power while barely influencing the performance of the device or consuming a large area. The thermistor principle described earlier, theoretically fulfills the given requirements and is therefore investigated during this work. Different ways of implementation of the thermistor power sensor are discussed and evaluated in the later chapters of this work, after starting with an introduction to the available automotive qualified radar technologies of Infineon.

Chapter 3

Overview of Silicon-Based Bipolar Technologies

Since many years, CMOS technologies have a dominant market position for digital applications like processing units for personal computing or microcontrollers for industrial applications. Also the lower GHz frequency market has been captured by CMOS rapidly by offering e.g. chipsets for mobile communications. However, for applications in the millimeter wave segment bipolar technologies are still dominating the market.

Main drivers for the increasing amount of CMOS solutions are less power consumption and better scalability especially in digital applications. This results in dense integration levels at even lower costs compared to bipolar-based solutions.

These drivers however, have less impact on analog circuit designs since the requirements on the transistor parameters and attributes are different from digital designs. If for example a bias reference network is only implemented once to feed multiple building blocks, the complete IC will not benefit as much from a lower power consumption or less space that is required. The most relevant requirements for these kind of networks are accuracy and independence from ambient temperature, rather than current consumption and scalability. In these applications, the characteristics of standard bipolar transistors are valuable. For most applications a parasitic bipolar transistor within a CMOS technology can be exploited to meet the requirements.

Another criterion for not using CMOS technologies is simply the lack of performance. For example high-power applications still make use of bipolar-based technologies. A well known example is the Insulated Gate Bipolar Transistor (IGBT), which has a low series resistance in conduction mode perfectly suitable for moderate duty cycles at high currents of more than 1000 A.

Another field of application where bipolar is preferred over CMOS because of performance reasons is high-speed circuitry. The combination of low parasitics and high current densities at moderate breakdown voltages allows robust circuit design. Maximum transit frequencies (f_{T}) and oscillation frequencies (f_{max}) of more than 500 GHz and 700 GHz are achieved in latest Silicon Germanium (SiGe) BiCMOS technologies [Heinemann 16].

Main applications for these technologies are automotive radars and communication systems, as their spatial accuracy and data rates profit from the increased operating frequencies compared to existing solutions. Advanced SiGe BiCMOS technologies feature additional CMOS process steps for the integration of digital building blocks and base-band processing.

In the next section, the characteristics of silicon-based HBT technologies in general will be further explained, followed by detailed information on the Infineon in-house technologies B7HF200 and B11HFC.

3.1 Advances of SiGe-Based HBT Technologies

The most commonly used benchmark parameters to compare the speed of a transistor in a specific technology are the maximum transit and oscillation frequencies f_{T} and f_{max}. The transit frequency of a single transistor is defined as the frequency where the small signal current gain drops to unity. The maximum oscillation frequency is defined as the frequency where the maximum available (unilateral) power amplification of the transistor equals 1. In addition to f_{T}, the maximum oscillation frequency f_{max} also depends on the collector-base capacitance C_{BC} and the base resistance R_{B} (see Equation 3.1), which relates the parameter closely to the performance of a circuit design.

$$f_{\mathrm{max}} \approx \sqrt{\frac{f_{\mathrm{T}}}{8\pi R_{\mathrm{B}} C_{\mathrm{BC}}}} \tag{3.1}$$

Both, f_{T} and f_{max}, are usually extrapolated from their gain at lower frequencies and have an optimum at a specific collector current density J_{C}.

Furthermore, the Current Mode Logic (CML) gate delay τ_{GD} of ring oscillators is used to compare the performance of different technologies [Reisch 03]. As the gate delay of a ring oscillator depends not only on the core transistor and its parasitic effects, but also wiring and other layout aspects, it is considered to predict the performance and behavior for speed-dependent circuit blocks like Voltage Controlled Oscillators (VCOs) and dividers more

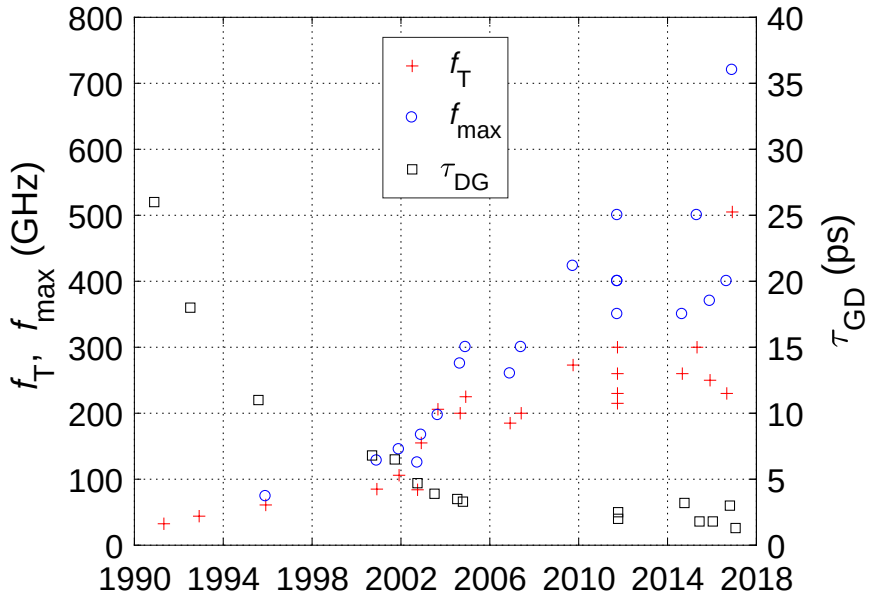


Figure 3.1: Development of f_T, f_{max} and τ_{GD} of HBTs in silicon-based technologies.

accurately than f_T and f_{max} do.

A rule of thumb says that f_T has to be at least 3-5 times higher than the operating frequency for proper circuit design. Figure 3.1 shows the significant publications in SiGe HBT development since 1991. By the time f_T reaches 200 GHz in 2003 the design of circuits in the E-Band range from 60 to 90 GHz became possible for silicon-based technologies. The design of a fully-integrated VCO around 80 GHz in 2004 [Li 04] made the automotive radar market accessible for cost-efficient SiGe-based solutions.

The development of SiGe HBT technologies continues up to now, further improving the key parameters f_T, f_{max} and τ_{GD} to 505 GHz, 720 GHz and 1.34 ps, respectively [Heinemann 16]. Main driver for this evolution are automotive radar applications. The need for autonomous emergency breaking systems in the medium-class car segment (included in the European New Car Assessment Programme (EuroNCAP) rating since 2014 [Ratingen 16]) pushes former niche products to high volumes.

The speed of an HBT is mainly limited by its transit time, parasitic resistors and capacitors, which are formed by the base, collector and emitter regions. Figure 3.2 indicates where the most limiting parasitics are located within the core npn HBT. The inner and outer capacitances which are formed between the base and emitter region are abbreviated by C_{BEi} and C_{BEo}, re-

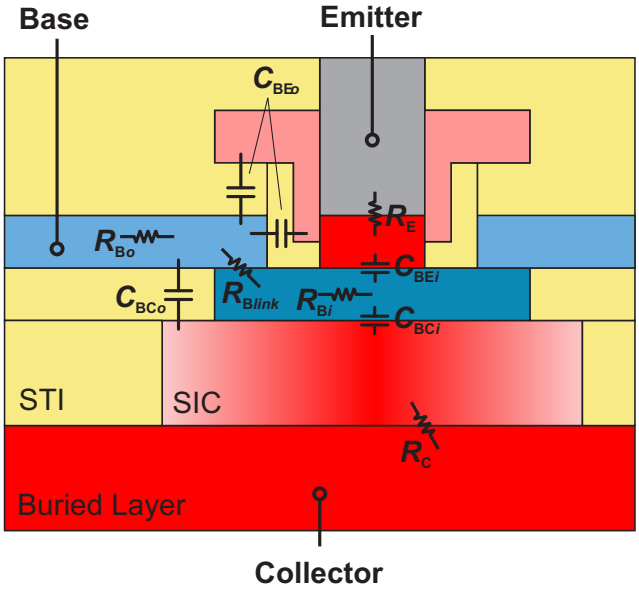


Figure 3.2: Simplified npn HBT cross section showing parasitic elements (not to scale).

spectively. The capacitances which are formed between the base and collector region are also split into an inner part (C_{BCi}) and an outer part (C_{BCo}). The resistance of the connection of the collector region and emitter region (R_{C} and R_{E}) is minimized by high doping levels. For a better understanding of the base structure, it is necessary to split the resistance of the SiGe base region into three parts. The part in the center is called inner base resistance (R_{Bi}), the outer base resistance (R_{Bo}) is located towards the edge of the cross section. The base link resistance (R_{Blink}) in between the two regions describes the behavior of the layer transition.

Lateral scaling of the transistor will reduce the overlap between the regions resulting in reduced parasitic resistance and capacitance hence increasing the speed of the transistor [Chevalier 11]. Furthermore, an optimized sub-collector concept using Shallow Trench Isolation (STI) can be used to increase the performance of the HBT. The STI mainly reduces the parasitic capacitance C_{BCo} between the base link region and the highly doped buried collector layer. Coupling to the nearby substrate is minimized by Deep Trench Isolation (DTI) surrounding the transistor. The trenches are typically filled with polysilicon.

The scaling measures will increase the performance of the conventional HBT to a certain extent at which the speed is mainly limited by the base link resistance R_{Blink}. The resistance in this transistor part results from the

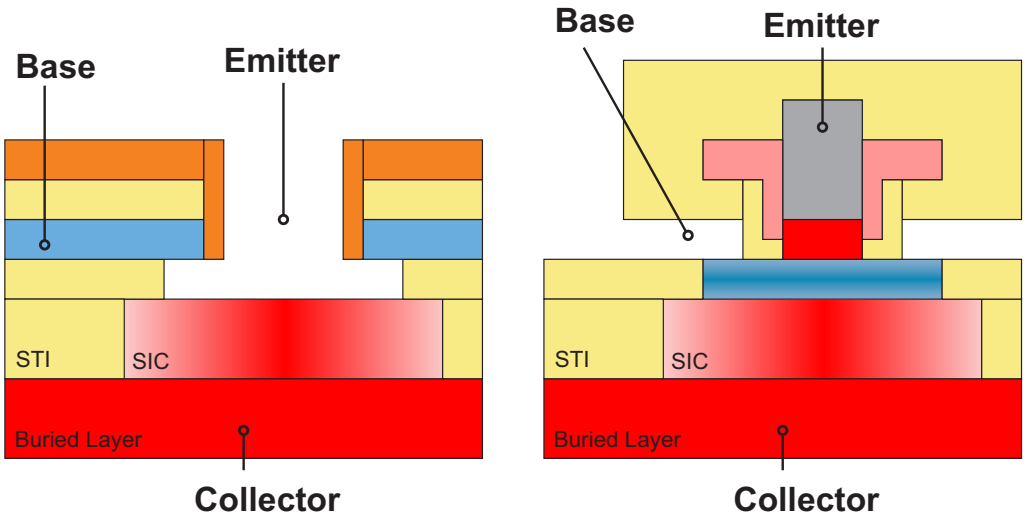


Figure 3.3: Cross section of the conventional HBT concept (a) and the EBL concept (b). Drawings based on [Fox 11].

non-monocrystalline area, which connects the active base of the transistor to the polysilicon electrodes.

Figure 3.3a shows the cross section of a conventional HBT before the SiGe base is formed. A wet etching process opens the oxide above the Selectively Implanted Collector (SIC) forming a self-aligned polysilicon overlap of the base electrodes above the active transistor area. A precise (self-aligned) implantation of the collector is done before the SiGe base is grown using a Selective Epitaxial Growth (SEG) manufacturing step. This process step connects the active base region to the polysilicon electrodes. The critical area where the SEG base touches the polysilicon requires additional annealing to reduce the base link resistance R_{Blink}. Unfortunately, the high temperatures during link anneal broaden the sharp base profile resulting in reduced f_{T}. Carbon is added to the active SiGe base in order to reduce diffusion at high temperature processing steps. Literature refers to this modification as SiGe:C. Nevertheless, the link anneal trades f_{T} for a lower base link resistance.

The base link resistance can be improved by using an HBT architecture with an Epitaxial Base Link (EBL) [Fox 11]. Figure 3.3b shows a cross section of the HBT before the EBL is grown. After removing a sacrificial nitride layer, the outer parts of the active base region are accessible for the base link growth. No additional link anneal is required potentially resulting in higher f_{T}. In this HBT architecture, the emitter is completely structured before the base link is formed.

Another concept which literature refers to as Elevated Epitaxial Base (EEB) shows similar RF performance as the EBL architecture [Heinemann 10]. This concept is processable with a Non-Selective Epitaxial Growth (NSEG) SiGe base simplifying process complexity.

The Growth in One Go (G1G) architecture also uses an NSEG to form the base and the collector in one step saving masks and simplifying complexity [Huylenbroeck 09].

Due to the significant performance increase of the EBL concept compared to the conventional processes it is expected that the next generations of SiGe HBT technologies will be based on this concept or similar ones which offer low-ohmic monocrystalline base links. These next generation technologies will contribute to more efficient and robust circuit design in the existing automotive radar frequency band around 80 GHz as well as to the acquisition of higher frequency bands which offer huge bandwidth and might therefore be suitable for new millimeter wave applications.

3.2 SiGe HBT Technologies at Infineon

There are two different SiGe HBT technologies used to manufacture the circuits described in this work. Both technologies (B7HF200 and B11HFC) are provided by Infineon Technologies AG and use the conventional HBT architecture as described in 3.1. B7HF200 as well as B11HFC are automotive qualified technologies mainly developed to provide products for the automotive radar market. Optionally, the products can be packaged with an advanced eWLB process [Brunnbauer 06, Böck 15,b]. As B11HFC is the successor technology of B7HF200, they have a lot in common regarding available devices - especially for RF applications - and the metal stack which is shown in Figure 3.4.

Both technologies offer polysilicon resistors which are located below the lowest metal layer M1. Due to their close physical positioning to the active transistors they are e.g. used as degeneration resistors in current source configurations keeping the parasitic capacitance at a minimum. Additionally, there is a silicide option for the polysilicon resistors which reduces the sheet resistance to less than $15\,\Omega/\square$. Silicided polysilicon resistors might be used as an additional wiring option or when a small resistance close to a transistor is required. The silicide option also affects the temperature behavior of the device.

The design of conventional VCOs requires voltage dependent capacitors. Therefore B7HF200 and B11HFC offer varactors of different sizes depending on the application. Furthermore, the also available Junction Capacitor

(JCAP) is based on the varactor structure. This JCAP device has a relatively low quality factor and therefore suits perfectly as a filter capacitor between the supply and ground voltage on the IC.

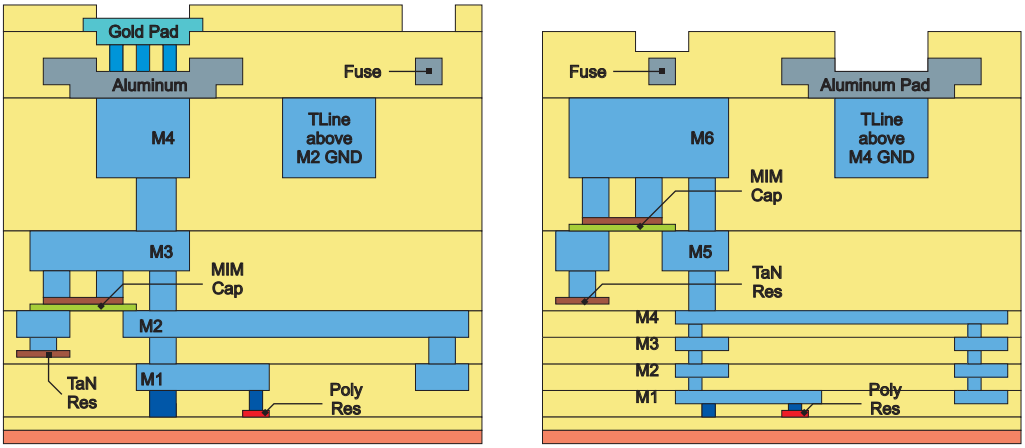
Passive RF components, such as transmission lines, Metal-Insulator-Metal (MIM) capacitors and precise Tantalum Nitride (TaN) resistors are located in the upper part of the metal stack.

Proper RF signal distribution requires transmission lines with a defined characteristic impedance Z_{L}. Transmission lines supported by the Process Design Kit (PDK) for B7HF200 and B11HFC are implemented as microstrip waveguides using a thick, low-loss top metal layer above a defined ground plane. Depending on which metal layer is defined as the ground plane, the geometry of the microstrip waveguide changes and therefore also Z_{L}. For the used technologies, an often required Z_{L} of $50\,\Omega$ can be achieved by skipping one layer between the signal path and the ground plane. The transmission line Parameterizable Cell (P-Cell) in the PDK also supports differential co-planar waveguides which are mostly used for RF differential signal distribution.

The MIM capacitor in B7HF200 and B11HFC is implemented as a lateral plate capacitor. It is mainly used for AC coupling in the RF signal path or in low-pass filters. In terms of accuracy and quality factor, the MIM capacitor is well ahead compared to the previously mentioned JCAP. However, as for all thin dielectrics, the usable MIM capacitor area is limited by reliability issues. Wherever possible, MIM capacitors are replaced by JCAPs. The location of the MIM capacitors in the upper part of the metal stack simplifies the combination with transmission lines to form passive matching networks efficiently.

The more complex manufacturing steps of the TaN resistor result in an accurate sheet resistance compared to the polysilicon resistor. The process target is to eliminate any dependency on temperature of the TaN resistor. The location in the metal stack on the one hand results in an increased thermal resistance compared to the devices which are located close to the substrate (like poly resistors and transistors). Therefore, the current density limits are smaller leading to larger devices in the design. On the other hand, the location of the TaN resistor is beneficial to connect other passive devices in the upper layers. Another advantage of the location in the metal stack is that there is less parasitic capacitance towards the substrate. In general, the sheet resistance of the TaN resistors is smaller than for the poly resistors.

The RF device library is completed by aluminum fuses. These structures can be used for post-process adjustments like trimming of the VCO frequency or storing simple data patterns like a device serial number. B11HFC also offers electronix fuses which can be used to replace most of the aluminum



(a) B7HF200 metal stack.

(b) B11HFC metal stack.

Figure 3.4: Metal stack comparison for Infineons' B7HF200 and B11HFC (not to scale).

fuses in the data storage application.

Further technology details unique to either B7HF200 or B11HFC are given in the following sections (3.2.1 and 3.2.2).

3.2.1 B7HF200

B7HF200 is an Infineon in-house SiGe HBT technology which is based on a 0.35 µm process similar to the results presented in [Böck 04,b]. It is an automotive qualified bipolar only process offering different types of npn transistors. The High Voltage (HV) type is optimized in terms of collector-base and collector-emitter breakdown voltages $BV_{\mathrm{CB}}/BV_{\mathrm{CE}}$, whereas the Ultra High Speed (UHS) type is designed for maximum speed. For the High Speed (HS) type maximum speed is traded for increased $BV_{\mathrm{CB}}/BV_{\mathrm{CE}}$. This enables the design of robust Power Amplifier (PA) output stages which are required for automotive radar applications.

The basic stripe configuration for all three types is BEC indicating that the emitter contact is placed between a base and a collector contact. In addition, there are other configurations with multiple stripes available. A double base npn transistor (BEBC) can for example be used to reduce the base resistance. Other configurations are CBEC, CBEBC, CEBEC and CBEBEBC. The reference transistor has an emitter mask size of 0.35 µm × 2.8 µm. Due to emitter-base spacers of 85 nm at each side the effective emitter area is reduced to 0.18 µm × 2.63 µm [Böck 15,a]. A comparison of the three transistor types is shown in Table 3.1.

Table 3.1: Comparison of B7HF200 transistor types in BEC configuration with an emitter mask size of 0.35 µm × 2.8 µm [Böck 04,a, Aufinger 11].

	HV	HS	UHS
f_{T} (GHz)	35	170	200
f_{max} (GHz)	120	250	250
BV_{CB} (V)	14.5	6.5	5.8
BV_{CE} (V)	4.0	1.7	1.5

In addition to the mentioned npn transistor types there are additional P-Cells for the implementation of multiple transistors which are used if the maximum single transistor size is not able to carry the required current. An additional vertical pnp transistor completes the list of active devices. This device is not optimized for speed but fulfills the requirements for bias network designs.

The pads in B7HF200 are made of gold and can be used for bonding as well as other packaging options. The final gold layer is connected to the underlying aluminum with tungsten vias. Also on-wafer measurements can be performed with minimum loss due to the low connection loss between the hard probing needles and the comparably soft gold layer.

The polysilicon resistors in B7HF200 can be doped at different levels to adjust the sheet resistance. Less doping results in a nominal sheet resistance of 1 kΩ/□, the higher doping level results in 150 Ω/□ [Böck 04,a]. The nominal TC_1 of the highly doped version is specified with $1.2 \cdot 10^{-3}\,\mathrm{K}^{-1}$ [Wursthorn 14], whereas the resistor with less doping has a negligible TC_1. By adding the silicide option to the poly resistor the TC_1 is increased.

Publications show that it is possible to transfer the single transistor speed into highly-performant circuit designs like ring oscillators and frequency dividers. A minimum τ_{GD} of 3.32 ps across the wafer with a deviation of less than 1 % is reported in [Böck 04,b], whereas the qualified high-volume process shows an τ_{GD} of around 4 ps for the UHS transistor. Static and dynamic frequency dividers are shown to work up to 110 GHz [Trotta 05] and 160 GHz [Trotta 06], respectively.

There are several publications available which deal with stand-alone building blocks in the B7HF200 technology. A mixer [Perndl 04], a low noise amplifier [Dehlink 05] and a VCO including a powerful output stage [Li 04] show sufficient performance for automotive radar applications.

Furthermore, a complete three-channel transmitter [Knapp 12] and receiver [Wagner 12] in a plastic package are demonstrated. Those circuits

Table 3.2: Comparison of B11HFC transistor types in BEC configuration with an emitter mask size of 0.22 µm × 2.8 µm. [Al-Eryani 17, Ahmed 18]

	HV	MS	HS
f_{T} (GHz)	55	80	250
f_{max} (GHz)	200	250	370
BV_{CB} (V)	14.5	13.4	5.3
BV_{CE} (V)	3.7	2.3	1.5

show that all essential building blocks for packaged millimeter wave products can be realized in the B7HF200 technology.

3.2.2 B11HFC

B7HF200 shows that the RF front-end for automotive radar applications around 80 GHz is feasible with silicon based technologies. The integration of additional digital content in B7HF200 is difficult because of the missing CMOS transistors. To overcome this limitation, Infineon integrates an advanced SiGe HBT process in its 130 nm CMOS process resulting in a BiCMOS technology called B11HFC which is very similar to what is presented in [Lachner 14] and [Böck 15,a]. B11HFC also fulfills the automotive quality requirements and can therefore be used for automotive radar designs.

B11HFC offers three types of npn transistors with different attributes. There is a HV type, a HS type and a Medium Speed (MS) type. A comparison of the three devices is given in Table 3.2. The HS type achieves a minimum CML gate delay of 2.5 ps. The circuit speed performance is shown with static [Knapp 10] and dynamic [Al-Eryani 15] frequency dividers working up to 133 GHz and 217 GHz, respectively.

The polysilicon resistor which is available in B11HFC is designed to have a low TC_1. The nominal specified sheet resistance is around 325 Ω/□ [Issakov 10] and can be drastically reduced by adding the silicide option. This option also increases the TC_1 compared to the default poly resistor.

The performance for circuitry in the automotive radar frequency range from 76 GHz to 81 GHz increases compared to B7HF200. Next to the gate delay, the maximum output power and efficiency of a PA are a good measure for the performance increase caused by the more advanced technology. It is shown that a saturated PA output power of more than 16 dBm and an efficiency of >12 % at 125 °C is feasible [Wursthorn 16]. If a power combining approach is used, a peak output power of >19 dBm is achieved [Furqan 15].

With f_T and f_{max} as high as 250 GHz and 370 GHz B11HFC makes the frequency range above 140 GHz accessible for circuit design in silicon based technologies. A fundamental VCO around 240 GHz including a dynamic frequency divider is presented in [Al-Eryani 16,c]. A PA output power of 14 dBm at 162 GHz is achieved [Al-Eryani 16,d] as well as a wideband push-push VCO with a tuning range of 40 % [Al-Eryani 16,a].

Even the frequency range of >300 GHz can be addressed when using frequency multiplication methods. [Al-Eryani 16,b] employs a frequency doubler to realize a 341 to 386 GHz transmitter.

Chapter 4

Thermistor Power Sensor Concept for on-chip Calibration

As already mentioned in Section 2.4, the state of the art solutions require an initial calibration for the diode-based power sensors in the TX chain. To map a certain output power P_{out} value to the according power sensor voltage V_{det} the RF signal power level needs to be known. As this measurement can not be performed for every single IC due to consumed test time and complexity a trade-off with accuracy is made. Therefore, the actual RF measurement is only performed on a number of selected reference devices to get an average characteristic of the diode power sensor. A margin is added for the process variation to the other samples which are not measured directly at the operating frequency around 80 GHz.

Figure 4.1 shows on the left side which measurements are required externally (off-chip) for the diode power sensor calibration. On the right side the effect of the margin on the characteristic is visualized by broadening the reference line (black) to the margin limits (grey).

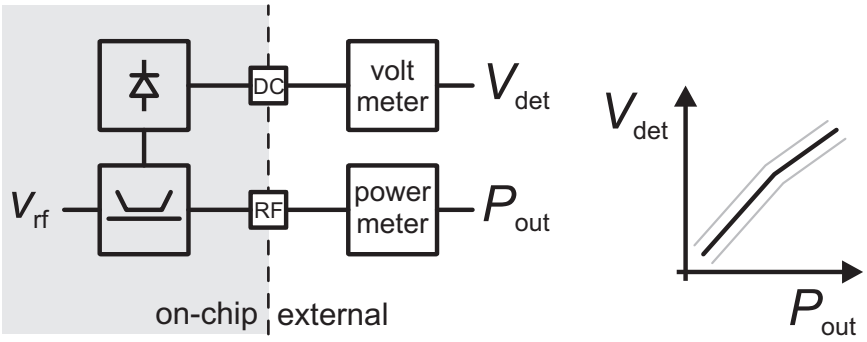


Figure 4.1: Calibration concept for state of the art diode detectors.

The goal of the newly developed power sensor calibration concept it to transfer the external absolute power measurement onto the IC. Therefore, a thermistor based approach is being implemented. As the thermistor can not simply be connected/disconnected from the RF signal path like the external measurement setup it is necessary to also realize a switching or splitting element on the device. As this element is only required during calibration it should have low impact on the final performance of the IC in the application.

The block diagram in Figure 4.2 shows a simplified implementation of the proposed calibration concept. At the input, the directional coupler splits a portion of the signal to the diode-based sensor which provides a DC output signal. The main signal path provides an RF output which can be measured with external equipment at the operating frequency. The thermistor-based sensor requires further signals for evaluation, at the output it provides a DC signal.

The advantage of the on-chip calibration is, that the RF interface connection is no longer required for calibration. The additional DC output which carries the substituted voltage level can be handled by standard test equipment without additional effort. Finally, this enables chip-fine calibration of the existing diode power sensors potentially reducing the required margin for process variation.

In Chapter 5 it is described how the switching or splitting element can be realized on the IC. Furthermore, there are implementation examples given in Chapter 6. In the following sections the behavior and implementation of the thermistor sensor is analyzed and discussed in more detail. A close analysis of the resistive layers in B7HF200 and B11HFC is given. Furthermore, it is described how the standard resistor model of the PDK can be extended by the thermal domain and how the thermal resistance R_{th} and capacitance C_{th} are extracted for modelling. This section also shows how the separation of the DC signal from the RF signal at the thermistor can be implemented. Finally, second order design considerations are discussed and a conclusion is given.

4.1 Thermal Behavior of Resistors in B7HF200 and B11HFC

One fundamental requirement for the integration of a thermistor is that a layer with a sufficient temperature coefficient is available. A further requirement is that the sheet resistance of the layer is in a useful range to create an RF termination around $50\,\Omega$ while maintaining a meaningful aspect ratio

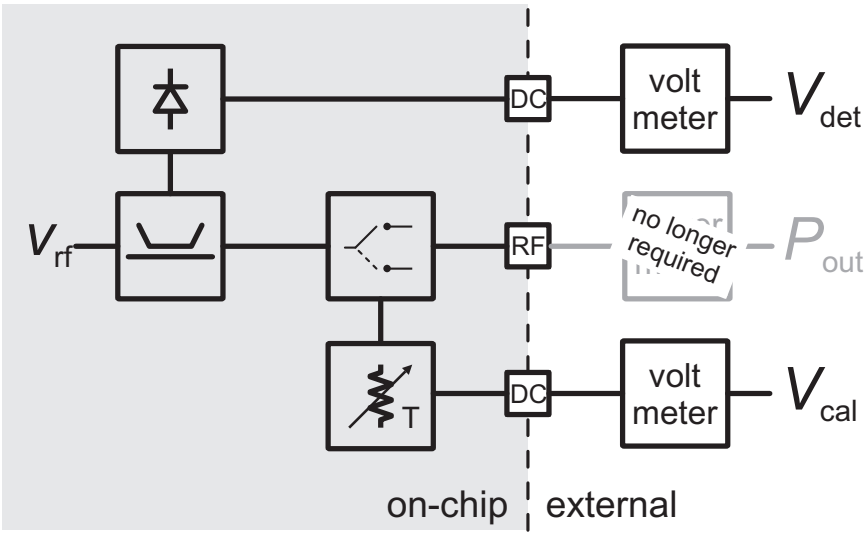


Figure 4.2: Proposal for new calibration concept with integrated thermistor.

(thermistor length/width) in the range of 1 to 10.

Various layers have been investigated in the available technologies. The most promising candidates for each technology have been selected and are shown in Figure 4.3. The shown measurement results are taken from resistor structures which have been designed for modeling purposes. Therefore, the absolute resistance target values are not around 50 Ω but are based on modeling constraints. Nevertheless, this has no impact on the extraction of the temperature coefficient which is related to the slope of the traces in the plot.

Figure 4.3a shows selected layers from the B7HF200 technology. In this technology there are two basic types of polysilicon resistors available, one is n-doped (n-poly) and the other one is p-doped (p-poly). The slope of both types is similar and therefore also the TC. An additional silicide layer can be added to the standard polysilicon resistor reducing the sheet resistance of the device. Usually, this option is used for the connection to the base contacts of the transistors or as an additional wiring option and is therefore part of the standard manufacturing process. As the results from Figure 4.3a indicate, the silicide option also changes the thermal properties of the device. The TC of the silicided polysilicon resistor is more significant than for the standard polysilicon devices.

The well known first order equation for a temperature dependent resistor

$$R(T) = R(T_1)(1 + TC_1\Delta T) \tag{4.1}$$

can be modified and the first order temperature coefficient TC_1 can be

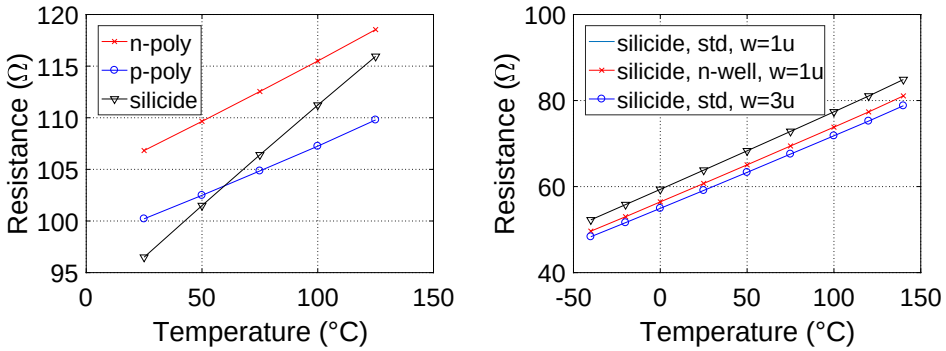


Figure 4.3: Polysilicon based layers in (a) B7HF200 and (b) B11HFC.

calculated from the resistance values measured at two different temperatures as follows

$$TC_1 = \frac{R(T_2) - R(T_1)}{R(T_1)(T_2 - T_1)} \tag{4.2}$$

Using the values at 25 °C and 125 °C leads to a first order temperature coefficient of the silicided poly resistor in B7HF200 of $TC_{1,\mathrm{silB7}} = 2.01 \cdot 10^{-6}\,\mathrm{K}^{-1}$. The sheet resistance of the silicided poly resistor is $R_{\mathrm{sh,silB7}} = 3.0\,\Omega/\square$.

Measurement results of silicided resistors over temperature in B11HFC are shown in Figure 4.3b. As well as for B7HF200 also in B11HFC the silicided polysilicon resistors have the most significant TC. The three traces show results for two different widths (1 µm and 3 µm) and for a device with an additional n-well below. The measurements confirm that none of the modifications has a significant impact on the TC, but the n-well might increase the thermal resistance of the device if the default value is not sufficient for the thermistor implementation.

From the measurement points at 25 °C and 125 °C a first order temperature coefficient for the silicided poly resistors $TC_{1,\mathrm{silB11}} = 2.88 \cdot 10^{-6}\,\mathrm{K}^{-1}$ is calculated. The sheet resistance is $R_{\mathrm{sh,silB11}} = 8.6\,\Omega/\square$.

The previous investigations show that the silicided poly resistors offer the required fundamental properties to serve as a thermistor element.

4.2 Thermal Domain Model Extension

During the design phase of ICs it is necessary to have reliable models of the used devices available. Usually, these models cover the electrical behavior of the device well enough to design functional circuits in the first manufacturing

iteration. Also the behavior over the ambient temperature is covered by the models to run reliable simulations for the required temperature range (i.e. $-40\,°C$ to $125\,°C$).

For accurate simulations of a thermistor however it is required to extend the electrical behavior by effects which are caused by self-heating. Therefore, the temperature of the thermistor device (and the electrical behavior accordingly) has to change if power is applied to it while the rest of the circuitry operates at the given ambient temperature. The implementation of the thermal behavior will allow closed-loop simulations with the desired thermistor behavior.

For accurate modeling of the thermal behavior of the resistor it is required to extend the electrical model by the thermal domain. Therefore, the thermal resistance R_{th} and the thermal capacitance C_{th} are introduced. The thermal resistance describes how much temperature difference occurs in a material if there is a heat flow through this material. It is essential for modeling the self-heating effect. A similar analogy also exists between the thermal capacitance and the electrical capacitance. If connected to their resistive counter part a time constant is formed.

Figure 4.4 shows how the interaction of the thermal and electrical domain works. On the left side the electrical part is shown, the right side shows the thermal part. First of all, it is assumed that only electrical DC signals are present in the circuit. The DC current I through the resistor will according to Ohm's Law force a voltage drop V. The dissipated power P_{d} in the resistor R is responsible for the self-heating of the device and can be calculated from the current and the resistance.

$$P_{\mathrm{d}} = I^2 R \tag{4.3}$$

The dissipated power causes a heat transfer I_{Q} in the thermal domain which is the counter part to the current in the electrical domain and is therefore represented by the current source (I^2R) in Figure 4.4. The heat transfer will cause a temperature difference ΔT in the thermal circuit (analog to a voltage difference in the electrical domain). The thermal capacitance will cause a latency in the signal settling comparable to a capacitor in the electrical domain.

The thermal resistance and capacitance are values which are defined by the material properties and geometry which allows to calculate them. In addition, there are also possibilities to extract them from measurement results. In the following, it is shown how R_{th} is extracted from measurement results and C_{th} is calculated from the geometry of the thermistor surroundings.

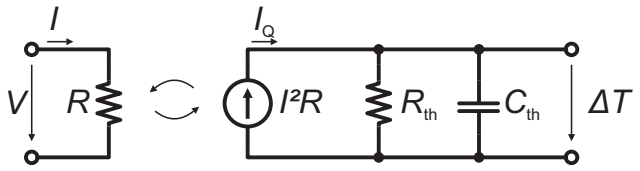


Figure 4.4: Resistor model including a simple thermal domain extension.

Analog to Ohm's Law, there is a definition for R_{th} in the thermal domain:

$$R_{\mathrm{th}} = \frac{T}{I_{\mathrm{Q}}} \tag{4.4}$$

If a heat transport $I_{\mathrm{Q}} = I^2R$ is present at the thermal resistance a temperature difference is caused by that leading to the following formula

$$R_{\mathrm{th}} = \frac{\Delta T}{\Delta(I^2R)} \tag{4.5}$$

Using the expression for the temperature dependent resistance from Equation 4.1:

$$R_{\mathrm{th}} = \frac{\Delta T}{I^2R(T_1)(1 + TC_1\Delta T)} \tag{4.6}$$

Equation 4.6 shows that the thermal resistance can be calculated from the DC current, the resistance at a given temperature, the temperature change caused by the current and the first order temperature coefficient. The following four steps explain how the extraction works. Figure 4.5 shows the measurement results required for the R_{th} extraction and are associated to the four steps.

1. The temperature dependence of the thermistor is measured. Therefore, the device is passively heated up while the resistance is monitored. The current which is required for the measurement has to be low to keep self-heating at a minimum.

2. In this step the dependence of the thermistor on self-heating is derived. Therefore, the ambient temperature is kept at a constant value while DC current is applied. The current will heat up the device and accordingly change the temperature of it. This again leads to a change in resistance which is monitored at the same time. The plot shows the relation between the applied current and the resulting change in resistance.

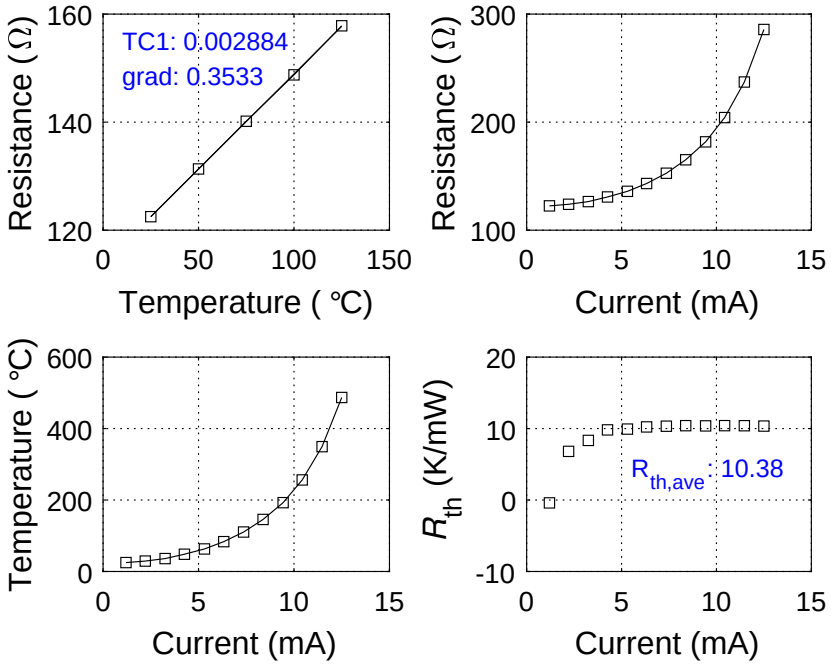


Figure 4.5: Measurement results for R_{th} extraction.

3. To solve Equation 4.6 it is required to know the temperature change which is caused by the applied current. This relation is gained by combining the characteristics measured in step one and two.

4. The value for R_{th} can be calculated for each dc current measurement point. The results are shown in the fourth plot. For small currents the measurements are affected by inaccuracies of the measurement setup and therefore the values deviate from the ones at higher currents. Once the measurements are more accurate at higher currents the values for R_{th} settle and do have only minor variations.

The fourth plot in Figure 4.5 shows the extracted results for the thermal resistance. A value of $R_{\mathrm{th}} = 10.38 \cdot 10^3\,\mathrm{K} \cdot \mathrm{W}^{-1}$ is observed from the plot. This is the complete thermal resistance from the device inside the silicon wafer to the backside of the wafer which is located on a thermal chuck which acts like an (almost) ideal heat sink at a constant temperature.

If the thermal resistance is added to the thermistor model, the electrical resistance value will be calculated for every simulation step. If a DC signal is applied to the thermistor, the dissipated power will lead to temperature

change caused by the thermal resistance. Therefore, also the electrical resistance will change. For the application as an RF power sensor, the thermistor has to deal with AC signals. Again, for each simulation step the dissipated power is calculated and leads to a change in electrical resistance. Hence, if the signal is at its maximum the change in resistance is significant. An instantaneous signal level of zero will lead to an unchanged resistance value. In other words, heating and cooling of the device follows the electrical signal. Up to a certain frequency (depending on the size of the device) this behavior is correct. But obviously, a device will not change its temperature several million times within one second as an electrical GHz-signal does. Therefore, it is required to extend the thermal domain model by this time constant.

The following section explains how the thermal capacitance can be calculated from the technology stack and material constants. Furthermore, is it shown how this affects the device behavior.

As soon as a signal is applied to the thermistor, power is dissipated in the device. This power dissipation leads to heating of the device. The thermal capacitance describes how much heat can be stored in the surrounding material. For the functionality of the thermistor it is required that the thermal time constant resulting from R_{th} and C_{th} is larger than the signal time period. This will ensure that the temperature of the device can no longer follow the electrical AC signal.

The thermal capacitance of any piece of volume can be calculated using the following formula:

$$C_{\mathrm{th}} = c\rho v \tag{4.7}$$

where c and ρ are the specific heat and density of the material and v is the considered volume.

During the design phase of the thermistor, different device sizes have been investigated. For the following calculation a width of $w = 1\,\mu\mathrm{m}$ and a length of $l = 5\,\mu\mathrm{m}$ are considered as this aspect ratio leads to a resistance value of around $50\,\Omega$. The height h of the device is given by the thickness of the polysilicon layer and is around 150 nm in both used technologies. The specific heat and density of polysilicon are $700\,\mathrm{J \cdot kg^{-1} \cdot K^{-1}}$ and $2.3 \cdot 10^6\,\mathrm{g \cdot m^{-3}}$, respectively. Using these numbers in Equation 4.7 leads to a thermal capacitance of

$$C_{\mathrm{th}} = 1.21 \cdot 10^{-12}\,\mathrm{J \cdot K^{-1}} \tag{4.8}$$

The thermal time constant τ_{th} is calculated from the product of the thermal resistance (from Figure 4.5) and capacitance (Equation 4.8):

$$\tau_{\mathrm{th}} = 12.4\,\mathrm{ns} \tag{4.9}$$

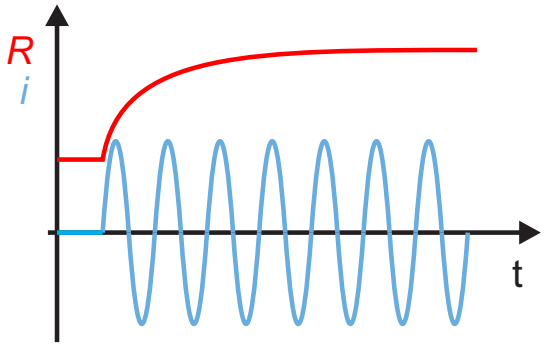


Figure 4.6: Thermistor resistance and current behavior over time.

If this value is compared with the time period of a 80 GHz signal which is 12.5 ps a difference of approximately three orders of magnitude is observed. This leads to the desired behavior that the temperature of the device can no longer follow the applied electrical signal. If the thermistor has to be re-sized for other implementations (i.e. two times 100 Ω in parallel) this statement is still valid.

Figure 4.6 illustrates the described behavior of the thermistor model with the thermal domain extension. The applied sinusoidal current leads to a change in resistance of the thermistor. Note that the current is centered around zero which means it forces current in both directions through the device. However, as the heating is caused by the RMS value of the signal the change in resistance is as expected.

The expected resistance change of the thermistor sensor to applied power can be calculated starting from Equation 4.1 for a temperature dependent resistor (first order temperature coefficient only). With the expression for the thermal resistance in Equation 4.6 a relation between the change in temperature and the dissipated power is derived. With this, the temperature can be replaced by a power term leading to the following formula.

$$R(P) = TC_1 R_{\text{th}} P R(P_0) + R(P_0) \tag{4.10}$$

The equation shows that there is a linear behavior between the applied power P and the resistance. This behavior is appreciated for the implementation as a sensor element.

4.3 Practical Thermistor Implementation

So far, the thermistor termination was treated as a box in the block diagram. For a practical implementation at around 80 GHz there are additional bound-

aries caused by the operating frequency. In the following it is discussed how the thermistor termination can be realized within the B7HF200 and B11HFC technology.

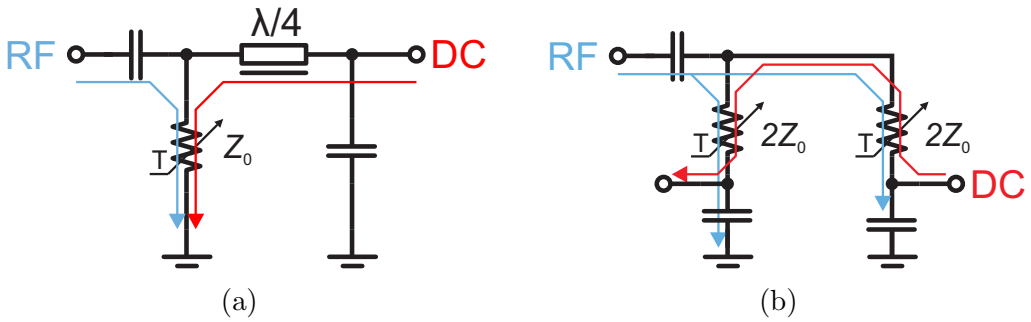
As mentioned earlier the thermistor terminates the system which provides the RF signal. If this termination matches the system impedance the complete power will be dissipated in the device and no signal is reflected into the source. Therefore, one goal is to design the thermistor with the system impedance of $50\,\Omega$. Furthermore, it is required to monitor the resistance value while the RF power is applied. The required DC signal through the thermistor for monitoring has to be split from the RF signal path to prevent performance degradation due to additional parasitic signal paths. For precise resistance monitoring it is necessary to implement a 4-wire concept.

Figure 4.7a shows one way to realize the thermistor termination. The RF signal is fed to the thermistor device through the coupling capacitor. The thermistor is designed to directly provide the system impedance. The DC signal for monitoring purposes is applied from the right side through the $\lambda/4$ transmission line. The transmission line is AC grounded at the right end. This electrical short will transform into an open at the other end of the transmission line in terms of RF behavior. Therefore the applied RF signal only faces the thermistor impedance and is decoupled from the DC signal path. A 4-wire resistance measurement can be realized by doubling the $\lambda/4$ and the grounding capacitance part.

The required space for the mentioned solution is dominated by the $\lambda/4$ transmission line. Especially for the 4-wire measurement solution with two transmission lines this is a major drawback of this solution.

An alternative solution is shown in Figure 4.7b. The RF signal is again AC coupled at the input. Two thermistor elements in parallel form the desired termination of $50\,\Omega$ which is required for the impedance matching. From an RF perspective both elements are grounded. The coupling capacitors towards ground allow a different DC signal path through the thermistors in series. For the functionality one capacitor would be sufficient but to keep the symmertry in the RF path a second capacitor is added. An additional de-coupling of the succeeding DC peripherals is not necessary as the node is RF grounded anyways. This saves the area for the transmission lines and therefore reduces the required space significantly compared to the earlier mentioned solution.

A layout of the final implementation of the thermistor termination is shown in Figure 4.8. The RF input signal is applied from the top side with a transmission line on M6 (purple). A via stack down to M1 (green) at the end of the transmission line connects the silicided polysilicon resistors (red). At the lower end of the resistors is a via stack up to M6 again to connect the



(a) (b)

Figure 4.7: Examples for the implementation of the thermistor termination.

MIM capacitors for AC grounding. The capacitors are not completely visible in the figure. The 4-wire measurement connections are also connected at the lower end of the resistors. For each wire there is a separate TaN resistor connected in series (horizontally, brown).

4.4 Further Design Considerations

During the implementation phase of the thermistor termination additional topics are considered. First of all, it is required to ensure a thermal isolation of the thermistor to achieve significant self-heating. Therefore, any unnecessary metal shapes are blocked from the closer surroundings as they will reduce the effective thermal resistance.

To keep the heat transfer from the device wiring at a minimum, the connections towards the end of the thermistor devices should be thin and massive metals should be far away. However, this is contradictory to the optimum RF solution which benefits from a compact layout. In this case it is preferred to have a proper termination with short metal interconnects for good RF performance.

The functionality of the thermistor is based on the fact that the device heats up significantly compared to the ambient temperature. Obviously, a well isolated device will heat up more efficiently and therefore has a better sensitivity for smaller signals. However, if the self-heating effect is too strong it will lead to permanent damage of the device. This results in a trade-off between sensitivity and reliability for the thermistor. The typical output power levels for automotive radar products around 80 GHz do usually not exceed 15 dBm [Texas Instru 17] which correspond to a power level of approximately 31 mW on a linear scale.

Calculating the maximum applied power level from the top right plot in Figure 4.5 results in 41 mW. For this operating condition the thermistor

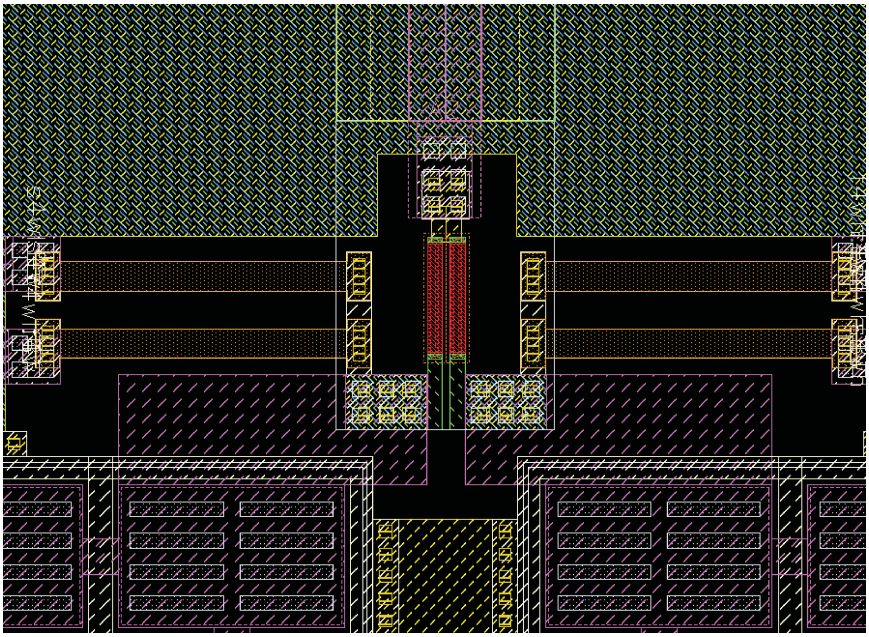


Figure 4.8: Layout of the proposed thermistor termination.

does not show any sign of degradation throughout the complete measurement time in the laboratory. However, Figure 4.5 (bottom, left) shows also that the device temperature at this power level exceeds 400 °C. For a product implementation according to automotive standards additional investigations on the maximum tolerable temperature are required. A trade-off between local heating in the device and sensitivity can be done depending on the reliability requirements.

Chapter 5

Thermistor Implementation in Multi Channel Transmitters

Previous chapters have shown that the available technologies provide the possibility to realize an on-chip thermistor without additional manufacturing steps. Furthermore, it has been shown how the thermistor termination can be implemented with minimum area consumption. In Chapter 4 the proposed power sensor calibration concept was introduced using an (ideal) RF power switch as a black box without further explanation.

The following sections give detailed information on the already mentioned switch topic. Obviously, the generated TX output power can not permanently be dissipated in the thermistor device. The following sections describe two approaches to overcome this issue. The first one has its focus on an additional TX calibration channel whereas the second approach follows the initial idea of having a switch or splitter implemented in the TX channel which is re-used for the application.

5.1 Additional Calibration Path

Usually, modern millimeter wave transmitters or transceivers are equipped with multiple TX channels as shown in Figure 5.1 with two channels. A VCO generates the signal at the desired operating frequency. This signal is then isolated from the succeeding stages using a buffer stage (BUF). Afterwards, the signal is split and distributed to the different TX channels (SPL). The signal in each channel is amplified by a powerful multistage amplifier (AMP) to generate the required output power.

In addition, each channel has an individual power detection unit (PDU) at the output to monitor the power of the transmitted and reflected signal.

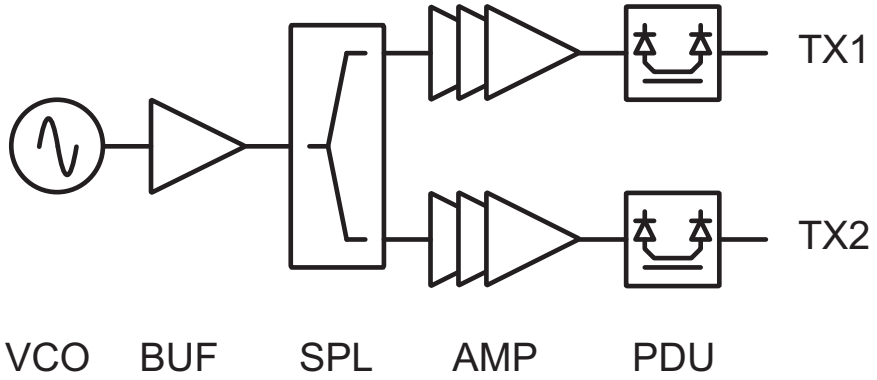


Figure 5.1: Block diagram of a multi channel transmit system with two channels.

The power detection unit of the earlier mentioned state of the art solutions contains a directional coulper and diode based level detectors. These power detection units are built up identically for all channels and therefore their characteristics are identical except for the mismatch within the IC. If the mismatch is taken into account by adding a small margin, the calibration for all the channels reduces to the calibration of one single diode detector which simplifies the process.

The idea to perform the calibration of the diode detector is to add an additional calibration channel which is identical to the TX channels as shown in Figure 5.2. With this approach the challenge of switching RF power efficiently between the thermistor termination and the TX output is solved by the generation of a signal similar to the one in the TX channel. The TX channels which are used for the application are not affected by this and can operate at full performance. The margin which has to be kept for the sensor characteristic is just a minor drawback and less than for the state of the art solution which keeps a margin for variation from wafer to wafer and over lifetime process variation. The described method for calibration is filed in the granted patent [Knapp 17].

Further details on the implementation and design of this approach are given in Section 6.2.

5.2 Switch in Transmit Path

The starting point for the solution using a switch is again the multi TX system which is shown in Figure 5.1. The TX outputs in this block diagram can not be terminated directly with the thermistor. Therefore, each TX

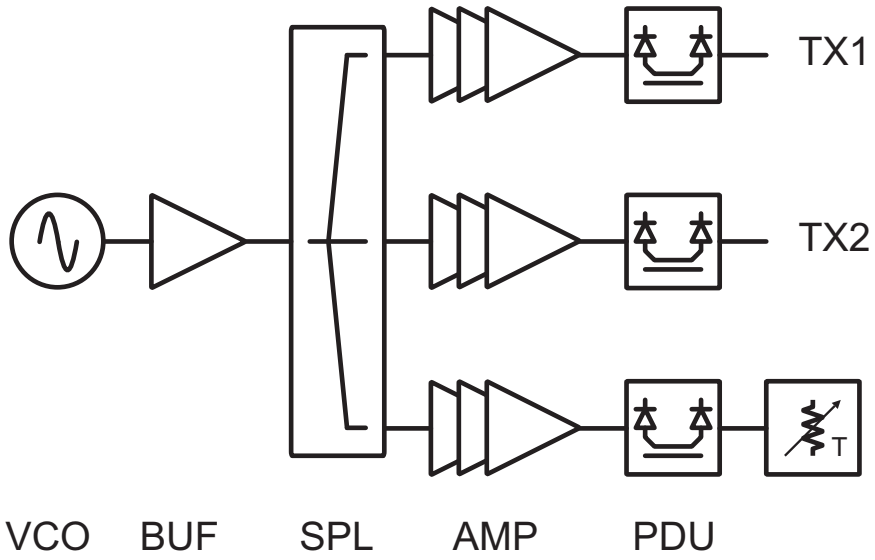


Figure 5.2: Block diagram of a multi channel transmitter with additional calibration channels.

channel requires a switching or splitting element as shown in Figure 5.3.

The simplest solution is to implement a passive power splitter (i.e. Wilkinson splitter) which permanently divides the power in two equal portions. One part is forwarded to the TX output whereas the other portion is fed to the thermistor termination. This simple and robust implementation however comes at the cost of reduced available TX output power. If the passive splitter works ideally a drop of 3 dB is expected. Additional losses due to longer wiring and coupling will add up resulting in a significant power loss in the TX channel. However, for verification of the thermistor functionality this approach is useful as the substituted DC power level can be compared with the power level at around 80 GHz simultaneously.

Alternatively, the passive splitter can be replaced by an active switch to reduce the losses in the TX channel. However, the implementation of an RF switch with sufficient performance is challenging. Nevertheless, literature shows that switches with Insertion Loss (IL) values of 1.4 dB are feasible while maintaining an isolation of more than 19 dB [Schmid 14].

Yet another solution which is from the functionality very close to the switch based approach is to modify the last PA stage to provide a second output which can be used to heat the thermistor. This modification is based on the common Gilbert cell and uses the active switching quad for redirecting the RF power to either of the two outputs. Detailed information and investigations on this approach are shown in Chapter 6.4.

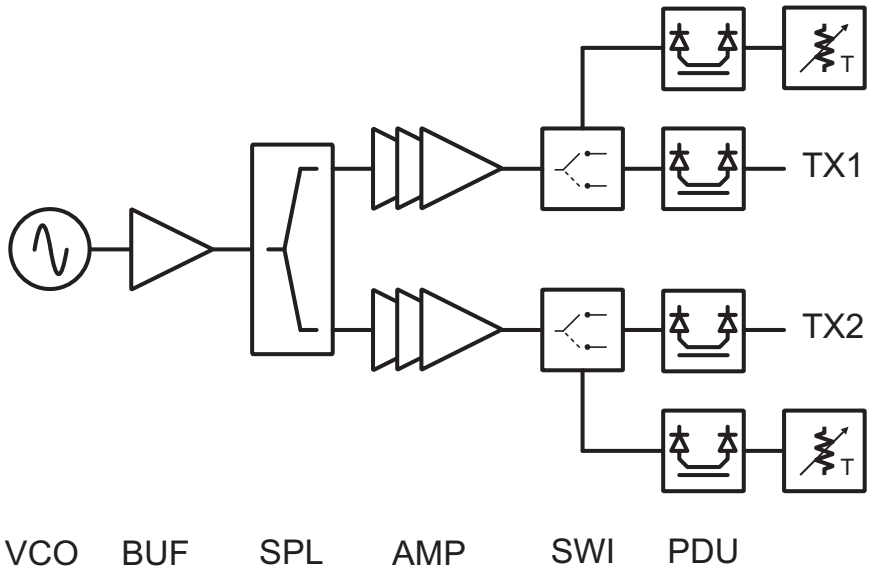


Figure 5.3: Multi channel transmitter with RF switch in each channel.

5.3 Comparison

A critical parameter in existing automotive radar products is the minimum specified TX output power. When comparing the two proposed solutions with respect to this number, the solution with the additional calibration path delivers better results as there is no additional insertion loss due to a splitter or switch in the active TX path. However, the losses of a switch are mainly caused by the parasitic capacitance and resistance of the switching element which is a transistor. The parasitics of HBT devices are described in Section 3.1 and are reduced by further miniaturization in upcoming HBT technologies resulting in less insertion loss. Lately, a trend in automotive radar towards CMOS technologies is observed which usually offer efficient switch implementation as well.

However, the additional calibration path also consumes additional silicon area which will result in increased costs per die compared to the switch based approach. Especially for systems with additional complexity (i.e. I-Q modulators) in each channel this can be critical. To circumvent this drawback it is also possible to implement an additional calibration path with reduced functionality and output power. For the calibration of the diode based sensors it is sufficient if a small set of power levels can be matched to the according level detector output voltages. Missing points for higher power levels can be calculated assuming a similar characteristic for all diode detectors throughout the IC.

For multi channel transmitters and transceivers it is required to have good isolation between the particular channels. Therefore, the spacing between these channels can not be reduced arbitrarily to save silicon area. If the overall silicon area is dominated by the isolation between the channels, the impact of an additional calibration path inside the IC on the area becomes negligible.

Goal of the new power sensor calibration method is to reduce the margin which is caused by technology drift and mismatch. Using the switch based approach allows to perform a calibration for each channel individually resulting in a calibration per channel. The solution with the additional calibration path reduces the variation compared to the existing state of the art solution as well, but only to a chip-fine level.

When comparing the power consumption of the two proposed solutions there is a slight disadvantage for the switch based approach caused by the permanent RF power loss in form of the additional insertion loss. The additional calibration path consumes a large amount of power in the PA during calibration but afterwards it can be turned to power down mode. Depending on the repetition rate the consumption will increase.

For future applications there are further parameters (i.e. phase) which might require a chip-fine calibration. These additional calibrations could also be handled in the additional calibration path increasing the value of the channel which finally justifies the effort and area.

Chapter 6

Measurement and Verification of different Thermistor Power Sensor Implementations

Previous chapters described the theoretical background required to understand RF power measurements and discussed the different topologies to use an on-chip thermistor in B7HF200 or B11HFC technology. To prove that the proposed calibration concepts work, different test circuitry is designed, layouted and measured. In the following sections the design of test circuits for the most promising approaches is explained in detail. Measurements on four different prototypes are presented and analyzed to show the feasibility of the on-chip thermistor power sensor.

In the first section a robust and straight forward implementation of the power sensor using a Wilkinson splitter is presented. This device is used to collect data on multiple dies in order to investigate process variations of the thermistor throughout a wafer. A product implementation of this concept seems rather unlikely due to already mentioned reasons.

The second part deals with the implementation of an additional calibration path. Therefore a two channel transmitter is modified. One of the channels is used as the calibration channel whereas the other maintains the functionality as a transmit channel.

Sections 6.3 and 6.4 provide detailed information on the switch-based approaches. One solution uses a reverse saturated HBT as switching element whereas the other employs a Gilbert cell based switching quad to redirect the signal between the TX output and the thermistor termination.

6.1 Implementation using a Wilkinson Splitter

This section deals with the design, layout and measurements of an IC which employs the Wilkinson approach. As already mentioned in Section 5.2 this approach uses a passive splitter and therefore has potentially the highest losses of all investigated structures. However, the implementation of this solution is robust and furthermore allows simultaneous monitoring of the TX output and the thermistor termination leading to less complex evaluation steps for verification. With the use of this test device it is shown that the DC power substitution of the thermistor works accurately throughout a whole wafer proofing its feasibility for product applications. The used technology for the presented IC is B11HFC.

6.1.1 Circuit Design

The final goal is to implement the thermistor power sensor in an automotive product environment. Therefore, the designed test IC contains all fundamental building blocks which are relevant to set up a radar TX channel. Figure 6.1 shows the building blocks which are implemented on the MMIC.

A state of the art push push Colpitts VCO is employed for the on-chip signal generation. It provides two outputs for the succeeding stages, one at the fundamental frequency f_0 of around 40 GHz and one at $2f_0$. The VCO provides a tuning range of more than 4 GHz and a phase noise of less than $-98\,\mathrm{dBc} \cdot \mathrm{Hz}^{-1}$ at a 1 MHz offset. The 40 GHz output is directly connected to a programmable CML frequency divider. A divider ratio d_1 of 16, 32 or 64 can be set leading to a signal in the lower GHz range. A succeeding buffer stage restores the signal quality for further processing (i.e. external measurements or Phase Locked Loop (PLL) input). Alternatively, a second divider stage d_2 can be used to further reduce the frequency into the upper kHz range using low power CMOS logic. The flexible divider circuitry allows convenient measurement setups in the laboratory and also for high volume test equipment.

Following the $2f_0$ path in Figure 6.1 leads to a buffer stage which prepares the RF signal for distribution on the IC. The succeeding PA stages are (depending on the device size) in large distance to the VCO output and can therefore not be directly connected to it. The PA consists of two cascode stages and is fully differential. Its output power can be digitally controlled in 64 steps via Serial Peripheral Interface (SPI). The maximum available output power at room temperature is around 12 dBm at 80 GHz. The differ-

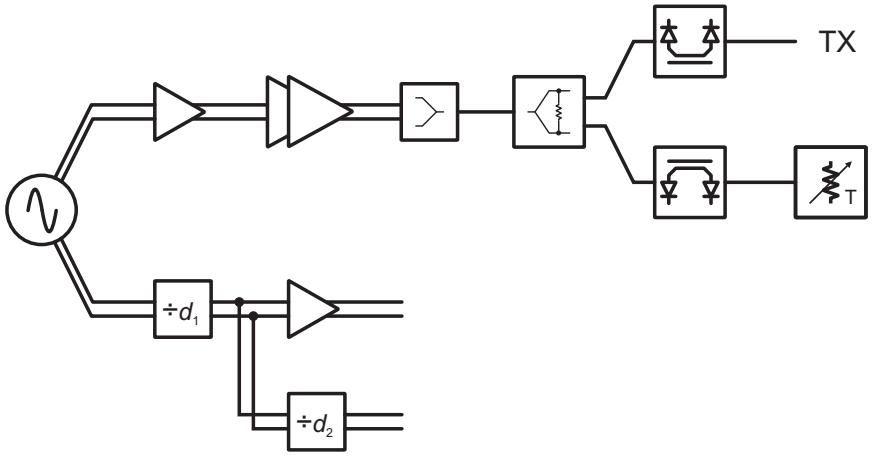


Figure 6.1: Block diagram of the developed IC based on the Wilkinson splitter.

ential output of the PA is converted to a single ended signal using a passive Balanced-Unbalanced (Balun) network offering easier implementation of the following building blocks and a less complex external measurement setup.

To divide the RF signal a Wilkinson splitter is employed using transmission lines and resistive termination as shown in Figure 6.2. In the test device, the output of the Balun is matched to the input impedance of the Wilkinson splitter which is $Z_{\mathrm{L}} = 50\,\Omega$. The transmission lines with the characteristic impedance of $70\,\Omega$ are realized as microstrip lines. However, the suggested metal layers M6 (signal) and M4 (ground) for transmission lines from Section 3.2.2 can not be used as the geometry (given from the metal stack) and design rules do not offer a characteristic impedance of $70\,\Omega$. Therefore, the signal line is kept on the uppermost metal layer (M6) but the ground shield is moved to M2. The differential impedance between the two outputs of the splitter is realized with a TaN resistor of $100\,\Omega$.

The signal paths which are connected to the splitter output contain an identical set of directional coupler and diode based power sensors. One of the outputs is directly connected to a pad which enables on-wafer measurements at the operating frequency of around 80 GHz. The other path is terminated with the proposed thermistor termination for DC substitution. RF signal power and substituted power can be compared. Furthermore, the diode-based sensors can be calibrated with this design.

The complete IC is supplied by 3.3 V and consumes approximately 140 mA if the power amplifier is set to maximum output power. The final layout of the test device is shown in Figure 6.3. It consumes $1448\,\mu\mathrm{m} \times 1448\,\mu\mathrm{m}$ of silicon area including the pads. The power supply is connected to the right

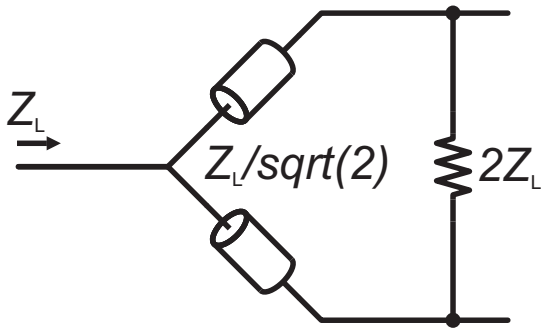


Figure 6.2: Schematic of the Wilkinson splitter.

side of the IC. One of the V_{CC} pads can be used to carry the supply current, the other to sense the voltage on silicon level to eliminate potential voltage drops caused by external wiring or contact resistance. Above the supply pads the SPI interface is located. It consists of four pads which are signal in, signal out, enable and clock. The ground connection can be shared with the neighboring ground pads. Furthermore, the right side contains the divider output pad at the lower end of the IC. The internal divider ratio is set to 32 resulting in a signal frequency of 2.5 GHz at this output.

The tuning voltage for the VCO is applied from the bottom side of the IC. Usually, this voltage is critical for phase noise performance and should have a ground pad and filters nearby to achieve best performance. However, for the thermistor evaluation phase noise is not a critical parameter and therefore the global ground connection can be shared. Left to the tuning pad are the outputs of the diode-based sensor of the channel which is terminated with the RF pad. The sensor voltage is provided as a pseudo-differential signal for forward and reverse direction resulting in a total of four pads.

The upper edge contains the pads for the diode-based sensor outputs of the other channel which is terminated with the thermistor. Furthermore, there are four pads located to perform the 4-wire measurement on the thermistor

The left-hand edge of the IC is the only one which carries the RF signal (around 80 GHz). It is provided with a GSG pad structure which has a pitch of 125 µm between each pad. The additional pad above the GSG structure is a dummy pad for the thermistor termination to have symmetrical load for the two RF paths.

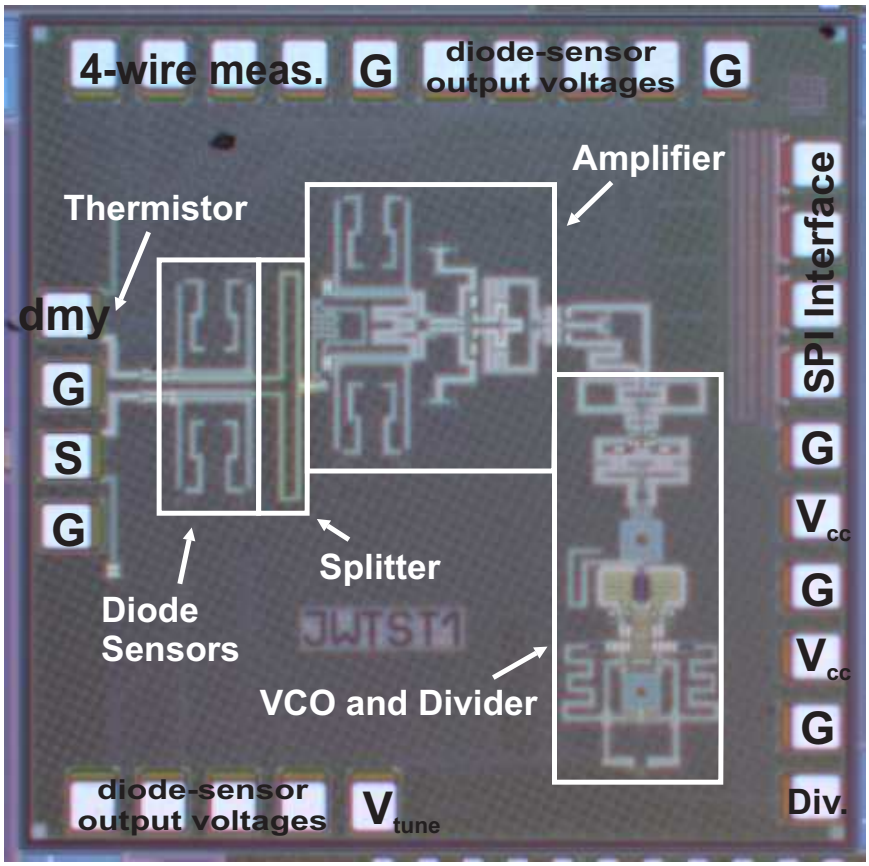


Figure 6.3: Photograph of the developed IC using a Wilkinson splitter.

6.1.2 Measurement Setup and Results

This section covers the measurement setup description as well as detailed measurement results for the developed IC using the Wilkinson splitter. All measurements are carried out as on-wafer measurements. Probing is done using a semi-automatic probe station. The measurements are performed at room temperature and a supply voltage of 3.3 V.

A detailed measurement setup is shown in Figure 6.4. The DUT is simultaneously contacted from all sides using different probe tips. The north and east edge are contacted with multi-contact DC/low-frequency probe tips (10x, pitch of 125 µm). From the south a similar probe tip is used with only 5 tips. For the contact of the GSG structure on the west side a waveguide probe tip for the frequency range from 60 GHz to 90 GHz is used (pitch of 125 µm).

For the 4-wire measurements on the thermistor termination precise current source and voltmeter are used to accurately monitor small changes in resistance. The diode-based sensor outputs in the north and south as well as the supply voltage are monitored with standard Digital Multi Meters (DMMs). A standard voltage source is used to supply the IC with power. Another voltage source is used to tune the frequency of the VCO. The divider output is configured with a divide ratio of 32 which leads to an output signal around 2.5 GHz. The signal is detected with a spectrum analyzer. To modify the registers inside the IC (i.e. to set the PA output power) an SPI is used which is connected to an external adapter. The adapter is controlled using a standard RS-232 interface. The RF signal on the west side is fed to an E-Band (60 GHz to 90 GHz) millimeter wave power sensor head using WR-12 waveguide connectors.

The characteristic in Figure 6.5 shows the thermistor resistance value over applied power. The 4-wire measurement access points of the IC are used to force different currents into the thermistor while accurately monitoring the resistance value. Without any power applied to the thermistor it shows approximately 175 Ω which corresponds to the two resistive elements connected in series for the DC domain in the thermistor termination as already mentioned in Section 4.3. The target value of 200 Ω - which corresponds to an RF termination of 50 Ω - is reached at an input power of around 6 mW. For power levels above 20 mW the resistance exceeds 260 Ω (RF impedance of 65 Ω). In this region the Standing Wave Ratio (SWR) starts to deviate significantly from 1 and therefore the mismatch for the RF signal might already have an impact on the accuracy of the detector.

Furthermore, the graph proofs the linear behavior of resistance over applied power which is expected from Equation 4.10.

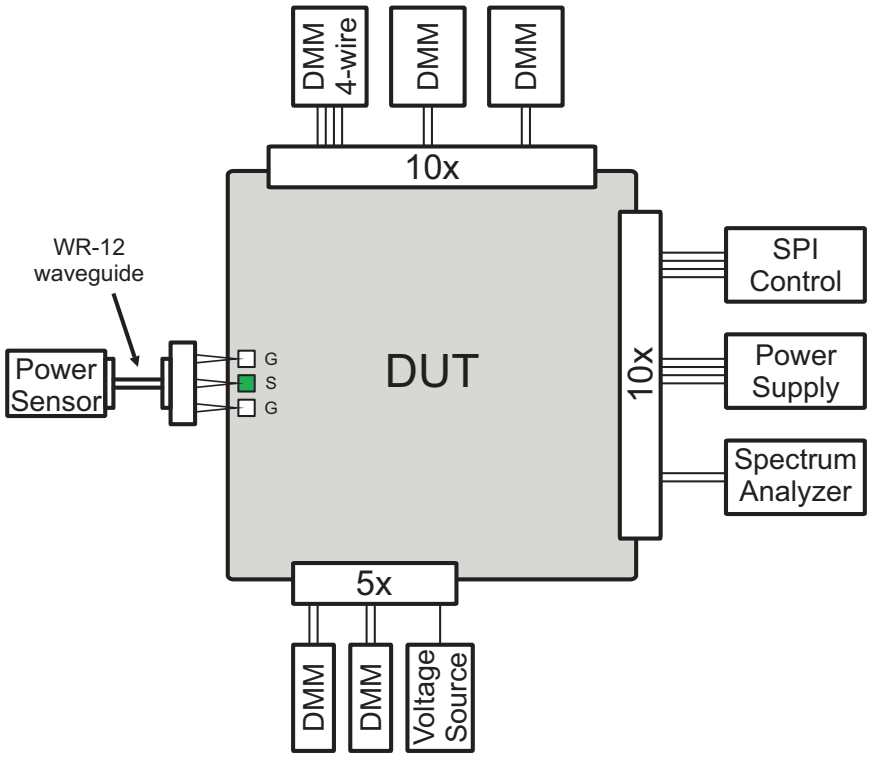


Figure 6.4: Measurement setup for the Wilkinson splitter test IC.

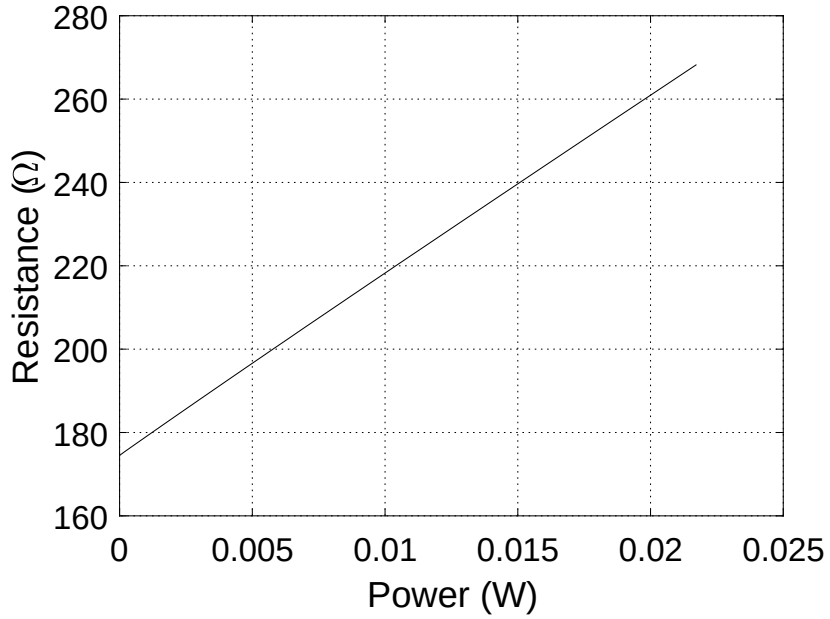


Figure 6.5: Resistance of thermistor termination vs. applied DC power.

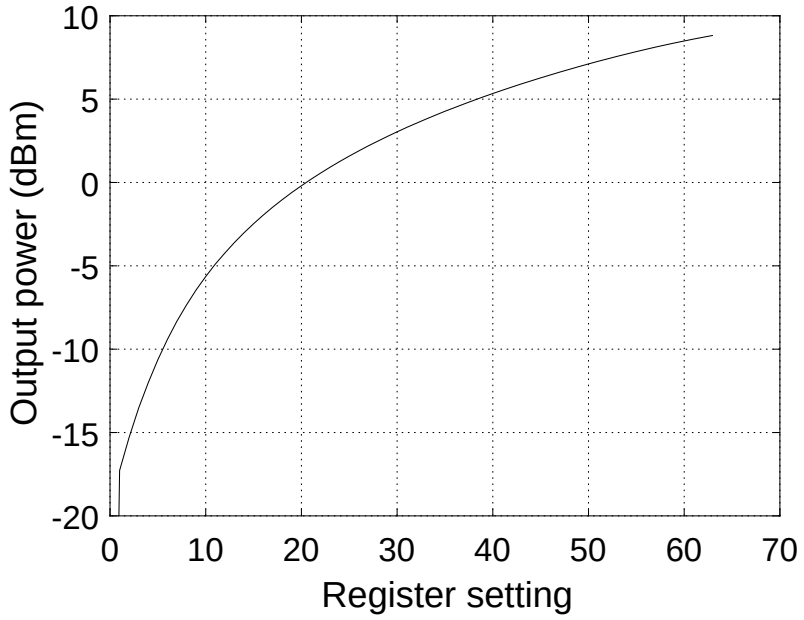


Figure 6.6: RF output power over digital PA setting.

Figure 6.6 shows the RF output power at the TX output over the whole range of digital PA settings. Register value 0 brings the PA in a power down mode which reduces the output power below −50 dBm. Increasing the register values from 1 towards 63 increases the quiescent current in the last PA stage which results in higher output power levels. The maximum output power level for the shown DUT is around 8.8 dBm. A correction factor of 1.5 dB for the GSG waveguide probe tip and the waveguide connection are already included in the shown results.

In the following measurement it is compared how the thermistor termination changes when DC or RF power are applied. The results for the DC response can be taken from the initial resistance measurement where power is applied from an off-chip source. The RF power which is dissipated in the thermistor termination is generated on-chip and therefore not directly accessible. However, the RF output power can be measured using an off-chip power meter. Assuming that the Wilkinson splitter divides the RF signal equally between the output and the thermistor termination a similar characteristic as for the DC response can be created.

Figure 6.7 shows the change of resistance in the thermistor termination if either DC or RF power are applied. Ideally, the response would be identical for DC and RF power. However, the measurement inaccuracy leads to a slight deviation of the two curves. Especially the RF measurement at 80 GHz is

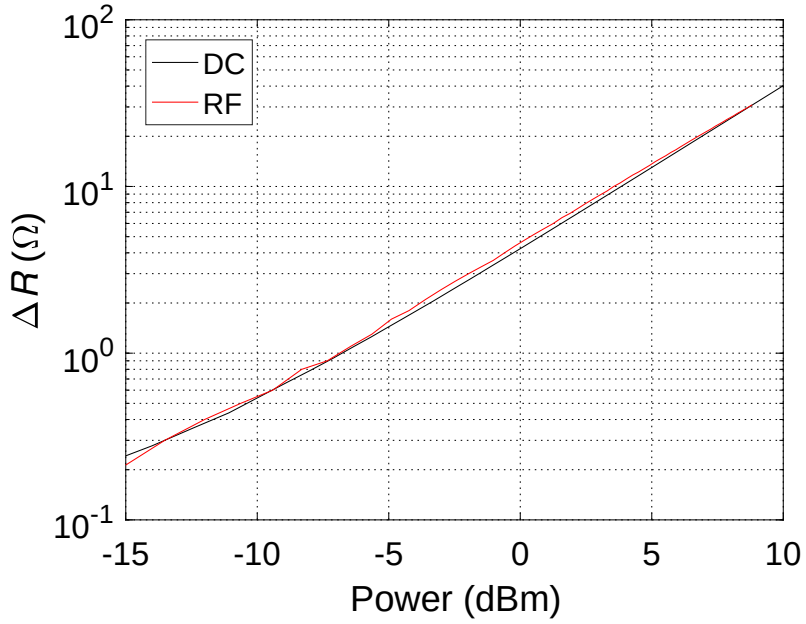


Figure 6.7: Comparison of thermistor termination response on DC and RF power.

challenging. An error of $\pm 0.5\,\mathrm{dB}$ is easily contributed by the power sensor accuracy only.

Nevertheless, the thermistor termination responds fairly similar to DC and RF power. The Wilkinson splitter seems to divide the signal equally onto its two outputs. Furthermore, the correction factor for the power measurement of 1.5 dBm for losses in the waveguide parts also agrees well. Another fact, which is even more important than what has previuously been mentioned, can be gained from the plot. The RF curve shows a linear behavior which leads to the conclusion that the slight mismatch which is introduced by the varying thermistor load is neglectable for the range of applied power levels.

The effect of the output power level on the implemented diode-based detectors is shown in Figure 6.8. In each of the two channels (Ch1 and Ch2) there are two diode sensors available - one for the forward power portion and one for the reverse power. Ch1 is terminated with the RF pad whereas Ch2 contains the thermistor termination. Ideally, the curves would show an identical response in both channels. Due to mismatch between the diode-based sensors a small deviation is observed. The reverse signals are close to zero for the whole power range which indicates good matching for the thermistor termination as well as for the external measurement setup. The

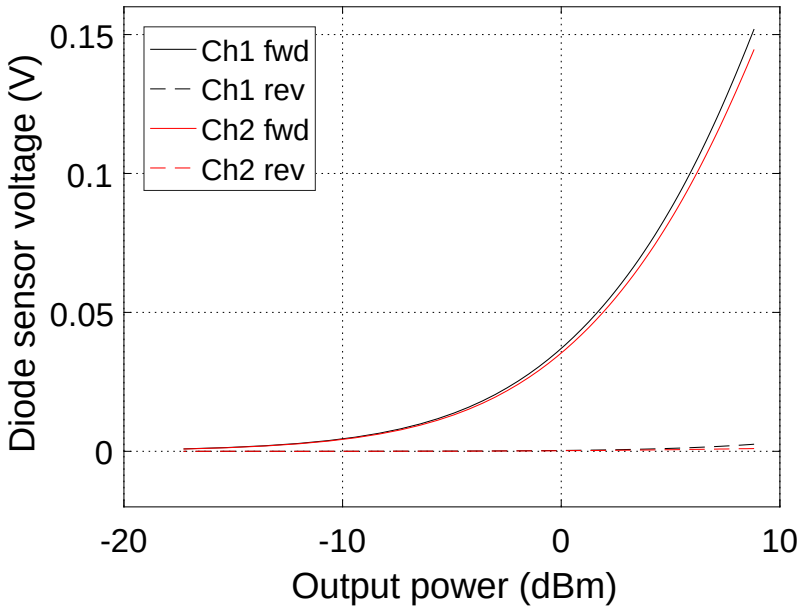


Figure 6.8: Forward and reverse diode sensor voltage for channel 1 and 2 versus TX output power.

voltage for the forward detectors rises up to approximately 150 mV for the maximum available output power at the output of channel 1.

Please note that the differential output voltage of the diode based sensors deviates from 0 even though no RF power is applied. This offset voltage is in the range of ±5 mV and can be measured and corrected by subtracting it from the characteristics aligning the diode sensors at 0 mV when no power is applied. This procedure - which can be described as an offset correction - has also been applied to the shown results.

So far it has been shown that the individual parts of the IC work as expected. In the next step it is evaluated and visualized how well the on-chip thermistor termination estimates the RF power compared to the external measurement setup. As mentioned earlier, the goal is to replace the external RF measurement by the on-chip estimation (using the thermistor). This will enable efficient chip-fine diode sensor and output power characteristics.

In Figure 6.9 it is shown how the externally measured RF output power behaves vs digital control settings as well as how the thermistor DC estimation works. In general it can be observed that the RF measurement and the DC estimation fit well. For the lower power settings the thermistor suffers from insufficient self heating. Therefore, the resistance does not change significantly which results in less accurate measurements. For power level

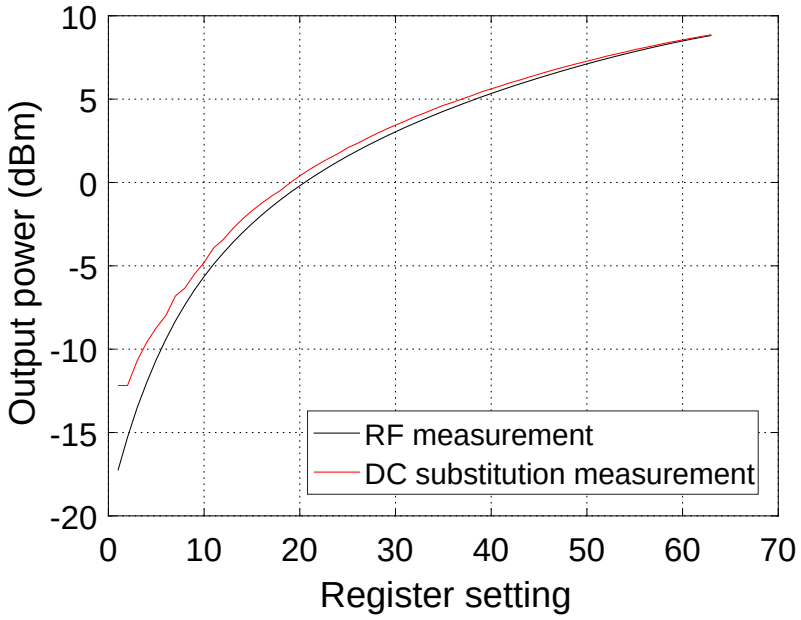


Figure 6.9: Measured RF output power (black) and estimated output power from the on-chip thermistor (red) vs. digital control settings.

settings above 20 this source of error gets smaller.

Figure 6.10 shows the deviation of the DC substitution from the RF measurement in more detail. For power level settings above 20 (corresponding to a power level of 0 dBm) an inaccuracy of less than 1 dB is observed.

Functionality of the on-chip thermistor based power sensor is shown with the previous measurement results. For a product implementation it is important to verify that the circuitry is functional throughout multiple devices on a wafer. Therefore, a semi-automatic probe station is used to repeat the measurements on multiple devices. Figure 6.11 shows which devices are measured on one wafer. A chessboard pattern is used to reduce the measurement time. Samples marked in orange are excluded from further evaluations because the DC parameters indicate that they are not contacted correctly by the automatic test setup. The results gained from the 20 samples which are marked blue are shown in the following.

In Figure 6.12a the RF measurement is compared with the DC substitution for 20 samples. The difference between the lines is plotted in Figure 6.12b. For power level settings above 20 an inaccuracy of less than ± 0.8 dB is observed over the complete wafer.

To visualize the error of the individual DUTs and assign it to a location on the wafer a color coded wafermap is used. Figure 6.13a shows the

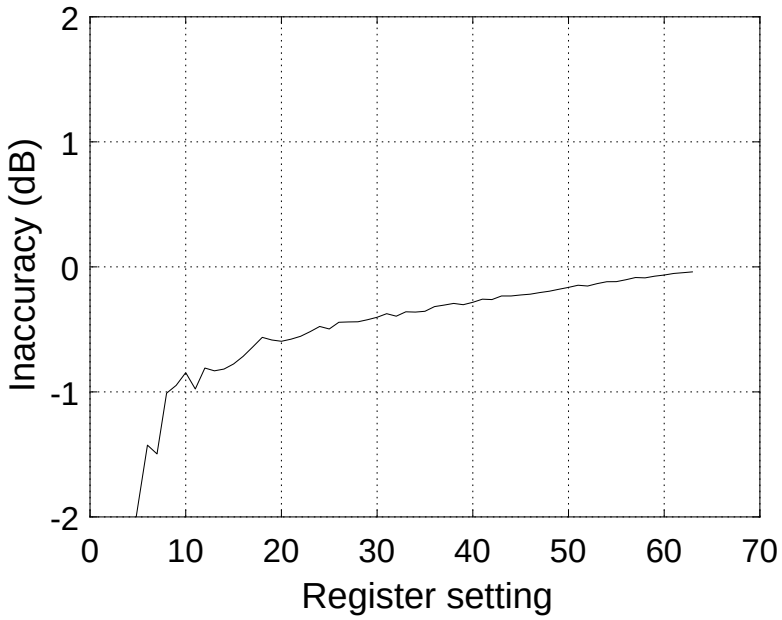


Figure 6.10: Error between the RF measurement and the DC substitution over digital power settings.

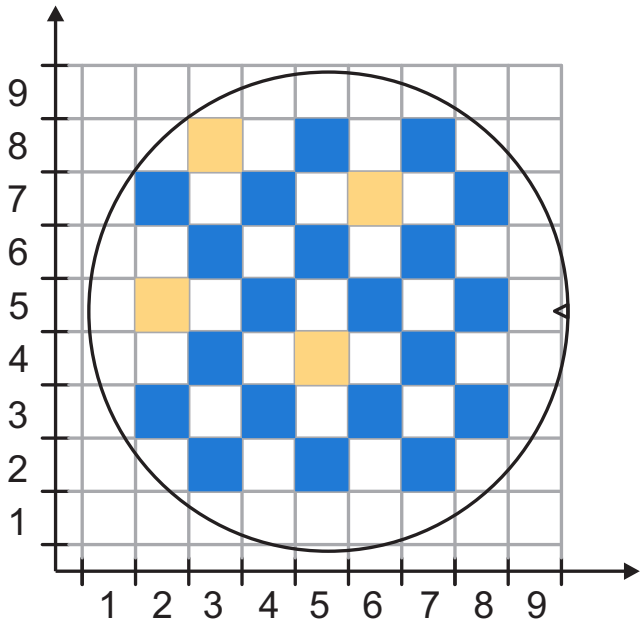
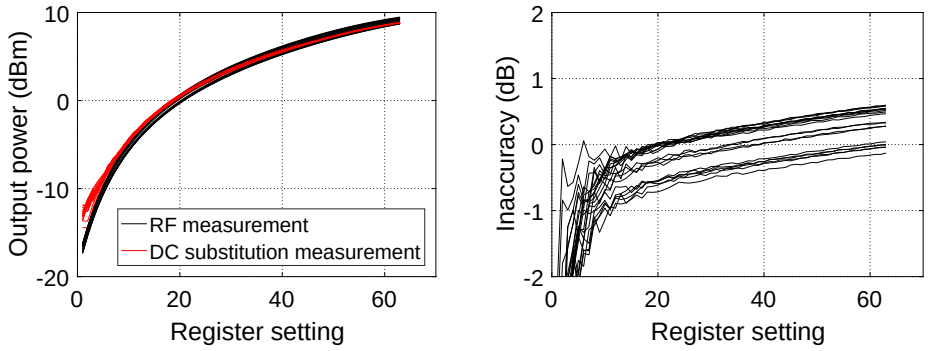


Figure 6.11: Measured devices on the wafer highlighted. Orange devices are not contacted correctly during automated measurements.



(a) (b)

Figure 6.12: RF measurement / DC substitution (a) and inaccuracy (b) over digital power level settings.

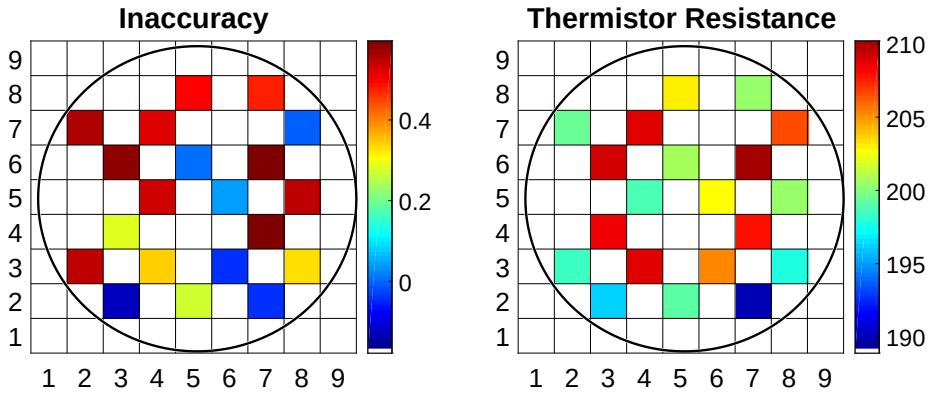
error for the digital control setting 63 from Figure 6.12b on the wafermap. White rectangles do not have any data associated, while measured devices are colored according to the shown legend.

An additional wafermap for the thermistor value is shown in Figure 6.13b. The resistance of the thermistor is shown for the digital power setting 63. For this power level the thermistor termination shows a DC resistance around 200 Ω which corresponds to a termination of 50 Ω for the RF signals (see Section 4.3).

The error on the wafermap does not show a significant or clear dependency of the error on the location. This indicates that the process and manufacturing are homogeneous throughout the wafer. Furthermore, it is observed that the pattern of the two wafermaps do not show similarities which indicates that the two parameters are not correlated. To proof this a scatter plot is shown in Figure 6.14. The plot shows the inaccuracy over the thermistor resistance for register 63. A clear correlation between the two parameters would result in a line of diamond markers. The observed distribution is an accumulation of diamond markers around the mean value which shows that there is no correlation between the parameters. It can be concluded that the variation of the RF termination around 50 Ω does not have a direct impact on the detected inaccuracies.

6.1.3 Conclusion

In this section the implementation of the thermistor power sensor using the Wilkinson-based concept has been presented. For this purpose it has been embedded in a state of the art radar transmitter environment including PA,



(a) (b)

Figure 6.13: Wafermap for (a) inaccuracy and (b) thermistor resistance.

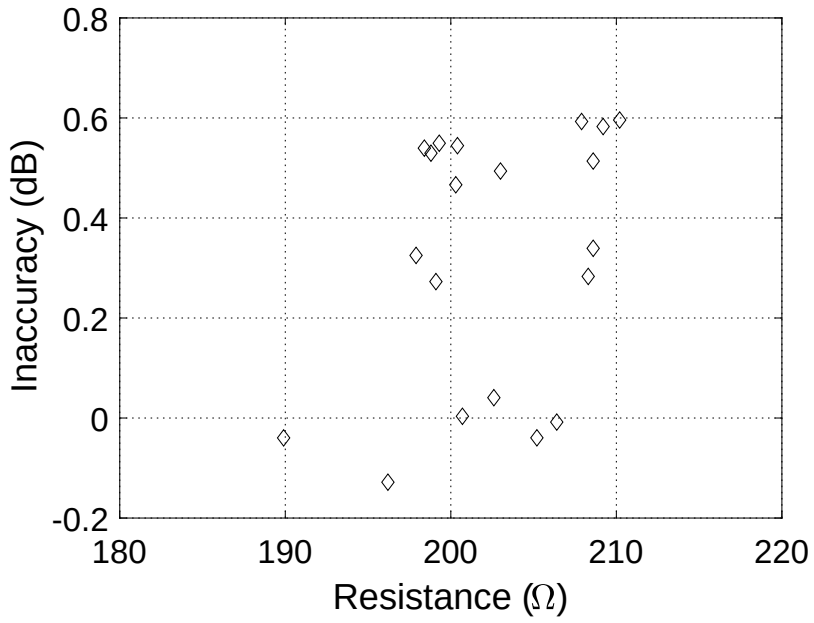


Figure 6.14: Correlation plot between thermistor resistance and inaccuracy.

VCO and additional peripherals. The thermistor behavior for applied DC and RF power has been shown as well as the possibility to calibrate an on-chip diode-based power sensor.

The main goal of the investigations on the Wilkinson-based concept has been to show that the thermistor works reliably over process variation and is a candidate for product implementation. It has been shown that the inaccuracy of the on-chip thermistor power sensor compared to an external RF measurement is smaller than $\pm 1\,\mathrm{dB}$ for the usual operating power levels.

6.2 Implementation using an additional Calibration Path

In this section it is shown how the solution with an additional calibration path - introduced in Section 5.1 - can be implemented. Detailed design considerations and the implementation in the B7HF200 technology are shown as well as the measurement results. The DUT has been also partly presented in [Wursthorn 14].

To verify the performance of the calibration path architecture it is required to have at least two transmit channels on a single IC - one which is used for the application and one which serves as the calibration path. Any additional channel can directly be used for the application without further overhead.

The DUT which is described and evaluated in this section is based on a fully integrated automotive radar transceiver. A block diagram of the original IC is shown in Figure 6.15. The RF part of the device consists of on-chip signal generation using a VCO, a frequency divider chain, an Local Oscillator (LO) signal distribution network as well as four receive and two transmit channels. On the digital domain a control interface is available to adjust for example the output power of the transmit channels. The IC is completed by an analog part which contains a temperature sensor as well as Analog Multiplexers (AMUXs). The Baseband (BB) part of the receiver is not implemented on the IC, therefore four differential analog outputs (IF+/-) provide the according signals to a dedicated BB unit.

The picture in Figure 6.16 shows the RF PCB of an automotive radar module. The presented radar IC is locate in the center of the module. In this example bond wires are used to connect the RF ports of the IC to the transmission lines on the PCB. It can be observed that the four RX channels are routed separately to the antenna feeding points whereas the two TX channels are combined on the PCB and the fed to the antenna.

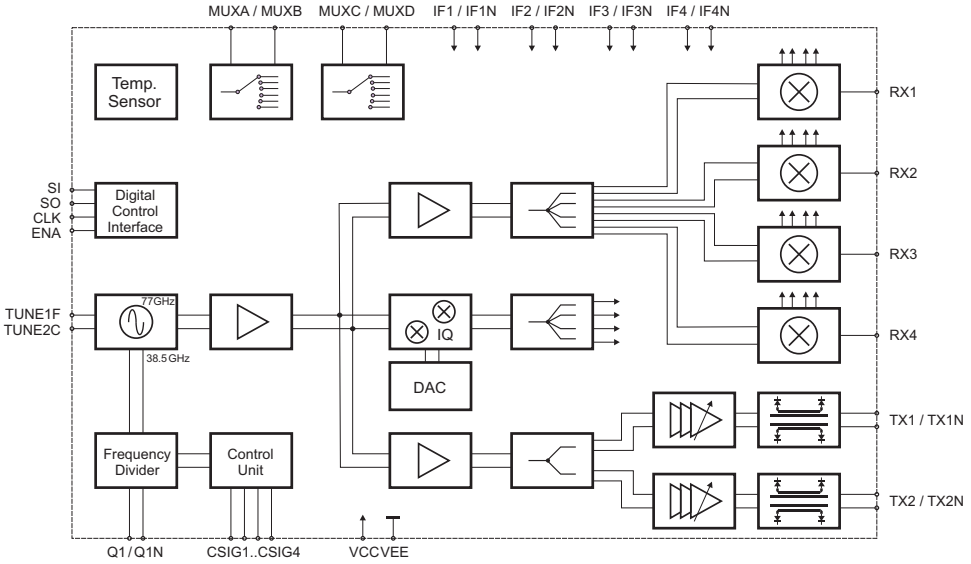


Figure 6.15: Block diagram of the automotive radar transceiver which serves as the basis for the DUT.

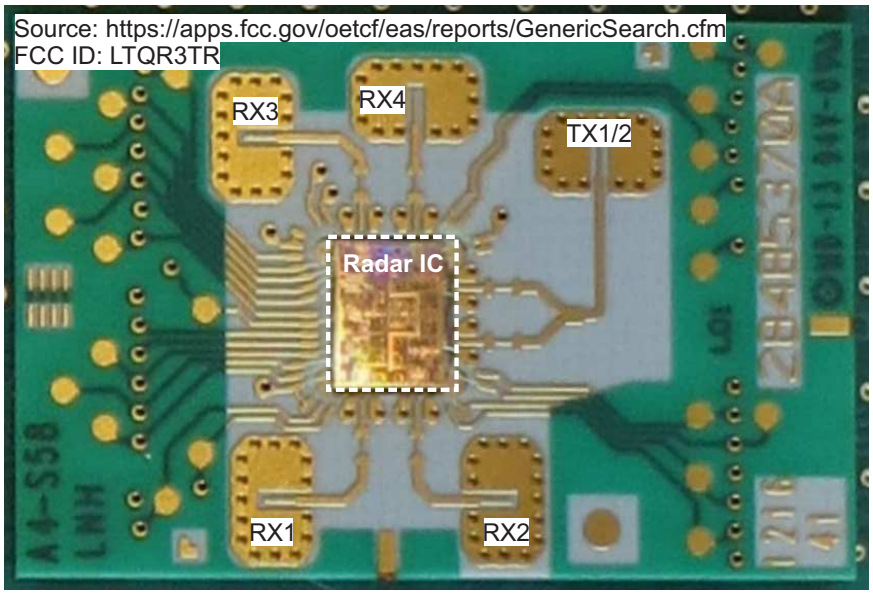


Figure 6.16: Micro photograph of an automotive radar module using the presented radar IC.

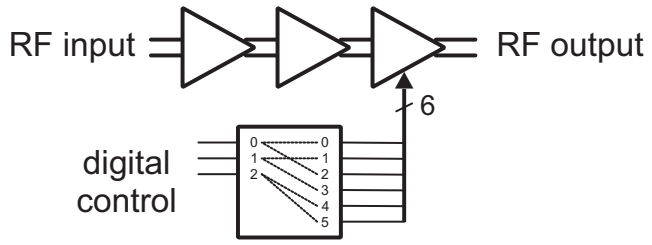


Figure 6.17: Block diagram of the 3-stage power amplifier including the digital control options.

A closer look at the transmit part in Figure 6.15 reveals that the PA consists of three stages where the last one offers adjustability. This part of the transmitter is of interest for the thermistor investigations as the power levels which can be applied to the termination are defined by the PA settings. Figure 6.17 shows a detailed block diagram of the 3-stage amplifier and the control options. Stage 1 and stage 2 are gain stages without control mechanisms except for a power down mode. The third stage however offers six bits for digital control of the output power. As indicated in the figure these bits are controlling the current in the last PA stage and accordingly the output power level. Furthermore, the six bits have a binary weighting where bit 0 has the least and bit 5 has the most impact. Due to limitations in the digital part of the transceiver only three bits are available to control the PA. In Figure 6.17 it is shown how the six available bits are mapped to the three available register bits. This mapping results in a reduced set of eight combinations that are available for the output power control. Furthermore, because of the weighting the lowest bit has just a minor impact on the output power, which does not cause sufficient change in the thermistor resistance. Therefore, the only useful power sweep combinations are derived from bit 1 and 2 resulting in four sigificant output power steps to investigate the thermistor behavior.

The previously described transceiver IC needs some modifications to evaluate the thermistor calibration path architecture. More precisely, one channel remains in its original condition whereas the other is terminated with the thermistor termination.

In general, the solution with the additional calibration path potentially requires more area compared to a switch-based solution (shown in Section 5.2). However, this solution does not suffer from additional losses caused by a switching element in the transmit path. Furthermore, the thermistor termination monitoring and the external RF measurement can be done simultaneously leading to reduced effort in verification.

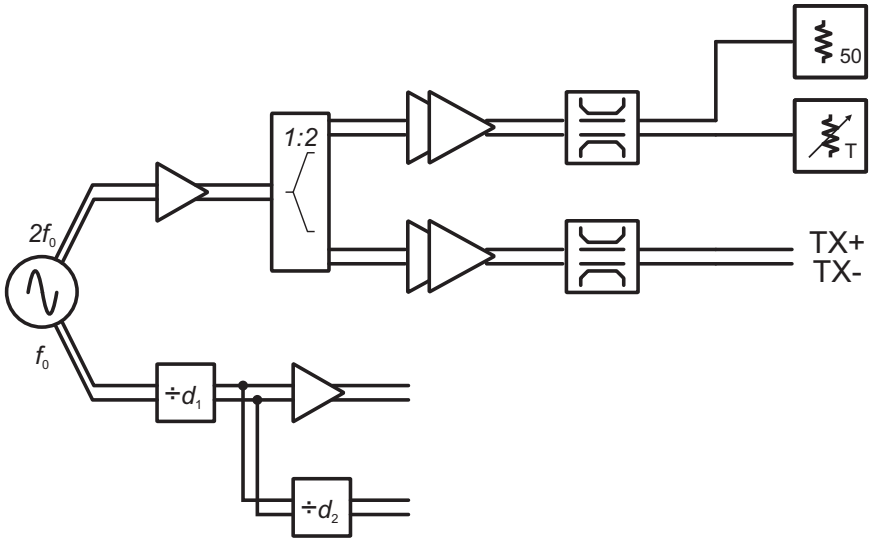


Figure 6.18: Block diagram of the transmit part of the modified transceiver IC.

6.2.1 Circuit Design

The device presented in this section will show how the thermistor works in an additional calibration path. The DUT contains all fundamental building blocks which are required for an automotive radar transceiver. However, for the verification of the thermistor termination only the transmit part is of interest. Figure 6.18 shows a simplified block diagram of the transmit part of the DUT including the modifications at the output of one of the channels.

On-chip signal generation is accomplished using a VCO in push-push topology. The output signal with f_0 of around 40 GHz is connected to a programmable frequency divider d_1 with a ratio range between 8 and 32 resulting in output frequencies convenient for laboratory measurement setups or PLL implementation. Therefore this signal is buffered and then directly provided at an output pad for further use. Furthermore, this is signal is also fed to another divider d_2 which further reduces the frequency to values between 200 kHz and 25 kHz. This output is not directly accessible but only via a chain of AMUXs. It can be used to verify the operating frequency during production test where only equipment with limited performance is available.

The signal branch with $2f_0$ is buffered and then distributed to the two transmit channels using a highly symmetric, passive 1:2 divider structure. Each of the two transmit channels consists of a three stage PA in cascode topology. The tail current source of the last stage draws approximately

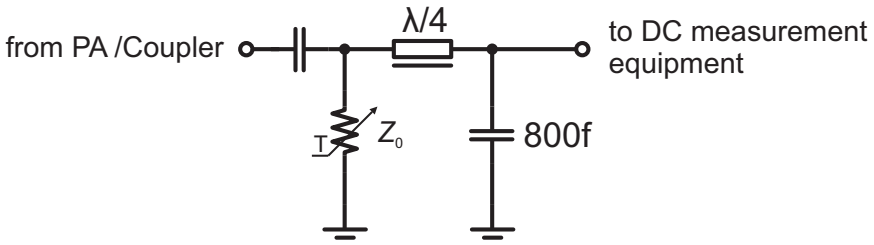


Figure 6.19: Schematic of the implemented thermistor termination.

100 mA from a 3.3-volts power supply. This current can be digitally reduced in four steps to adjust the RF power level at the transmitter output.

The PA is followed by a directional coupler which is connected to each of the differential transmit signals. The ports on the secondary side of the directional coupler are terminated with diode-based power sensors (which are not shown in the Figure) allowing to distinguish between forward and reverse traveling signal power.

The difference between the two transmit channels is in how they are terminated. While the differential signal of channel 1 is connected to a Ground-Signal-Ground-Signal-Ground (GSGSG) pad configuration (TX+, TX-), the other channel is terminated with the thermistor termination. To be precise, one part of the differential signal is connected to the thermistor while the other is at a fix load of 50 Ω. Ideally, this will split the available output power into two equal parts. Alternatively, the thermistor can also be connected differentially between the two RF outputs.

This setup allows to do an external RF power measurement while at the same time monitoring the thermistor behavior. Ideally, the two measurement possibilities will result in identical results. However, this has to be proven.

In Figure 6.19 it is shown in detail how the thermistor termination is implemented. The MIM capacitor creates a short in terms of RF on the right side of the quarter-wave transmission line. This short is transformed into a high impendance seen into the transmission line. This leads to the fact that the RF signal coming from the PA/Coupler sees an impedance which is dominated by the thermistor value. This thermistor is designed to be around 50 Ω. The change in resistance of the thermistor can be easily measured with external equipment through the transmission line.

Figure 6.20 shows a photograph of the bottom-right corner of the IC where the thermistor is implemented. On the bottom edge it is observed that two of the pads are missing in the regular pad pattern. These pads are removed and replaced by the thermistor and a termination of 50 Ω. The thermistor termination can be recognized by the folded quarter-wave transmission line

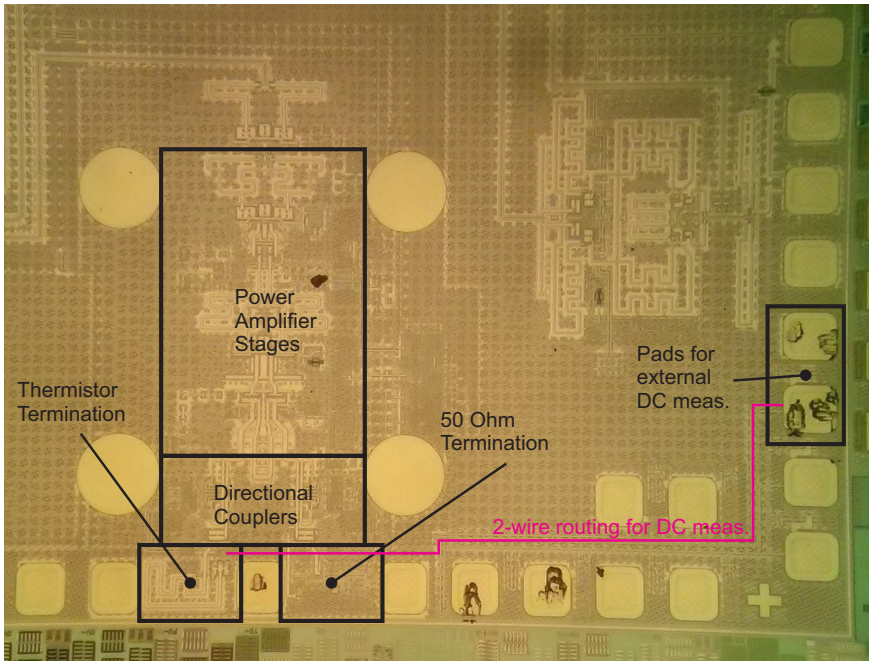


Figure 6.20: Photograph shows the area of the IC where the thermistor is implemented.

whereas the termination can not be seen from this level of zoom. The pads for the external DC measurement should ideally be close by. However, the existing padframe does not allow a simple implementation close by. Therefore, the measurement pads are located on the right edge. This results in a line length which is in terms of ohmic losses not neglectable and potentially leads to voltage drop and measurement error.

6.2.2 Measurement Setup and Results

This section deals with the measurement setup and results of the thermistor implementation using an additional calibration path. All measurements are executed as on-wafer measurements at room temperature on a manual probe station. The supply voltage for the DUT for all measurements is 3.3 V.

Figure 6.21 shows a detailed block diagram of the measurement setup. Connections from all four sides are required to perform the measurements. The left side of the IC is used to connect the 3.3-volts power supply. Therefore, a probe tip with four needles is used (2xVdd, 2xGND, pitch of 125 µm). On the top edge of the device, another DC/low-frequency probe tip with a pitch of 125 µm is connected to the device.

Two of the eight available needles are used to monitor the frequency

divider output with a spectrum analyzer. The internal frequency divider is configured to have a divide ratio of 32 resulting in a frequency around 1.25 GHz. Another two needles on the top side are connected to a low-noise voltage source. This voltage is used to control the VCO frequency. The VCO is tuned to oscillate at 80 GHz for all of the measurements. The remaining four needles are connected to the SPI interface. An external SPI controller is used to modify the internal registers to for example change the output power level of the transmit channels.

The right side of the device is used to monitor the change in resistance of the thermistor. Therefore, a probe tip with two needles is mounted (pitch of 125 µm). Unfortunately, there is no possibility to perform the measurement in a 4-wire configuration as would be preferred. The reason for that is that only a limited number of pads were available in the original pad frame of the automotive transceiver IC.

The two RF transmit outputs (TX1 and TX2) are located on the bottom of the IC. TX1 is in its original state, TX2 is the modified channel. For the measurement setup the bottom edge is the only one which is connected to external RF measurement equipment. A waveguide probe tip with a pitch of 125 µm in GSGSG configuration is used connect the output of TX1. A straight WR-12 waveguide section connects the probe tip to the power sensor head. As mentioned earlier, the signal pads of TX2 have been replaced by the thermistor termination.

In Figure 6.22 it is shown how the resistance of the thermistor changes if power is applied to it. The blue curve is obtained from a DC measurement. Therefor, an external current is fed to the terminstor termination to heat up the device while the voltage drop is monitored. The red circles represent the thermistor behavior caused by RF power which is dissipated in the device. The four measurements points are gained from the different PA settings mentioned earlier in this section.

It is observed that for applied power levels below −10 dBm the thermistor value gained from the RF measurement agrees well with the DC curve. Furthermore, the plot shows that the thermistor resistance for low power levels is almost at the target value of 50 Ω. For higher power levels the resistance of the thermistor termination increases as expected. For a DC power of 12 dBm the resistance is approximately 64 Ω. For applied RF power a similar trend is observed. The deviation between the two curves can be explained by measurement inaccuracies at 80 GHz and the unsymmetrical loading of the differential transmit channels.

The distance in x direction between the red circles and the blue line is the difference between the RF measurement and the DC estimation. Figure 6.23 shows exactly this difference for the available RF power level settings which is

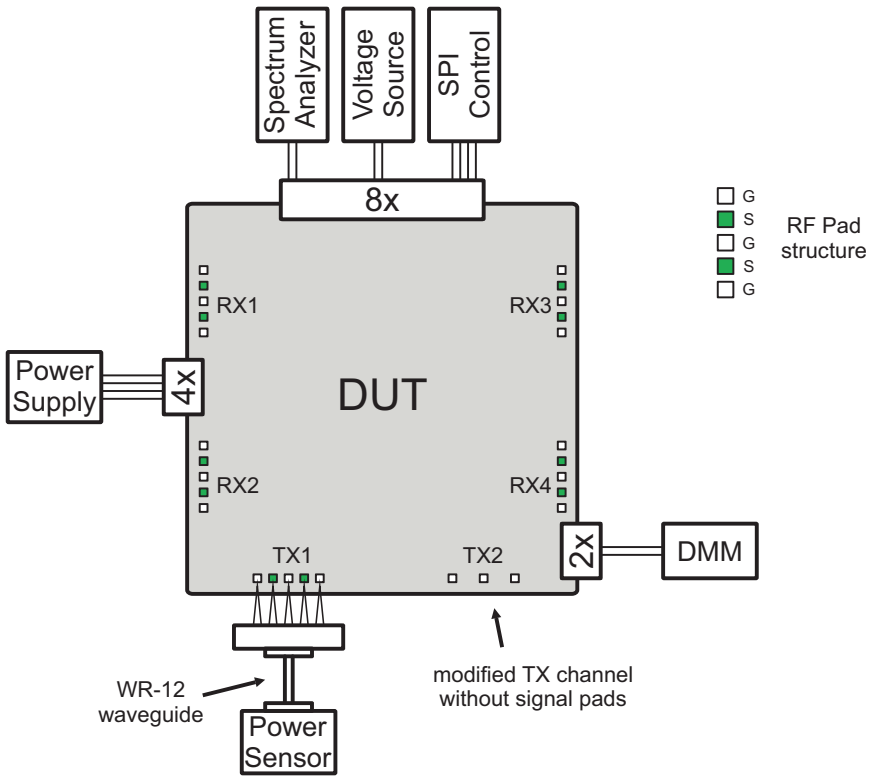


Figure 6.21: Block diagram of the used measurement setup.

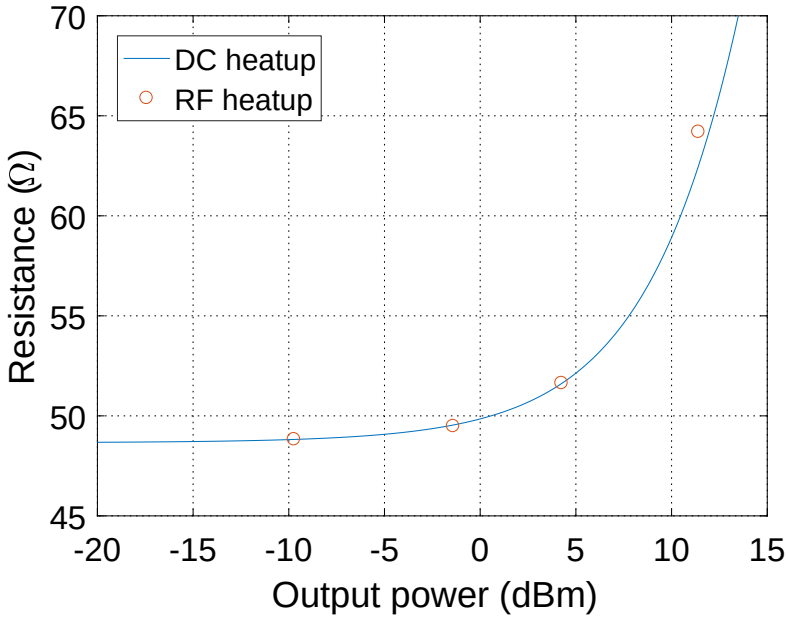


Figure 6.22: Thermistor resistance change over applied DC and RF power.

considered as the inaccuracy of the thermistor power detector. It is observed that the thermistor is able to estimate the available RF power level with less than ±0.55 dB error by using only DC measurement equipment.

6.2.3 Conclusion

In this section it was shown how the thermistor using the additional calibration path architecture can be implemented in a product-like MMIC. The transmit channel of an existing automotive radar transceiver is modified and terminated with the thermistor. The presented implementation principle is closely related to patents [Kammerer 19], [Wursthorn 18] and [Knapp 17] which are granted in the United States and similar to what is shown in [Wursthorn 14].

The presented results show that the thermistor termination is able to estimate the RF power level at the transmit output with less than ±0.55 dB of error over the relevant power range by using DC measurement equipment only. This is a good prerequisite for product integration as it allows the straight forward usage of Automatic Test Equipment (ATE) which is much appreciated for high volume production.

For the future it is expected that the accuracy of the thermistor power detector can be further increased by enabling 4-wire measurement and a

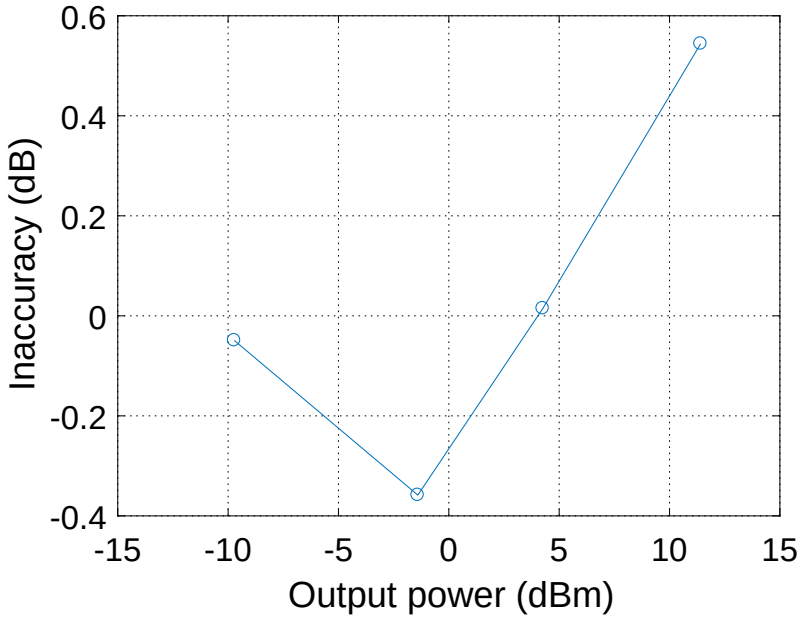


Figure 6.23: Difference between the RF measurement and the DC estimation versus power level.

more robust termination principle like shown in Section 4.3. Furthermore, the termination and measurement of the differential RF signal in the transmit channels needs to be done symmetrical. Alternatively, a Balun network can be implemented on the IC to reduce measurement complexity.

6.3 Implementation using an SPDT Switch

Ideally, the thermistor based power detector is implemented with little effect on the transmit channels and low area overhead. The previously discussed solutions which are using the Wilkinson splitter or an additional calibration path are violating at least one of the mentioned targets.

The most intuitive way to implement the thermistor termination under the mentioned constraints is to use a switch to guide the RF power either to the transmit output or the thermistor termination as already shown in Section 5.2. Unfortunately, the design of a switch with low insertion loss and good isolation at around 80 GHz is limited by the parasitic capacitance and series resistance of the switching elements offered by the technology. To be more precise, the capacitance in off state (C_{off}) and the resistance in on state (R_{on}) can not be optimized at the same time. For a series switch this means

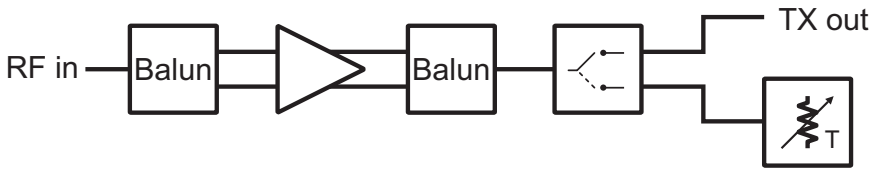


Figure 6.24: Block diagram of the DUT which uses the SPDT switch-based thermistor implementation.

that the insertion loss reduces if the transistor size is increased but at the same time the isolation suffers due to larger C_{off}. The product of C_{off} and R_{on} is a technology constant for a given type of switch which can be used to compare the performance of different technologies.

In this section it is shown how a Single Pole Double Throw (SPDT) switch can be used to implement the thermistor power detector using the B11HFC technology. There will be a detailed design description of the switch and the transmit part as well as an insight on the RF measurement setup and results.

6.3.1 Circuit Design

The circuitry which is presented in this section deals with the thermistor implementation using an SPDT switch. In Figure 6.24 it is shown which building blocks are part or the DUT. The RF input signal is applied to the first Balun network from an external signal source. The differential Balun output is fed to a cascode amplifier stage. Afterwards, another Balun provides the signal to the SPDT switch. Depending on the switch position the signal either enters the transmit path which is terminated by a pad (TXout) to perform external RF power measurements or the path which is terminated with the thermistor.

The Baluns are realized using a lumped element approach as described in [Bakalski 02]. The required capacitors are realized as MIM capacitors whereas the required inductances are replaced by transmission lines. Using Baluns simplifies the measurement setup considerably as only single-ended signals need to be measured.

The buffer stage between the Baluns is implemented in cascode topology. A detailed schematic view of the block is shown in Figure 6.25. Voltage biasing networks are not shown for simplicity reasons.

The RF input signal is applied to a common emitter stage represented by transistors T_{1a} and T_{1b}. The collectors of the common emitter stage are connected to the common base stage through transmission lines TL_{1a} and TL_{1b}. These transmission lines do have inductive behavior to partly compensate the

capacitance seen at the collectors of T_{1a} and T_{1b}. The inductance and capacitance are designed to be in resonance at the target frequency. The common base stage consists of transistors T_{2a} and T_{2b}. The base node between the two transistors is critical for unwanted oscillation. Therefore, the distance between the two base terminals is minimized to reduce inductive behavior. Furthermore, a small silicided polysilicon resistor is used in common mode to achieve additional damping.

The output of the common base stage needs to be matched to the succeeding building block to ensure maximum power transfer. Transmission lines TL_{2x} and TL_{3x} are used to accomplish the matching. Furthermore, they are supplying the transistors with current from a 3.3-volts power supply.

The tail current source consists of transistors T_{3a} and T_{3b} defines the DC current which is drawn from the power supply. In this example the reference current is set to 10 mA and the mirror ratio is 6 resulting in a current of 60 mA in the amplifier stage.

In total, the cascode stage achieves a small signal gain of >14 dB at a maximum saturated output power of >17.5 dBm. The peak Power Added Efficiency (PAE) of the stage is 16 % at an output power of 17 dBm. More measurement and design details on the behavior of the cascode stage are presented in [Wursthorn 16].

Note, as this DUT contains only one cascode gain stage the external signal source might not be able to drive the amplifier into deep saturation. However, this does not have any negative impact on the evaluation of the thermistor behavior.

In Figure 6.26 it is shown how the SPDT for 80 GHz is implemented. The RF input signals which is provided by the amplifier stage is fed to the switch from the left. At the node T it is the target that one of the branches provides a high impedance whereas the other impedance should provide good matching to the system impedance. In this example the system impedance at the two RF outputs is 50 Ω for the target frequency.

Let us consider that V_{B1} is at 2 V which results in a low impedance between the collector and emitter terminal of transistor T_1. This creates a short circuit for the RF signal. The RF short is transformed by the $\lambda/4$ transmission line providing an open at node T looking into branch 1. The inductance L_1 which is in parallel to the transistor T_1 does not have any impact on the behavior in this configuration.

While V_{B1} is at 2 V we consider now that V_{B2} is at 0 V. This means that the transistor T_2 shows a high impedance between the collector and the emitter node. This impedance however is limited by the parasitic capacitance seen from the emitter node towards ground. To prevent RF signals from leaking through towards ground at this node the parasitic capacitance is

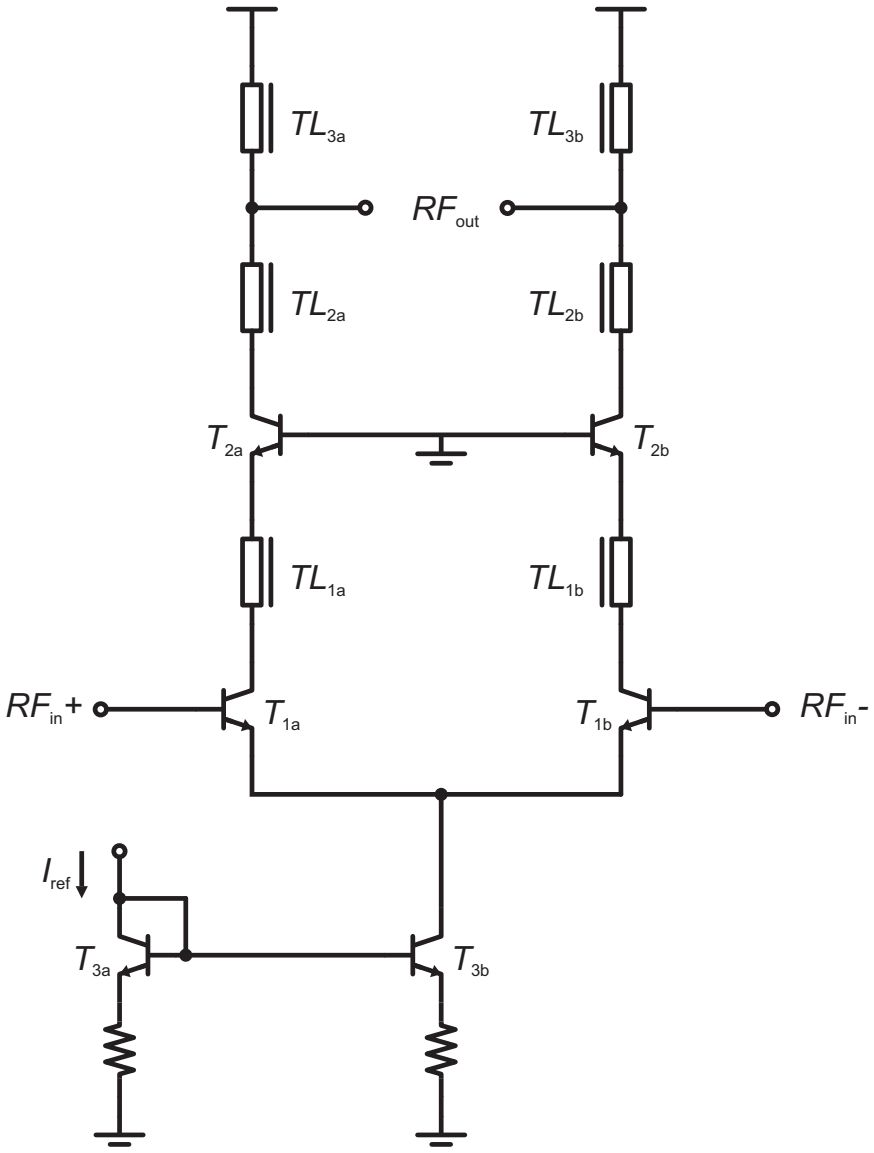


Figure 6.25: Schematic view of the buffer stage.

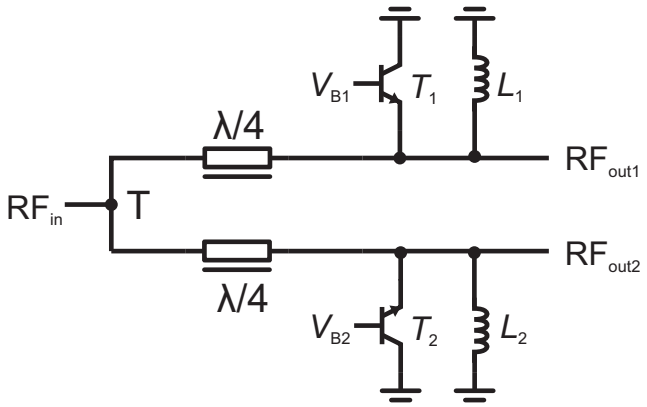


Figure 6.26: Schematic view of the SPDT switch.

compensated by a parallel inductance L_2. L_2 is designed to be in resonance with the capacitance in the target frequency range. For flexibility L_2 is implemented as an inductive stub with multiple grounded taps along the line. This allows to adjust the effective length of the line after IC manufacturing by cutting some of the grounded taps with a laser.

In contrast to the conventional common emitter configuration, the emitter nodes in this circuit are connected to the RF signal lines while usually the emitter is connected to ground. In literature this operating mode for a transistor is often referred to as reverse saturated regime. The advantage of this configuration is that the parasitic capacitance of the emitter towards ground is smaller than for the collector. The reason for this lies in the technology itself and can be understood when looking at the transistor cross section in Figure 3.2 (Section 3.1). From there it can be observed that the emitter is isolated from the substrate by the collector and base regions. On the other hand the buried layer which connects the active collector region to the collector contact creates a pn junction towards the substrate, resulting in a larger capacitance towards ground. Further design considerations on reverse saturated HBTs can be found in [Schmid 14].

To investigate the performance of the reverse saturated HBT in detail a stand-alone version of this switch is implemented in addition to the complete DUT. In Figure 6.27 it is shown how the SPDT switch behaves for frequencies around 80 GHz. The small-signal S-parameters show a minimum insertion loss of around 2.7 dB at the target frequency. Furthermore, an isolation of around 20 dB is observed. The performance is expected to improve if a fixed stub length is used instead of a fuse-based approach.

In Figure 6.28 it is shown how the thermistor termination is implemented on the DUT (see also Section 4.3). The RF signal coming from the SPDT

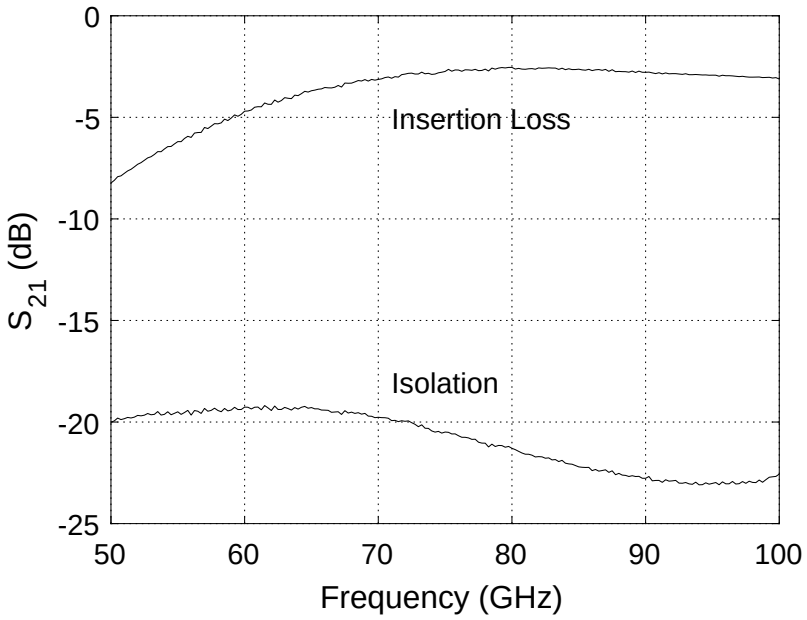


Figure 6.27: S-parameter measurement results of the stand-alone SPDT switch.

output enters the circuit on the top left through an AC coupling capacitor. The signal faces an impedance Z_0 which is created by two thermistors in parallel having $2\,Z_0$ each. The resistance change of the thermistors is monitored by DC measurement equipment through resistors of $1\,\mathrm{k}\Omega$. For monitoring, the resistance could also be increased but the DC substitution current has to be applied through this path as well and the voltage drop needs to be in a reasonable range.

A micro photograph of the $1.3\,\mathrm{mm} \times 1.3\,\mathrm{mm}$ DUT is shown in Figure 6.29. The RF signal is fed from the left through a GSG pad structure. Directly next to the input pad is the Balun network which provides the differential signal to the amplifier stage. Another Balun network afterwards provides the amplified, single-ended signal to the SPDT switch. Node T is the splitting point for the two branches of the switch and therefore the starting point of the $\lambda/4$ transmission lines. The switching elements are located at the end of the transmission lines. The inductive stubs to compensate the parasitic capacitance are placed between the two branches. Each of the inductive stubs has a set of 5 laser fuses for post process trimming. The lines running next to the $\lambda/4$ lines are used to isolate the base biasing connection of the circuit from the RF part. Furthermore, it is observed that the upper branch is terminated with the GSG pad on the right edge of the device whereas the lower branch

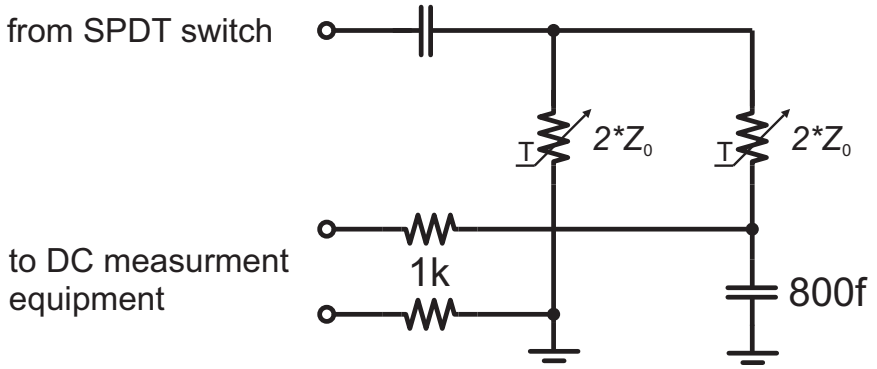


Figure 6.28: Schematic view of the thermistor termination.

ends at the thermistor which itself consumes only 75 µm × 60 µm.

On the south edge of the IC four pads are reserved to perform the 4-wire resistance measurement of the thermistor. In addition two ground pads and a 3.3-volts power supply pad (V_{CC}) are located on this edge.

The north edge of the device is also occupied by DC pads. The pad row starts on the left with two additional ground pads and a power supply. Next are two pads for PA bias voltages which can be left open for the default biasing setting. The last four pads in this row are used to set the base bias voltage V_{B1} and V_{B2} for the switches.

To achieve a more compact layout, the $\lambda/4$ transmission lines can be folded multiple times.

6.3.2 Measurement Setup and Results

In the following it is explained in detail how the measurement setup looks like and how the DUT is connected. All of the measurements are taken at room temperature and on wafer level using a manual probe station. Furthermore, the measurement results are shown and discussed with respect to advantages and drawbacks of the switch-based implementation of the thermistor.

A block diagram of the measurement setup is shown in Figure 6.30. The DUT is contacted from all sides using probe tips with a pitch of 125 µm. On the left side a signal generator feeds the RF signal through a GSG E-Band waveguide probe tip to the input of the device. A similar probe tip is used on the right side to connect the output signal with the external power sensor. This connection is also done via waveguide.

The lower edge of the device is connected with a 7x DC probe tip. A digital multimeter is used to perform the 4-wire measurement of the thermistor. Note, for the DC substitution measurements the forcing lines of the

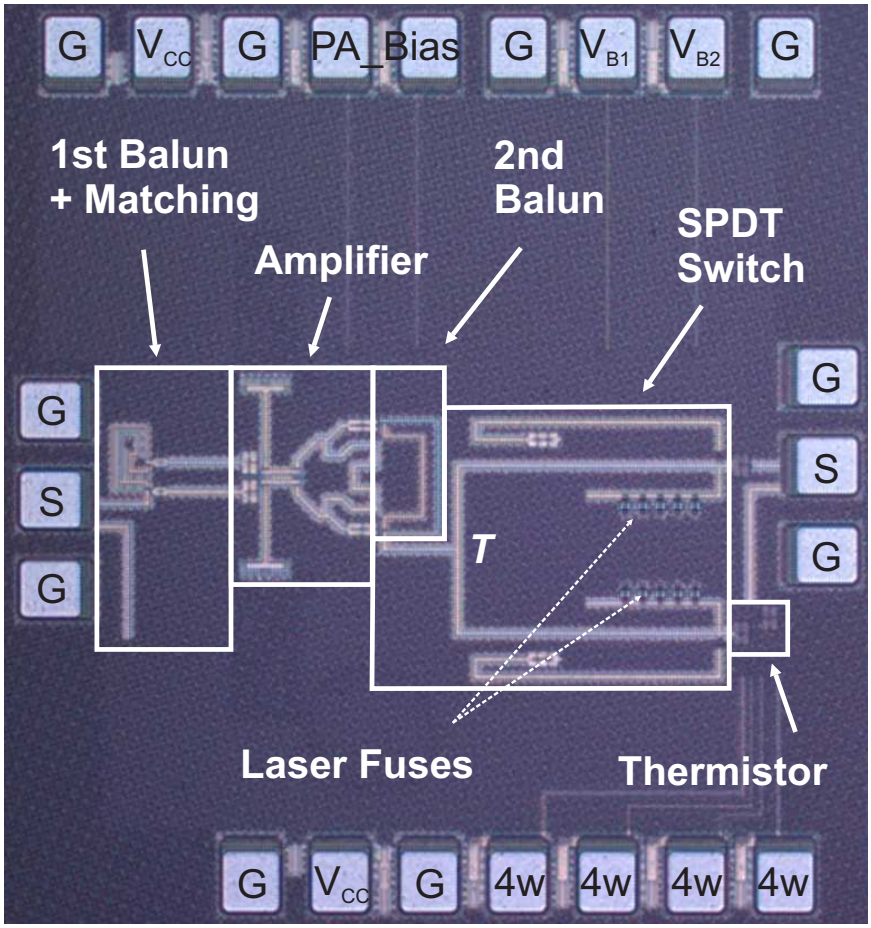


Figure 6.29: Photograph of the presented DUT using the SPDT switch.

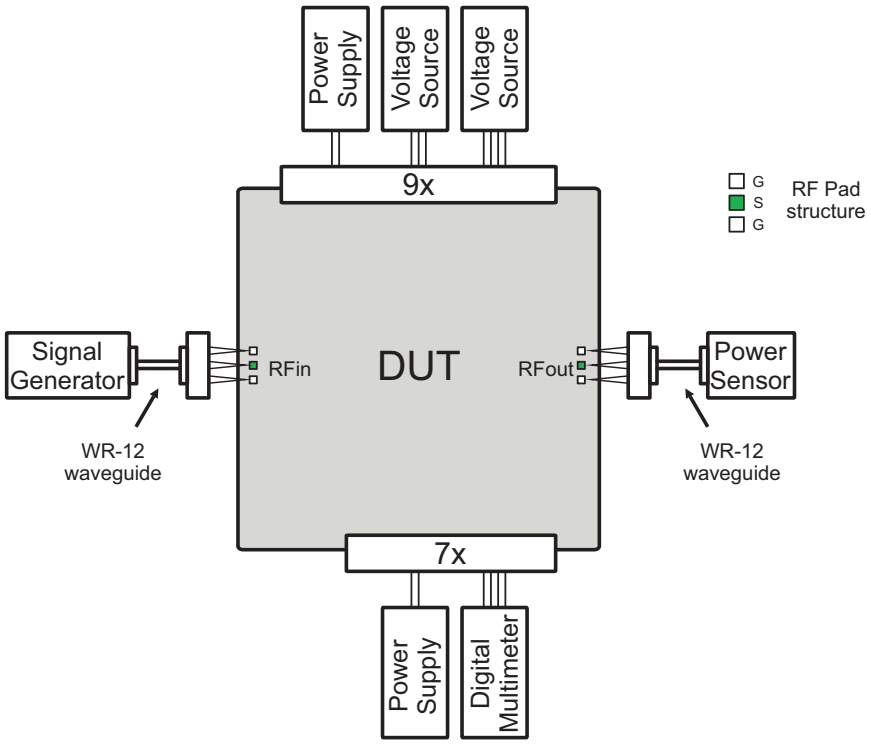


Figure 6.30: Measurement setup for the thermistor SPDT switch implementation.

4-wire setup are used to increase the current in various steps. Furthermore, a power supply is providing the required supply current from 3.3 V.

On the upper edge a DC probe tip with 9 needles is used for further biasing. An additional 3.3-volts power supply is connected there which can alternatively be used to sense the on-chip supply voltage to make sure the setup does not suffer from significant voltage drops across not properly connected needles. An additional voltage source can be used to modify the default PA behavior. This option is not used for the measurement results presented in the following. The last voltage source on this edge of the device is used to control the switch behavior. Measurements are taken for both switch positions.

The plot in Figure 6.31 shows how the switch directs the RF power either to the thermistor or through the pad to the external power sensor. For the lines with a circle marker the switch is in the position where the RF power goes to the transmit pad and is measured externally. The lines with a triangle marker indicate that the signal is directed to the on-chip thermistor.

First let us focus on the black lines which do represent the external power

measurement and belong to the left y axis. The upper line is taken at the external power sensor when the switch is the position where RF power is directed to the transmit output. It is observed that the circuit has a linear gain of approximately 13 dB. At around 0 dBm input power the circuit starts to saturate and delivers >10 dBm of output power. The lower black line with the triangles shows what happens when the switch position is changed. Ideally, the output power at the transmit output would reduce towards $-\infty$. However, the limited isolation of the SPDT switch leads to a shift of the curve by approximately −20 dB. This shift agrees well with the isolation value shown in Figure 6.27 for the stand-alone switch.

Let us now focus on the red curves which are representing the resistance measured at the thermistor termination. The circled line is gained from the measurement when the switch directs the RF power to the transmit output. In this case the resistance remains constant along the input power sweep. The absolute value of 235 Ω deviates from the target value of 200 Ω due to process variation. However, the thermistor termination still provides a good match to the SPDT switch. The line with triangular markers shows what happens if the RF power is directed to the thermistor. Due to the heating caused by the power the resistance changes significantly up to values in the range of 300 Ω for an input power of 2 dBm.

In Figure 6.32 it is shown how the thermistor resistance changes for different DC and RF power levels. Note that the y axis represents the change in resistance on a logarithmic plot and the x axis is also in a logarithmic scale. The characteristic gained from the DC power sweep is represented by the straight red line in this plot. For the thermistor heating with RF power it is observed that the curve starts to bend for power levels >7 dBm. This is most likely related to the impedance that the thermistor provides to the SPDT switch which is >70 Ω instead of the target value of 50 Ω.

The most interesting question for the overall performance of the switch-based implementation of the thermistor is how accurate it can detect the RF power using only DC measurement equipment. The solid line in Figure 6.33 shows how the actual characteristic for the output power versus input power sweep looks like. The dash-dotted line is gained from the on-chip thermistor power sensor by DC power substitution. The difference between these two lines is treated as the inaccuracy of the thermistor power sensor and represented by the red line belonging to the right y axis. It is observed that for the output power range of interest for automotive radar applications of >0 dBm the error is smaller than ±1.1 dB.

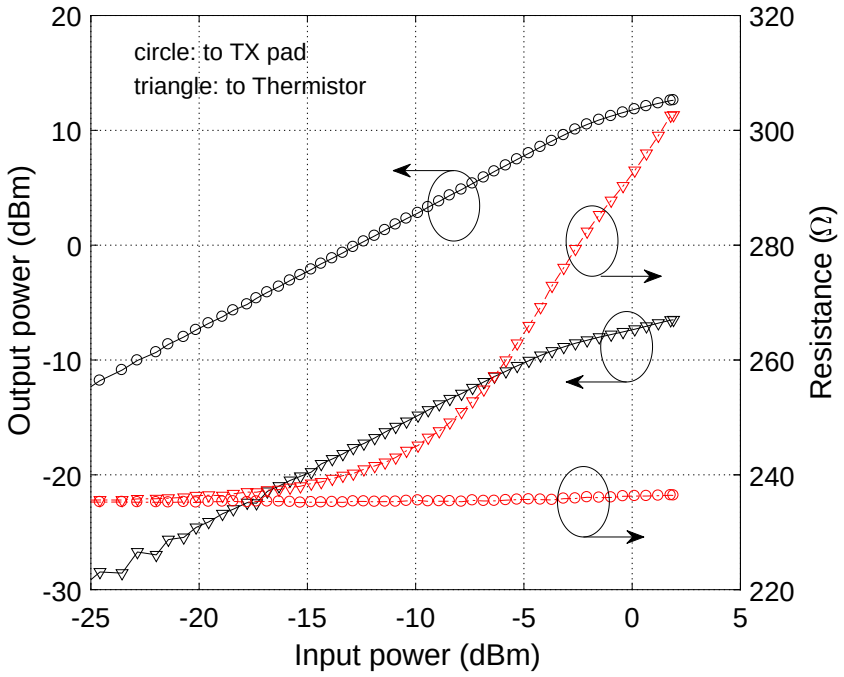


Figure 6.31: Output power and thermistor resistance for the two switch states over input power.

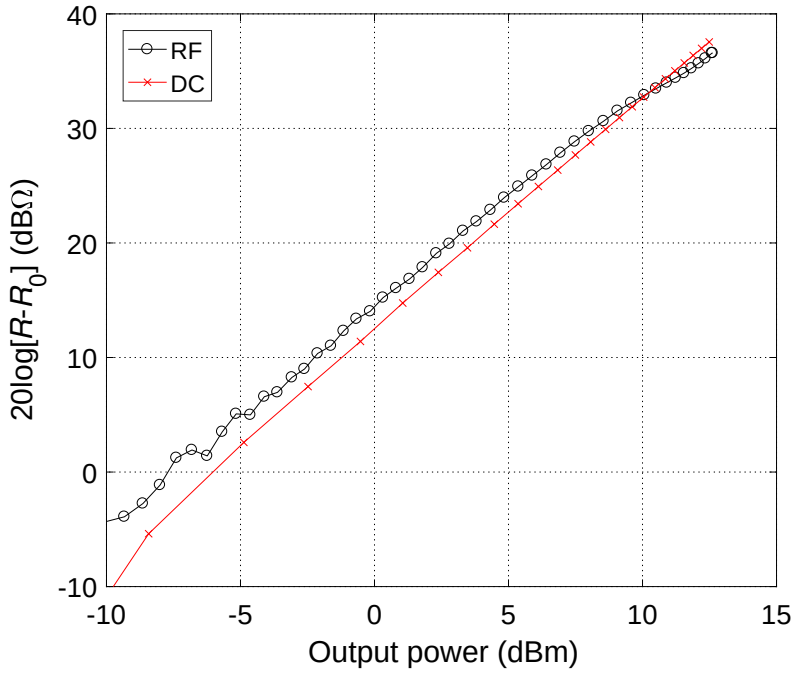


Figure 6.32: Change in thermistor resistance over input power.

6.3.3 Conclusion

In this section it was shown how the switch-based thermistor power sensor implementation can be realized. Therefor, an SPDT switch was implemented using reverse saturated HBTs in combination with $\lambda/4$ transmission lines. Publication [Wursthorn 16] provides further detailed design information on the circuit.

The stand-alone performance of the SPDT switch shows an insertion loss of 2.7 dB and an isolation value of >20 dB. These numbers can be further improved by using a fixed stub inductance to compensate the parasitic capacitance of the switch element in upcoming designs.

Furthermore, it is shown that the SPDT configuration is able to switch the used RF power levels reliably between the transmit output and the on-chip thermistor termination. For RF output power levels of >0 dBm a sensor accuracy of better than ±1.1 dB is observed.

As the principle is based on DC power substitution, no RF measurements are required to sense the power of the signal at the operating frequency on the IC. This will - as for the other solutions - allow straight forward implementation in high volume product test.

An advantage of the switch-based solution is that silicon area is smaller

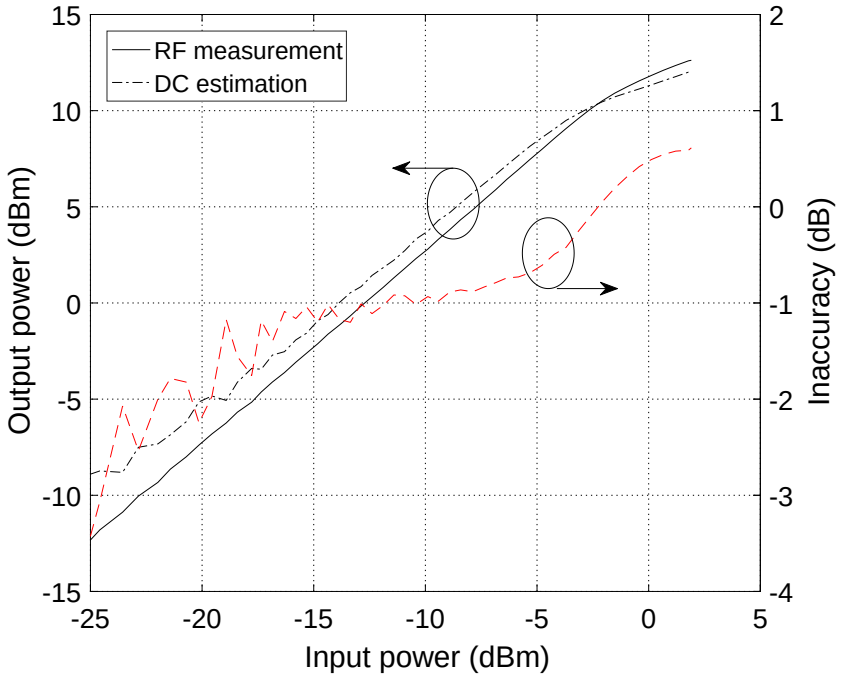


Figure 6.33: Output power and difference between RF and DC measurement.

compared to the implementation where a complete transmit channel is required. The main drawback is that the switch-based solution comes at the cost of an additional insertion loss in the transmit chain which is usually not tolerable as less output power in automotive radars results directly in less detection range. However, for future implementations it is expected that the insertion loss can be further reduced by optimized switch design and the area can be reduced by folding the $\lambda/4$ transmission lines.

6.4 Implementation using a Gilbert Cell Switching Quad

In this section another thermistor implementation is presented which falls in the category of the switch-based solution as mentioned in Section 5.2. This means no separate calibration channel is required but potentially additional losses in the active transmit channel will occur.

The presented DUT is manufactured in the B7HF200 technology and parts of it have been published in [Wursthorn 17]. The solution uses a Gilbert cell in the last amplifier stage as the switching element. Compared to the

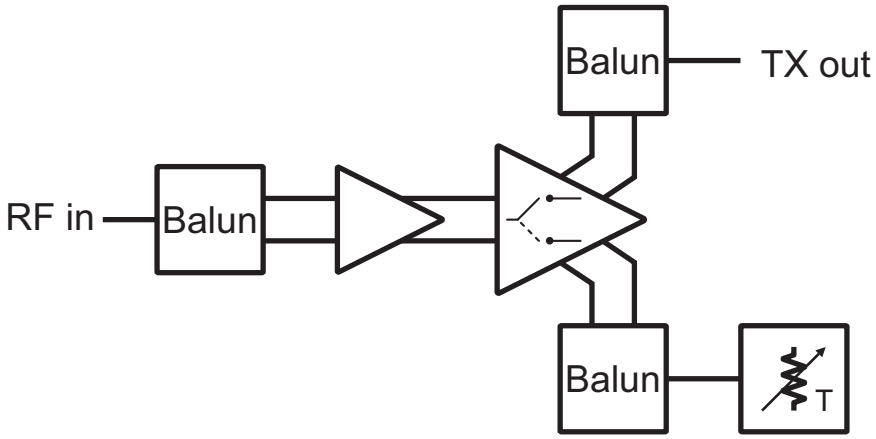


Figure 6.34: Block diagram of the presented DUT using a switching quad.

previously mentioned implementation using the SPDT switch, this solution does not require additional passive structures, potentially saving area.

The following sections will give an overview of the DUT and what has been implemented on the IC to investigate the thermistor accuracy. A detailed design description of the Gilbert cell amplifier is given including considerations for layout implementation. Furthermore, the RF measurement setup and results are shown and discussed.

6.4.1 Circuit Design

This section deals with design details for another implementation of the thermistor power sensor. A block diagram of the presented DUT is shown in Figure 6.34. The input and output interfaces are designed to be single-ended to simplify the measurement setup. For robustness, the internal signals are processed in differential mode. The single-ended to differential conversion is achieved by Baluns which are based on a lumped element approach which is presented in [Bakalski 02]. Furthermore, the Balun networks contain impedance matching structures. Realizing the single-ended/differential conversion and the impedance matching in one step leads to less loss compared to a separate approach.

The differential RF input signal is first fed to a buffer stage which provides sufficient output power to drive the succeeding stage in saturation. The buffer stage is based on the cascode topology and runs at a tail current of 20 mA which is drawn from a 3.3-volts power supply.

As indicated in the block diagram the second amplifier stage also contains the switching quad which directs the power either to the on-chip thermistor

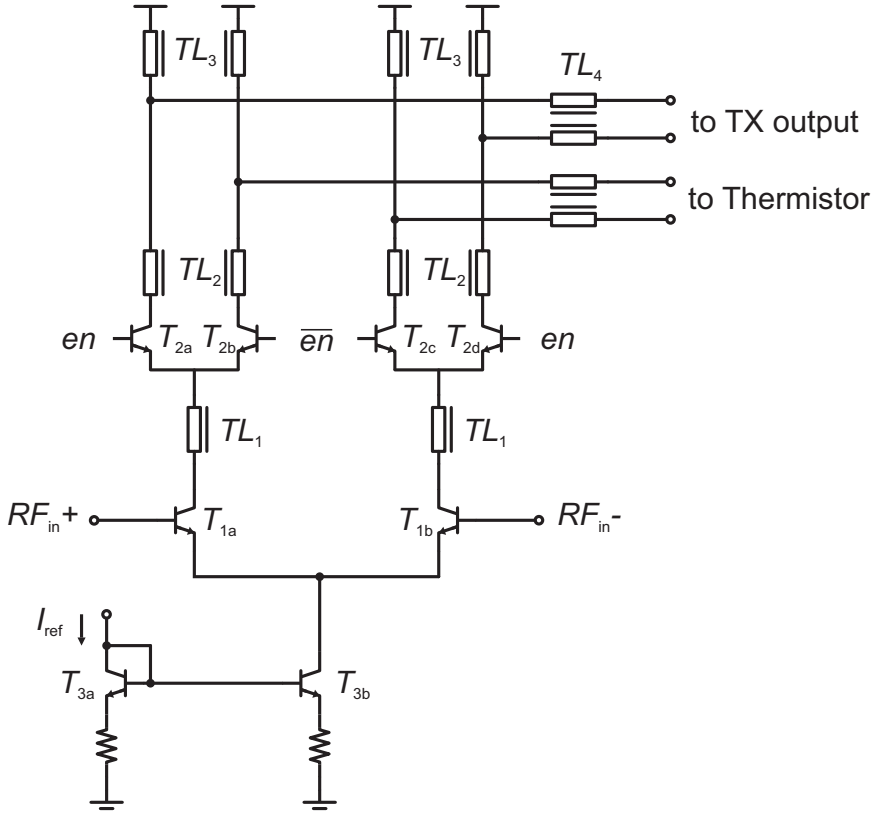


Figure 6.35: Schematic of the switching quad amplifier stage.

termination or to the TX output which can be measured with external equipment. The schematic in Figure 6.35 shows the amplifier stage on transistor level. The common emitter stage represented by T_{1a} and T_{1b} at the RF input is not different to a standard cascode input. The common emitter output however is connected through TL_1 to a switching quad instead of a standard common base stage. The enable signal (en) is used to control the base of the transistors T_2. Either the pair T_{2a}/T_{2d} or the pair T_{2b}/T_{2c} are enabled at the same time. If the transistors T_{2a}/T_{2d} are enabled their collectors provide a differential RF signal at the output which is connected to the TX. At the same time transistors T_{2b}/T_{2c} provide a high impedance from emitter to collector isolating the thermistor termination from the RF signal. An inverted enable signal results in a vice versa behavior.

The tail current for the amplifier stage is applied through the 1:4 current mirror made of the transistors T_{3a}/T_{3b}. A reference current of 12.5 mA leads to an effective tail current of 50 mA. The source degeneration resistor forces a voltage drop of approximately 100 mV.

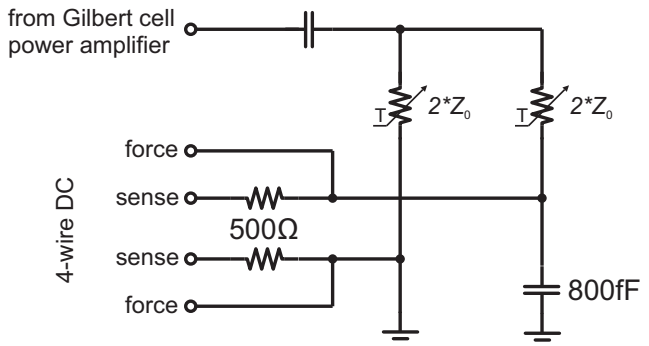


Figure 6.36: Schematic of the implemented thermistor termination.

The schematic in Figure 6.36 shows the implementation of the thermistor termination on the presented DUT. The implementation is based on the principle which is described in Section 4.3. An RF signal coming from the Gilbert cell PA is applied on the top left terminal. Two thermistors with a resistance of $2\,Z_0$ each provide an RF impedance of $50\,\Omega$. For the 4-wire DC measurement an impedance of $200\,\Omega$ is observed.

A micro photograph of the DUT which consumes $1.15\,\text{mm} \times 0.95\,\text{mm}$ is shown in Figure 6.37. The left edge is used to apply most of the analog and DC signals. Starting from the top there are pads for supply voltage (V_{CC}) and ground (G) connections. The reference currents for stage one and two (I_1 and I_2) are following below. The lower most pad provides the control signal (en) for the switch. The right edge is used for the 4-wire resistance measurement of the thermistor termination.

The GSG pad structure on the bottom is used to feed the 80 GHz signal to the circuitry. From there a long transmission line is used to connect to the input Balun and matching network. The succeeding stage is the first amplifier stage (PA1). The Gilbert cell amplifier PA2 is placed right next to the PA1. In a standard transmit chain the output would be expected on the right of PA2. However, in this case the RF output pad structure is located on top of the DUT. This is caused by the fact that the Gilbert cell amplifier has two RF branches towards the output which are layouted symmetrically. The second branch is connected to the thermistor termination towards the center of the IC. For both branches the differential to single-ended Balun networks are implemented.

Note, for the implementation on a multi channel transmitter IC, the orientation of the transmit chain has to be taken into account. Eventually, an additional 90° bend is required for proper connection.

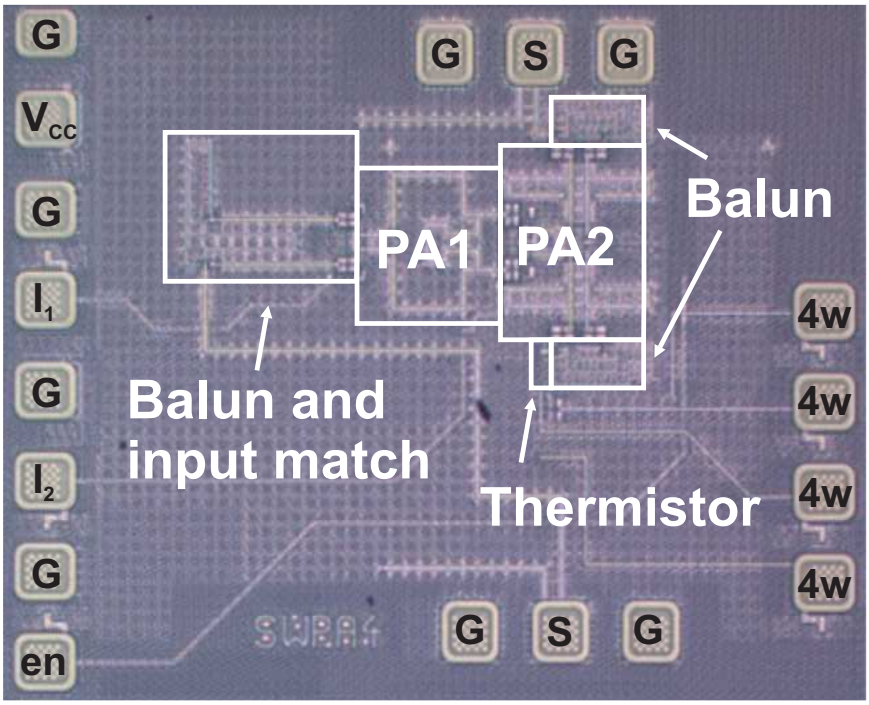


Figure 6.37: Photograph of the DUT using the Gilbert cell amplifier.

6.4.2 Measurement Setup and Results

This section deals with the RF measurement setup and the results of the DUT using the Gilbert cell amplifier. All measurements are performed as on-wafer measurements at room temperature on a manual probe station. Post-processing steps, like waveguide insertion loss corrections, are already considered in the shown results.

In Figure 6.38 it is shown how the on-wafer measurement setup looks like. The DUT is connected on all four edges with probe tips having a pitch of 125 µm. The connection of the DC signals located on the left side is done by a probe tip with 8 needles. A 3.3-volts supply is used to feed the DUT with DC power. A current source with multiple outputs is used to provide the reference currents for the two amplifier stages. An additional voltage source is used to control the *en* input which selects the state of the Gilbert cell.

The thermistor terminals for 4-wire measurement are provided on the right edge of the device. A probe tip with 4 needles is used to connect the force and sense signals to monitor the thermistor resistance. For the DC substitution the force current is increased until the thermistor resistance has the same value as previously measured when the device is heated by the dissipated RF power.

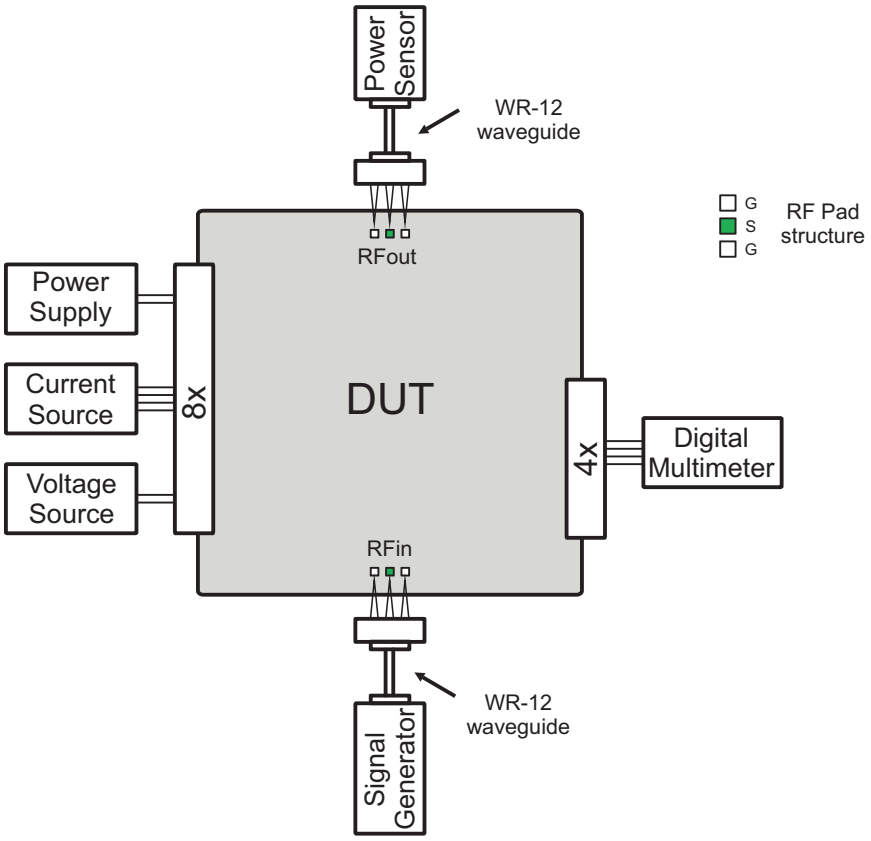


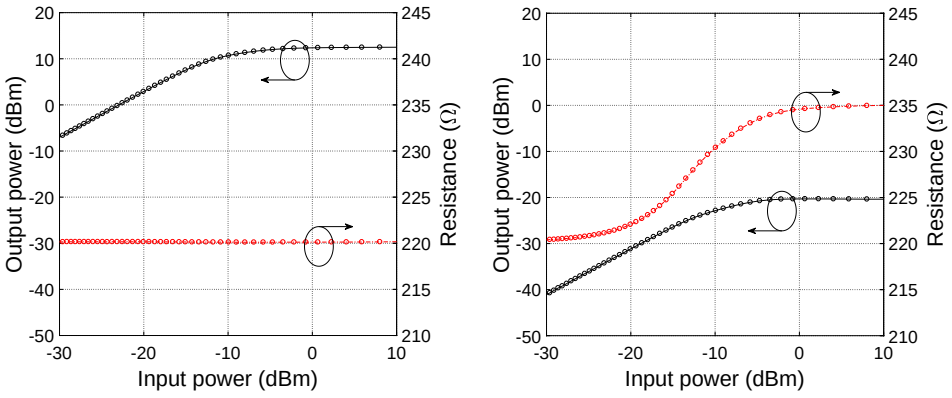
Figure 6.38: Measurement setup for the DUT using the Gilbert cell amplifier.

The RF signal is applied on the lower edge of the device. Therefor, a GSG WR-12 waveguide probe tip with a pitch of 125 µm is used. The power level of the signal generator is swept during measurements to gain a curve of thermistor resistance over RF power.

On the upper edge of the device an external power sensor is used to monitor the RF output power level. The connection is also realized by a GSG WR-12 waveguide probe tip with a pitch of 125 µm. The goal of the measurements is to show that the external power measurement results can be achieved as well with the on-chip thermistor power sensor with a tolerable error.

Depending on the *en* state the RF signal is taking either the branch to the transmit output or to the internal thermistor power sensor. For both switch positions it is of interest how the thermistor resistance and the output power at the transmit pad behave. The two plots in Figure 6.39 show the transmit out power and the thermistor resistance for the two Gilbert cell conditions.

Results in Figure 6.39a are taken for the state where the RF signal is



(a) (b)

Figure 6.39: Input power and thermistor resistance versus input power when power is directed to transmit output(a) or to the thermistor termination (b).

traveling towards the transmit output. The black curve represents the transmitter output power whereas the red trace is showing the behavior of the thermistor for applied input power levels.

The x axis shows the range which is covered by the input power level sweep. For an input power level of −30 dBm a transmit output power of −8 dBm is observed. A corresponding small signal gain of the amplifier of more than 20 dB is derived. Increasing the input power level to values larger than 0 dB leads to saturation of the amplifier. A maximum saturated output power of around 12 dBm is observed.

In this switch position ideally no RF power is directed towards the thermistor termination. The red curve shows that this assumption holds well as the thermistor resistance does not change over the complete input power range. The measured DC thermistor resistance of 220 Ω can be transferred into an RF impedance of 55 Ω which is slightly above the target value of 50 Ω.

In Figure 6.39b it is shown how the same outputs behave for the other state where the RF signal takes the thermistor branch. It can be observed that the resistance (red curve) now changes for different input power level. For an input power level of −30 dBm a resistance of 220 Ω is observed which is expected from the first plot. An input power level of 10 dBm results in a thermistor resistance of 235 Ω.

At the same time, the transmit output power characteristic looks similar to the one from Figure 6.39a but is shifted by more than 30 dB towards lower levels. This difference between the two black curves in the two figures corresponds to the isolation that the Gilbert cell amplifier provides between its two output terminals.

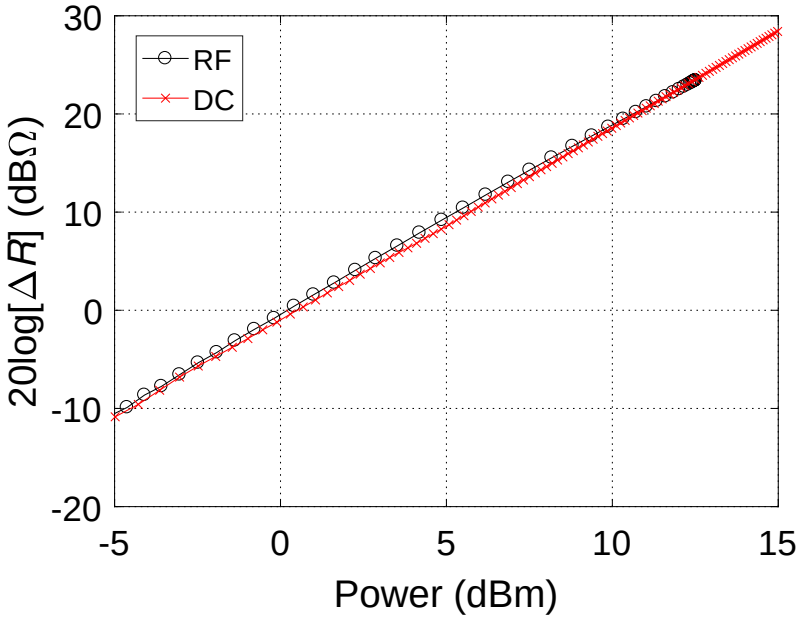


Figure 6.40: Change in thermistor resistance over applied power level.

The graph in Figure 6.40 shows the behavior of the thermistor over applied RF (black line) and DC (red line) power. Ideally, the two lines would be coinciding. The observed difference is caused by (RF) measurement inaccuracies and will contribute to the inaccuracy of the thermistor power sensor. The straight lines once again show the desirable linear behavior of the thermistor resistance over applied power which is favorable for most kinds of sensors.

The most interesting part of the measurement results of the presented DUT is shown in Figure 6.41. The solid black line represents the standard output power over input power characteristic of an amplifier for the measurement using the external RF power sensor. The black dash-dotted line is gained from the evaluation of the DC signals of the on-chip thermistor power sensor without any external measurement equipment. The difference between the two black lines is considered to be the inaccuracy of the thermistor power sensor and shown as the red dashed line. It is observed that the inaccuracy of the thermistor sensor is less than $\pm 0.6\,\mathrm{dB}$ over the entire input power range. For the saturated output power range of the PA the inaccuracy is less than $\pm 0.15\,\mathrm{dB}$.

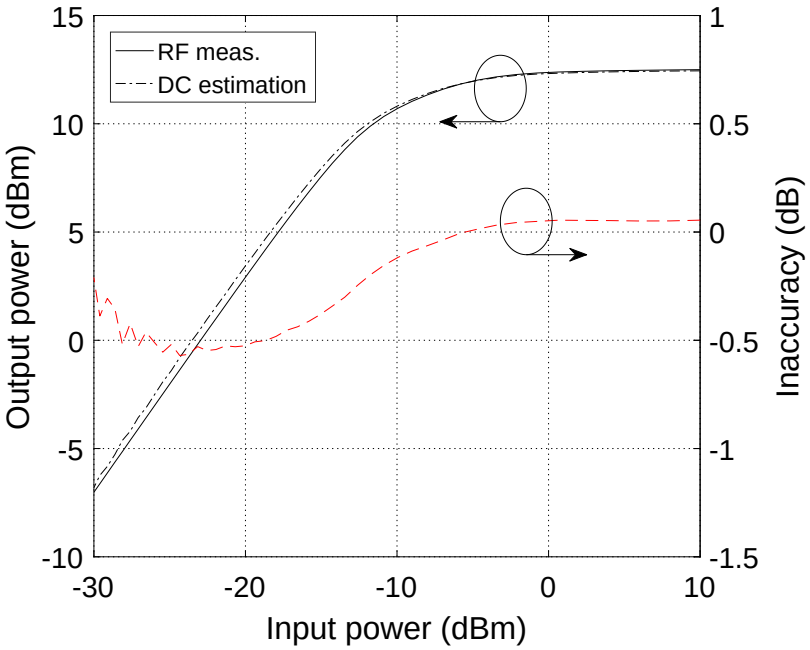


Figure 6.41: Measured and estimated output power and thermistor inaccuracy over input power level.

6.4.3 Conclusion

In this section another thermistor power sensor implementation from the switch-based category was shown. The approach is similar to what has been presented in [Wursthorn 17]. A Gilbert cell is used to either feed the RF signal to the transmit branch or the thermistor branch. This solution proved to have an isolation of more than 30 dB between the two branches while providing a saturated RF output power of 12 dBm. Furthermore, it is shown that the proposed solution works as accurate as ±0.6 dB over a large range of power. For an operation scenario where the amplifier is in saturation the error minimizes to less than ±0.15 dB.

The fact, that this on-chip RF power sensor only requires DC signals to be evaluated makes it a good candidate for productive test equipment.

Upcoming implementations using this approach will benefit from progress in technology development as parasitic capacitance is expected to be reduced. This will allow to further trade isolation for maximum saturated output power depending on the application.

6.5 Comparison and Rating of the different Implementation Options

The previous sections gave a detailed description on the different thermistor implementation test circuits. In general, four different ways of integrating the thermistor in a state of the art transmitter were presented and are summarized in the following.

1. **Wilkinson Splitter:** The first presented device uses a passive Wilkinson divider to equally split the available power between the thermistor termination and the transmitter output. On the one hand, this results in a straight forward measurement implementation in the laboratory while on the other hand the available output power is only 50 % of what has been generated on the device.

2. **Additional Calib. Path:** The additional calibration path method requires a separate chain in parallel to the active transmit chains which is terminated with the thermistor power sensor. The occupied area for this solution is potentially the highest. However, the additional chain can be a reduced copy of the active transmit chains to save area. Furthermore, if the number of transmit channels is increased the relative occupied area is decreased as well.

3. **SPDT Switch:** The first switch-based approach which is presented uses an SPDT switch to either feed the signal power to the thermistor termination or the transmit output. The comparably compact layout of this solution has the drawback that the insertion loss, which is caused by the switch, is visible in the transmit chain reducing the output power.

4. **Switching Quad:** The other approach from the switch-based category uses a Gilbert cell switching quad in the last power stage to direct the signal power either to the thermistor termination or the transmit output. This kind of switch maintains good isolation between its two outputs while keeping a moderate output power level. Challenges arise in a multi channel transmitter layout caused by the orientation of the last stage.

A quantitative comparison of the Key Performance Indicators (KPIs) is given in Table 6.1. A plus sign represents a better rating for the according parameter. The calibration path for example shows a minus sign for the KPI

Table 6.1: Comparison table of presented thermistor power sensor implementations.

	Wilkinson	Calib. Path	SPDT Sw.	Sw. Quad
Area	∘	–	+	+
Power Cons.	–	+	∘	∘
Complexity	+	+	∘	–
Impact on TX Ch.	–	+	∘	∘
Accuracy	±0.6 dB	±0.55 dB	±1.1 dB	±0.6 dB

named Area which means it is worse compared to the others and not that it consumes less area.

In terms of occupied layout area the switch-based approaches are ahead of the others. The Wilkinson solution suffers from the $\lambda/4$ lines while the additional calibration path obviously requires the most area for additional amplifier stages and matching networks.

The direct power consumption of the individual presented approaches is only present during the calibration period and therefore strongly depends on the duty cycle. The assumption for the comparison in Table 6.1 is that a one-time calibration per turn-on of the device is sufficient for functionality and therefore the active power consumption vanishes for all approaches except the Wilkinson where 50 % of the power are permanently dissipated resulting in the worst rating. What is compared in the table for the other implementation principles is the indirect power consumption caused by the losses of the respective solution. For the additional calibration path only a small additional buffer is required before the signal distribution network as it has to feed one more chain. The switch-based solutions introduce an insertion loss in the active transmit chain which has to be compensated by the amplifier.

To realize the thermistor termination on-chip some additional design effort is required. Adding a passive Wilkinson splitter or copying the complete transmit chain will add a low level of complexity. The implementation of an SPDT switch with low losses requires a little more design effort. Re-designing the last amplifier stage to a Gilbert cell switching quad will consume the most design time of all presented solutions.

The impact on the active transmit channel is closely related to the comparison of the power consumption. Here, the solution using the additional calibration path has the best rating as it has no direct impact on the active

transmit channels. The switch-based approaches as well as the Wilkinson approach do add additional losses to the active chain resulting in a less good rating.

Last but not least, the accuracy of the different implementations is compared. The stated values are valid for transmit output power levels above 0 dBm, as this is the typical range of operation for automotive radar transmitters. The accuracy which is achieved with the Wilkinson and the additional calibration path is $\pm 0.6\,\mathrm{dB}/\pm 0.55\,\mathrm{dB}$. The SPDT and the switching quad show $\pm 1.1\,\mathrm{dB}$ and $\pm 0.6\,\mathrm{dB}$ of inaccuracy, respectively. Please note, the sensors are also functional for output power levels below 0 dBm. However, the accuracy will suffer the smaller the power level gets.

Including all given constraints of the state of the art, the additional calibration path seems to be the best candidate for product implementation. The only existing drawback compared to the other solutions is the consumed silicon area. However, the area of a state of the art automotive radar transceiver is dominated by the isolation between the channels. To keep a tolerable isolation level, the distance between the transmit outputs offers some unused space which can partly be used for the additional channel. Furthermore, it is not necessary that the additional channel supports all features that a transmit channel offers resulting in less area.

Chapter 7

Conclusion

Wireless communications and automotive radar applications are the drivers for high volume production of millimeter wave integrated circuits. This leads, especially for automotive products, to the challenging task of testing, where every single device needs to be verified to secure automotive quality standards. The goal of this thesis is to develop and verify an on-chip thermal-based power sensor concept to reduce the test effort.

After a brief introduction to the basics of millimeter wave power detection and the state of the art in automotive radar transceivers, it turns out that an absolute on-chip power measurement is required to calibrate the existing sensors. The investigation of various layers in the available technologies show that the implementation of a thermistor is possible and has low dependency on process variation. A silicided polysilicon layer is used as the thermistor material. It shows a TC of $2.01 \cdot 10^{-6}\,\mathrm{K}^{-1}$ and $2.88 \cdot 10^{-6}\,\mathrm{K}^{-1}$ for the B7HF200 and B11HFC technology, respectively. The availability of such a silicided polysilicon layer is under no circumstance limited to the investigated technologies. Many state of the art CMOS processes are using such material to reduce the gate resistance of the transistors. This means that the proposed sensor concept can in general be transferred to any standard CMOS process which uses polysilicon gate electrodes.

Furthermore, it is shown how the existing resistor model can be extended by the thermal domain to represent self-heating effects correctly. In this context, it is also presented how the thermal modeling parameters R_{th} and C_{th} are derived, and what impact they have on the device behavior in simulations.

Additionally, it is discussed how the thermistor power sensor can be implemented in state of the art multi channel automotive radar transmitters. In general, the approaches for implementation are either based on an active switch, or they require a passive power splitter. For each category, two ICs are developed for verification. The Wilkinson splitter after the last amplifier

stage, and the additional calibration path are representing the splitter category. Switch-based approaches are the SPDT switch and the Gilbert cell switching quad in the last amplifier stage.

The measurements on the four DUTs show functionality and work as expected. The results of the on-chip power measurement gained from the thermistor structure, using a DC substitution principle, are compared to corresponding external RF measurements. From these measurements an inaccuracy range from ±1.1 dB down to ±0.55 dB is observed for the different approaches for output power levels above 0 dBm.

First, a solution using the passive Wilkinson splitter after the last amplifier stage was presented. It is the solution which is easiest to characterize as RF output power and thermistor behavior can be measured simultaneously. Measurements are carried out on a wafer with chessboard pattern showing less than 1 dB variation over all samples. However, a product implementation of this solution is unlikely as it permanently dissipates more than 50 % of the available power in the thermistor termination.

Taking into account all the discussed aspects of the four different approaches the one using the additional calibration path is the best candidate for straight forward product implementation with low risk and impact on existing solutions. It can make use of the empty space between the existing transmit channels which reduces the effective occupied silicon area. Furthermore, it shows promising accuracy of better than ±0.6 dB over the whole range of power levels which are interesting for automotive radar applications. The method of calibrating the existing sensors with the additional path and the thermistor are therefore filed in patents [Knapp 17], [Wursthorn 18] and [Kammerer 19].

If a little more risk can be taken for the implementation and a re-design of the last power amplifier stage is tolerable, the switching quad solution might be a good choice. It shows good accuracy of better than ±0.55 dB. In the saturated output power region, the inaccuracy is even less than ±0.15 dB. However, it is important to keep in mind that additional layout considerations are necessary as there is a 90° bend between the RF input and output of the circuit.

The shown results for the SPDT solution were not as promising as the other approaches. However, if the thermistor principle is transferred to an advanced CMOS technology the switch-based approach might get into focus as the insertion loss as well as the isolation are expected to improve.

For future implementations the main focus for optimization will be on the thermistor termination itself. For the developed test ICs, the thermistor impedance varies when RF power is applied. This effect can be minimized by designing the impedance below the characteristic system impedance. Then

additional DC power can be applied until the target value is reached. If additional RF power is also dissipated in the device, the amount of DC power can be reduced. The concept of power substitution stays the same as in the presented solution.

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