# Design of Highly Integrated Interface Electronics for Capacitive Micromachined Ultrasonic Transducers

**Prajith Kumar Poongodan**

Vollständiger Abdruck der von der Fakultät für Elektrotechnik und Informationstechnik (EIT) der Universität der Bundeswehr München zur Erlangung des akademischen Grades eines

**Doktor-Ingenieurs (Dr.-Ing.)**

genehmigten Dissertation.

Gutachter:

1. Prof. Dr. techn. Linus Maurer
2. Prof. Dr.-Ing. Ralf Brederlow

Die Dissertation wurde am 22.11.2022 bei der Universität der Bundeswehr München eingereicht und durch die Fakultät für Elektrotechnik und Informationstechnik (EIT) am 10.03.2023 angenommen. Die mündliche Prüfung fand am 12.04.2023 statt.

# Declaration

I hereby declare that except where specific reference is made to the work of others, the contents of this dissertation are original and have not been submitted in whole or in part for consideration for any other degree or qualification in this, or any other university. This dissertation is my own work and contains nothing which is the outcome of work done in collaboration with others, except as specified in the text and Acknowledgements.

Prajith Kumar Poongodan
April 2023

# Acknowledgements

First, I would like to thank my advisor Prof. Linus Maurer for his guidance, support and valuable insights throughout my doctoral studies. I would also like to thank my second examiner Prof. Ralf Brederlow for his valuable time in reviewing my manuscript and providing feedback.

This work was done in close collaboration between Fraunhofer EMFT and Universität der Bundeswehr München. I would like to thank my group manager Frank Vanselow who initiated this project and trusted me with it for my doctoral work. I appreciate his support, guidance and mentorship to go deeper with my research work and his valuable technical insights. Special thanks to David Borggreve and Pragoti Bora who decided to accept me to work with them for my master thesis which brought me into the circuit design team. I had wonderful learning experience and fun during all our technical discussions. Furthermore, I would like to express my thanks to Enno Böhme for all the support during the tapeouts and help with the digital designs. Thanks to Oleg Sakolski whose master thesis contribution was very important to this work. I would also like to thank my other colleagues at the circuit design group Radu Ciocoveanu, Erkan Isa, Harshitha Basavaraju, Lei Zhang, Jakob Stuprich, Ferdinand Pscheidl, Pengcheng Xu, Sebastian Ruping, Aleksander Bajt, Himadri Shekhar Bhattacharyya and Piyush Kumar for their support and wonderful time in the office.

I would also like to thank the ProTaktilUS project consortium partners at Fraunhofer IPMS, Fraunhofer IKTS and Fraunhofer IFF for their assistance throughout the project and the wonderful working environment created during the project.

Finally, I would like to thank my parents Janardhanan and Preetha and my brother Hari for their continuous support over these years. I would like to express my deepest gratitude to my wife Vaani for being exceptionally understanding, supportive and encouraging throughout the years.

# Abstract

Ultrasound based sensing modality is one of the oldest in medical and industrial applications. Advancements in micromachining techniques opened up possibilities to develop micromachined ultrasonic transducers (MUTs). Of these, capacitive micromachined ultrasonic transducer (CMUT) technology has proven to be a promising alternative to conventional bulk piezoelectric based ultrasonic transducers. This enabled the design and development of miniaturized CMUT based sensor solutions for a wide range of applications. The medical imaging has benefited a lot from the advancements in CMUT fabrication technology. Advances in high voltage (HV) integrated circuit design processes for high voltage and high power applications opened up the opportunity to design highly compact application specific integrated circuits (ASIC) for such transducers. The CMOS compatibility of CMUTs makes it a very attractive option for a monolithic integrated CMUT sensor system.

In this thesis, the design of integrated circuits to interface a CMUT array is addressed. Circuit architectures are investigated and implemented to enable a highly integrated CMUT-ASIC system. A novel CMUT driving architecture is presented which eliminates the need to use an external bias tee circuit to bias the CMUT to HV levels. The structure also helps to avoid the use of HV isolation switch in the receive path of the transceiver channel. This reduces the die area and helps to improve the signal to noise ratio (SNR). Design and implementation of an 8 channel transceiver ASIC in 0.18 µm HV silicon on insulator (SOI) technology is presented. Design of key circuit blocks in the transmit path including HV pulsers, level-shifters, HV linear regulator and other auxillary circuits are provided and the performance verification through silicon measurements are also presented. In the receive path, a resistive feedback transimpedance amplifier (TIA) is used for converting the time-varying input current into an output voltage. Four adjustable gain settings are possible for the designed TIA. Measurement results are provided which validates the analysis and design presented. A pulse-echo measurement result demonstrates the capability of the complete system to be operated as proposed.

A transmit beamforming circuit for phased array actuation of CMUT arrays is presented in the final part of the thesis. An architecture combining an analog wide-range delay locked loop (DLL) and digital circuits is implemented. Such a very low-power area efficient approach

demonstrates the possibilities of circuit integration on front-end ASICs for CMUT based imaging devices. Extensive simulation results presents the feasibility of the proposed solution to perform a high resolution beam focusing and steering using only a single low frequency clock source. The digital circuit blocks provide further flexibility to the ASIC by adding of frequency division and pulse count functionality.

# Kurzfassung

Ultraschall ist eine der ältesten Sensormethoden für medizinische und industrielle Anwendungen. Fortschritte in der Mikrofertigungstechnik ermöglichen die Entwicklung mikromechanischer Ultraschallwandler (MUTs). Die Technologie der kapazitiven mikromechanischen Ultraschallwandler (CMUT) hat sich dabei als vielversprechende Alternative zu konventionellen Ultraschallwandlern auf piezoelektrischer Basis erwiesen. Dies ermöglichte das Design und die Entwicklung von miniaturisierten CMUT-basierten Sensorlösungen für ein breites Spektrum von Anwendungen. Die medizinische Bilderzeugung hat stark von den Fortschritten in der CMUT-Technologie profitiert. Fortschritte bei der Entwicklung integrierter Hochspannungsschaltungen für Hochspannungs- und Hochleistungsanwendungen ermöglichten die Entwicklung hochkompakter anwendungsspezifischer integrierter Schaltungen (ASIC) für solche Wandler. Die CMOS-Kompatibilität von CMUTs macht sie zu einer sehr attraktiven Option für ein monolithisch integriertes CMUT-Sensorsystem.

In dieser Doktorarbeit wird der Entwicklung integrierter Schaltungen für die Schnittstelle eines CMUT-Arrays behandelt. Es werden Schaltungsarchitekturen untersucht und implementiert, um ein hochintegriertes CMUT-ASIC-System zu ermöglichen. Es wird eine neuartige CMUT-Ansteuerungsarchitektur vorgestellt, die den externen Biaseinspeisungsschaltkreis zur Einstellung des CMUT auf HV Pegel vermeidet. Die Struktur trägt auch dazu bei, den Hochspannungsisolationsschalter im Empfangspfad des Transceiverkanals zu vermeiden. Dies reduziert die Chipfläche und trägt zur Verbesserung des Signal-Rausch-Verhältnisses (SNR) bei. Es wird der Entwurf und die Implementierung eines 8 Kanal Transceiver ASICs in Silizium-auf-Isolator (SOI) Technologie vorgestellt. Das Design der wichtigsten Schaltungsblöcke im Sendepfad, einschließlich HV Pulsern, Pegelumsetzern, Hochspannungslinearreglern und anderen Zusatzschaltungen, wird vorgestellt und die Leistungsüberprüfung durch Siliziummessungen wird ebenfalls präsentiert. Im Empfangsweg wird ein Transimpedanzverstärker (TIA) mit Widerstandsrückkopplung zur Umwandlung des zeitvariablen Eingangsstroms in eine Ausgangsspannung verwendet. Für den entwickelten TIA sind vier einstellbare Verstärkungseinstellungen möglich. Es werden Messergebnisse vorgelegt, die die vorgestellte Analyse und den Entwurf validieren. Die Ergebnisse einer

Puls-Echo Messung zeigen, das der entwickelte Prototyp in der Applikation wie gewünscht funktioniert.

Im letzten Teil der Doktorarbeit wird eine Transmit Beamforming Schaltung für phasengesteuerten Arraybetrieb von CMUT-Arrays vorgestellt. Es wird eine Architektur implementiert, die eine analoge Delay Locked Loop (DLL) mit hoher Bandbreite und digitale Schaltungen kombiniert. Dieser sehr stromsparende und flächeneffiziente Ansatz demonstriert die Möglichkeiten der Schaltungsintegration auf Front-End-ASICs für CMUT-basierte Bildgebungsgeräte. Ausführliche Simulationsergebnisse zeigen die Realisierbarkeit der vorgeschlagenen Lösung für eine hochauflösende Strahlfokussierung und -steuerung mit nur einer einzigen niederfrequenten Taktquelle. Die digitalen Schaltungsblöcke bieten weitere Flexibilität für den ASIC durch zusätzliche Funktionen zur Frequenzteilung und Impulszählung.

# Table of contents

**List of figures** **xiii**

**List of tables** **xix**

**List of Acronyms** **xxi**

**List of Symbols** **xxv**

**1 Introduction** **1**

1.1 Motivation and research objective . . . . . 2

**2 Ultrasound System** **7**

2.1 Conventional CMUT driving architecture . . . . . 7

2.2 Proposed CMUT driving architecture . . . . . 8

2.3 Ultrasonic Transceiver Chip Architecture . . . . . 10

2.4 High Voltage Process Technology . . . . . 14

**3 Integrated Circuits for CMUT Transceiver Interface** **17**

3.1 Background . . . . . 17

3.2 High Voltage Transmit Pulser Circuit . . . . . 18

3.2.1 Static level shifter based pulser design . . . . . 19

3.2.2 Gate charge recycled level shifter based pulser . . . . . 23

3.2.3 Nanosecond delay dynamic level shifter based pulser circuit . . . . 26

3.3 High Voltage, Fast Transient Response and High Current Sinking Linear Regulator . . . . . 34

3.3.1 Measurement results . . . . . 43

3.4 Low Voltage Receiver Front-End Design . . . . . 46

3.4.1 Open-loop transimpedance amplifiers . . . . . 46

3.4.2 Feedback transimpedance amplifiers . . . . . 48

3.5 Start-up clamp circuit . . . . . 65
3.5.1 Bandgap reference circuit . . . . . 66
3.5.2 Symmetric OTA . . . . . 68
3.6 Transceiver Chip Performance and Comparison to State of the Art . . . . . 69

**4 Transmit Beamforming Circuit Design 75**
4.1 Introduction . . . . . 75
4.2 Beamforming architectures . . . . . 76
4.3 Delay Locked Loop . . . . . 79
4.3.1 Frequency response . . . . . 80
4.3.2 DLL operation . . . . . 81
4.3.3 Voltage controlled delay line design . . . . . 87
4.3.4 Dynamic phase detector . . . . . 91
4.3.5 Charge pump . . . . . 94
4.3.6 Transmit beamforming output simulation results . . . . . 109

**5 Conclusion 113**
5.1 Summary . . . . . 113
5.2 Enhancement to state of the art . . . . . 115

**References 117**

**List of publications 125**

**Appendix A Verilog codes 127**

# List of figures


1.1 Cross section view of a conventionally used bulk piezoelectric transducer. . 2
1.2 Cross section view of a Capacitive Micromachined Ultrasonic Transducer (CMUT). . . . . 4
1.3 (a) Circuit used to interface the CMUT when operated as an ultrasound transmitter; (b) Circuit interface for the CMUT when used as an ultrasound receiver. . . . . 5

2.1 A conventional block diagram of ultrasound based system. . . . . 7
2.2 A conventionally used driving structure for a pulse-echo operation. . . . . 9
2.3 The proposed transmit-receive structure for the pulse-echo operation. . . . . 10
2.4 Block diagram representation of the designed CMUT transceiver ASIC. . . 11
2.5 Microphotograph of the ProTaktilUS_A0 chip. . . . . 12
2.6 Microphotograph of the ProTaktilUS_B0 chip. . . . . 12
2.7 Chip layout of the ProTaktilUS_C0 chip which is under fabrication. . . . . 13
2.8 Cross section view of a super junction high voltage NMOS (LNDMOS) transistor [14], [15]. . . . . 14
2.9 Symbols used for the different MOSFETs used in designs. . . . . 15

3.1 The top-level block diagram of the high voltage pulser circuit. . . . . 18
3.2 Static level shifter based pulser circuit . . . . . 19
3.3 Current limited static level shifter based pulser circuit. . . . . 20
3.4 High voltage output of the pulser circuit. . . . . 21
3.5 Gate drive signals of the push-pull stage. . . . . 21
3.6 Current through transistors $M_1$ and $M_2$. . . . . 22
3.7 Gate charge recycled level shifter based pulser circuit. . . . . 23
3.8 (a) Simulation results showing gate drive signal of the low-side and high-side; (b) Output of the pulser circuit. . . . . 24
3.9 (a) Currents through the transistors $M_1$ and $M_2$; (b) Input control signals. . 25

3.10 Dynamic level shifter based pulser circuit. . . . . 26
3.11 (a) Post-layout simulation showing the HV pulser output and the high side and low side gate drive voltages of the push-pull stage; (b) Simulation showing the drain currents through the transistors $M_1$ and $M_2$. . . . . 28
3.12 Die photo and layout of the pulser circuit highlighted. . . . . 29
3.13 The test PCB with the two transceiver chips and external control and power circuits. . . . . 31
3.14 (a) Measured output of the HV pulser circuit at 2 MHz; (b) pulser output showing response to an input triggering signal. . . . . 32
3.15 (a) Measured crosstalk between two adjacent HV pulser channels; (b) Frequency spectrum of the two channels. . . . . 32
3.16 A PMOS pass transistor LDO. . . . . 34
3.17 The designed HV linear regulator topology with current sinking capability. . 35
3.18 Small-signal gain presented by the output stage for maximum and minimum load conditions. . . . . 36
3.19 AC circuit of the linear regulator used to derive the small-signal equivalent circuit. . . . . 37
3.20 Small-signal equivalent circuit of the HV regulator. The compensation capacitor is not shown. . . . . 37
3.21 Small-signal equivalent circuit of the HV regulator with lead compensation capacitor connected. . . . . 38
3.22 Schematic of the linear regulator with a class AB error amplifier. . . . . 40
3.23 Magnitude and phase response plot of the loop-gain of the uncompensated regulator at the two dc operating points. . . . . 41
3.24 Magnitude and phase response plot of the loop-gain of the regulator at the two dc operating points after adding the compensation capacitor. . . . . 42
3.25 Die photo and layout of the HV linear regulators highlighted. . . . . 43
3.26 Measurement results showing the start up behavior of the low side HV regulator. The regulator settles to around 10.2 V in 270 ns. . . . . 43
3.27 Measurement result showing the line regulation behavior of the low-side regulator. . . . . 44
3.28 (a) Measurement result showing the transient load response of the 11 V linear regulator when all 8 channels of the HV pulsers are turned on; (b) The regulator output ripple voltage after AC coupling the output voltage. . . . . 44
3.29 (a) Conversion of CMUT current to voltage output; (b) Equivalent circuit. . 46
3.30 (a) Schematic of the CG-TIA; (b) Regulated cascode CG-TIA. . . . . 47

3.31 (a) A feedback TIA with common gate input stage (Shunt-shunt feedback amplifier); (b) Closed loop small-signal model. . . . . 48
3.32 Open loop small-signal model of Fig. 3.31b. . . . . 49
3.33 Schematic diagram of a resistive feedback transimpedance amplifier. . . . . 50
3.34 Closed-loop small signal model of the TIA. . . . . 50
3.35 Open-loop small signal model of the TIA. . . . . 51
3.36 Open loop small-signal model to calculate the output resitance of the TIA. . 51
3.37 Schematic diagram of the designed resistive feedback transimpedance amplifier. 53
3.38 Die photo and the layout of the receiver circuit is highlighted. . . . . 54
3.39 Measured frequency response of the TIA. . . . . 55
3.40 Measured input-referred noise current. . . . . 55
3.41 (a) Measured crosstalk between one HV pulser channel and the TIA of the same channel; (b) Frequency spectrum of the two circuits. . . . . 56
3.42 (a) Measured crosstalk between two adjacent receive channels; (b) Frequency spectrum of the two channels. . . . . 57
3.43 Measurement data showing the TIA dynamic range. . . . . 57
3.44 (a) A PMOS source follower; (b) small-signal equivalent circuit. . . . . 58
3.45 Schematic diagram of a super source voltage follower. . . . . 59
3.46 Small-signal equivalent circuit of the super source voltage follower. . . . . 60
3.47 (a) Simulated response of the SSF to a step input voltage; (b) Drain currents of the transistors $M_2$ and $M_1$. . . . . 62
3.48 Layout of the TIA with super source follower. . . . . 63
3.49 (a) Gain of the receiver; (b) Input referred noise of the receiver. . . . . 64
3.50 Block diagram of the start-up monitor circuit. . . . . 65
3.51 Schematic of the 1 V bandgap voltage reference circuit. . . . . 66
3.52 (a)Post-layout simulation showing the BGR output voltage against temperature sweep; (b) BGR output variation with a dc sweep of the supply voltage. 67
3.53 Schematic of the OTA used as comparator. . . . . 68
3.54 (a) Plot showing the operation of the clamp circuit; (b) the 60 V power supply ramp-up and the ramp-up of the 56 V linear regulator is also shown here. . . 69
3.55 High voltage pulses applied to the airborne CMUT under test. . . . . 72
3.56 Echo received at the output of the transimpedance amplifier measured by oscilloscope with the target at approximately 1 cm from the CMUT. . . . . 73
3.57 Pulse-echo measurement result of the low voltage CMUT immersed in silicone oil. . . . . 74

4.1 Illustration of the transmit beamforming using a CMUT array. . . . . 76

4.2 Block diagram of the digital beamforming architecture presented in . . . . 77
4.3 Block diagram of the proposed DLL based transmit beamformer circuit. . . 78
4.4 Block diagram of a conventional delay locked loop. . . . . 79
4.5 S-domain linear model of the DLL. . . . . 80
4.6 Illustration of DLL locking operation and frequency locking range. . . . . 82
4.7 A wide range DLL with a replica delay line (RDL). . . . . 84
4.8 Replica delay line with current steering phase detector (CSPD) and representation of waveforms showing operation. . . . . 85
4.9 Gain curve of the CSPD and locking range. . . . . 86
4.10 Schematic diagram of a current starved delay cell with dual control. . . . . 87
4.11 (a) Post-layout simulation result showing the delay variation against a sweep of coarse control voltage. The fine control voltage set at 800 mV; (b) delay variation against sweep of fine control voltage. Coarse control voltage set at 1.2 V. . . . . 88
4.12 (a) Post-layout simulation result showing the delay variation of the complete delay line against a sweep of coarse control voltage. The fine control voltage set at 800 mV; (b) delay variation of delay line against sweep of fine control voltage. Coarse control voltage set at 1.2 V. . . . . 89
4.13 Transient simulation of the delay line with a 20 MHz clock input. The coarse control voltage is set at 2 V and fine control voltage at 800 mV . . . . . 90
4.14 (a) An XOR phase detector, (b) a phase-frequency detector. . . . . 91
4.15 Schematic diagram of the dynamic phase detector circuit to generate the UP and DN control signals for the charge pump. . . . . 92
4.16 Waveforms showing the operation of the PD. . . . . 92
4.17 Simulation result showing the operation of the dynamic phase detector. . . . 93
4.18 (a) Drain-switched charge pump, (b) source-switched charge pump, (c) gate-switched charge pump. . . . . 94
4.19 A conventional source-switched charge pump and its charge and discharge operation. . . . . 95
4.20 Designed charge pump and loop filter. . . . . 97
4.21 Complementary input stage for rail to rail input operation. . . . . 98
4.22 Transconductance $g_{mtot}$ of the complementary input stage versus the common-mode input voltage. . . . . 99
4.23 Schematic diagram of the complete rail to rail input OTA. . . . . 100
4.24 Post-layout simulation showing the frequency response of the rail to rail input OTA. . . . . 101

4.25 Frequency response of the rail to rail amplifier showing the results at the nominal corner and the worst identified corner. . . . . 102
4.26 Post-layout simulation showing the variation of $g_{mtot}$ versus the input common mode voltage. . . . . 103
4.27 Post-layout simulation showing the variation of DC open-loop gain versus the input common mode voltage. . . . . 104
4.28 Layout of the charge pump and loop filter with rail to rail OTA and biasing circuits. . . . . 104
4.29 Post-layout dc simulation showing the variation of the charging and discharging currents of the charge pump versus the control voltage variation at the loop filter output. . . . . 105
4.30 Layout of the complete multi-phase clock generator DLL. . . . . 105
4.31 Post-layout simulation results showing the transient response of the reference clock and delayed clock; (a) transient simulation showing the misaligned reference clock and the feedback clock (output from tap 10) after start up; (b) fully aligned clocks after DLL achieved locked state. . . . . 106
4.32 Transient simulation showing the coarse and fine control voltages of the DLL. 107
4.33 Post-layout transient simulation showing the control voltage response for a frequency jump in the reference clock. . . . . 108
4.34 Eye diagram of the DLL. . . . . 108
4.35 Transient simulation showing the output of the HV driver after applying the delays. Each HV driver channel is separated by the DLL delay of 5 ns. . . . 110
4.36 Transient simulation showing the output of the HV driver after applying the coarse timing delays. . . . . 111
4.37 Simulation showing the triggering operation of the beamforming block. . . 112

# List of tables


3.1 6 bit clock division . . . . . 30
3.2 Measured performance parameter of the HV pulser circuit compared with prior art . . . . . 33
3.3 Performance parameters of the low side linear regulator. . . . . 45
3.4 Dynamic range of the TIA for different gain setting. . . . . 56
3.5 Performance parameters of the super source follower . . . . . 62
3.6 Measured performance parameter of the TIA circuit compared with prior art 64
3.7 Design values for the BGR circuit . . . . . 67
3.8 System level comparison with state of the art . . . . . 71
3.9 Parameters of the CMUT used for testing . . . . . 72
3.10 Parameters of the CMUT used for fluid testing . . . . . 74

4.1 Design specifications for the rail to rail amplifier and the charge pump loop 97
4.2 Performance parameters of the DLL . . . . . 108

# List of Acronyms

| | |
|---|---|
| **ac** | Alternating Current |
| **ASIC** | Application Specific Integrated Circuit |
| **BCD** | Bipolar CMOS DMOS |
| **BGR** | Bandgap Reference |
| **BIST** | Built in Self Test |
| **BOX** | Buried Oxide |
| **BW** | Bandwidth |
| **CBF** | Current Boosting Factor |
| **CDR** | Clock and Data Recovery |
| **CG** | Common Gate |
| **CMRR** | Common Mode Rejection Ratio |
| **CMUT** | Capacitive Micromachined Ultrasonic Transducer |
| **CP** | Charge Pump |
| **CS** | Common Source |
| **CSPD** | Current Steering Phase Detector |
| **CTAT** | Complementary to Absolute Temperature |
| **dc** | Direct Current |
| **DC** | Delay Cell |

**DLL** Delay Locked Loop

**DTI** Deep Trench Isolation

**FFT** Fast Fourier Transform

**FOM** Figure of Merit

**FPGA** Field Programmable Gate Array

**GBW** Gain Bandwidth

**HIFU** High Intensity Focused Ultrasound

**HS** High Side

**HV** High Voltage

**HW** Handle Wafer

**IC** Integrated Circuit

**ICE** Intra-cardiac Echocardiography

**ICMR** Input Common-mode Range

**IVUS** Intra-vascular Ultrasound

**KCL** Kirchhoff's Current Law

**LDO** Low-dropout Linear Regulator

**LF** Loop Filter

**LNA** Low Noise Amplifier

**LPF** Low Pass Filter

**LS** Low Side

**LV** Low Voltage

**MEMS** Micro-electromechanical Systems

**MOSFET** Metal Oxide Semicondcutor Field Effect Transistor

**MUT** Micromachined Ultrasonic Transducers

| | |
|---|---|
| **MUX** | Multiplexer |
| **NDE** | Non-destructive Evaluation |
| **NMOS** | n-channel MOSFET |
| **OTA** | Operational Transconductance Amplifier |
| **PCB** | Printed Circuit Board |
| **PD** | Phase Detector |
| **PFD** | Phase Frequency Detector |
| **PLL** | Phase Locked Loop |
| **PMOS** | p-channel MOSFET |
| **PSS** | Periodic Steady State |
| **PTAT** | Proportional to Absolute Temperature |
| **PZT** | Lead Zirconate Titanate |
| **RDL** | Replica Delay Line |
| **RGC** | Regulated Gate Cascode |
| **RX** | Receive |
| **SPI** | Serial Peripheral Interface |
| **SR** | Slew Rate |
| **SSF** | Super Source Follower |
| **SOI** | Silicon on Insulator |
| **SONAR** | Sound Navigation and Ranging |
| **TGC** | Time Gain Compensation |
| **TIA** | Transimpedance Amplifier |
| **TX** | Transmit |
| **QFG** | Quasi Floating Gate |

**QFN** Quad Flat No Leads

**VCDL** Voltage Controlled Delay Line

**VCO** Voltage Controlled Oscillator

**VDE** Variable Delay Element

# List of Symbols

| | |
|---|---|
| $\beta$ | Feedback factor |
| $\mu_n$ | Mobility of electrons |
| $\mu_p$ | Mobility of holes |
| $\Omega$ | Unit of resistance |
| $\tau$ | Time constant of a circuit |
| $C_{ox}^{'}$ | Oxide capacitance per unit area of a MOSFET |
| $f_{-3dB}$ | -3 dB bandwidth |
| $g_m$ | Transconductance of a MOSFET |
| $g_{mb}$ | Body transconductance of a MOSFET |
| $k$ | Boltzmann constant |
| $r_o$ | Small-signal output resistance of a MOSFET |
| $V_{\text{bias}}$ | DC bias voltage on the CMUT |
| $V_{\text{BSmax}}$ | Maximum bulk-source voltage of a MOSFET |
| $V_{\text{DSmax}}$ | Maximum drain-source voltage of a MOSFET |
| $V_{\text{GSmax}}$ | Maximum gate-source voltage of a MOSFET |
| $V_{\text{pp}}$ | Peak to peak voltage |
| $V_{\text{th}}$ | Threshold voltage of the MOSFET |
| $\varepsilon$ | Dielectric constant |

| | |
|---|---|
| $\omega$ | Angular frequency |
| $\phi$ | Phase of the input signal |
| $A$ | Ampere |
| $F$ | Farad |
| dB | Decibel |
| kHz | Kilohertz |
| MHz | Megahertz |

# Chapter 1

# Introduction

Ultrasound refers to signals whose frequency range are above the audible range of 20 kHz. Ultrasound based imaging systems have been widely used for medical, industrial, automotive and consumer applications for decades. Ultrasound is also used by animals in the nature. A very well known example is that of bats. Bats emit ultrasound signals and when these signals strike an obstacle and bounce back, the bats use this information to locate the obstacle. Certain marine animals like Killer whale and dolphins use ultrasound for orientation and find their prey. This process is called echolocation or bio sonar. SONAR ( Sound Navigation and Ranging) was the first reported use of sound by humans. In 1826, Jean- Daniel Colladon, used an under water bell to measure the speed of sound in water in Lake of Geneva [1]. Based on this research, Colladon established a method to communicate between ships using acoustic signals and measure depth of sea using echo.

The discovery of piezoelectric effect pushed forward the practical use of ultrasound in medical and industry. The most commonly used applications for ultrasound are in the areas of medical imaging, non-destructive evaluation (NDE) in industry, automotive parking sensors, fluid flow measurements, robotics and high frequency ultrasonic probes for diagnosis and therapy. Based on applications, the frequency of the ultrasound can vary from a few kHz to few tens of MHz. Generally, for air based applications like range finding or distance measurement, few hundreds of kHz are used and for applications that require high resolution, ultrasound in MHz range is used. Some of the applications which require ultrasound in MHz range are high intensity focused ultrasound (HIFU), catheter based applications such as Intravascular ultrasound imaging (IVUS) and Intra-cardiac echocardiography (ICE) and doppler ultrasound.

Conventionally, a piezo ceramic based transducer is used to generate the ultrasonic waves. A cross-section view of such a piezoelectric transducer is shown in Fig. 1.1. A piezoelectric material layer (usually lead zirconate titanate (PZT)) is placed between two electrodes. The

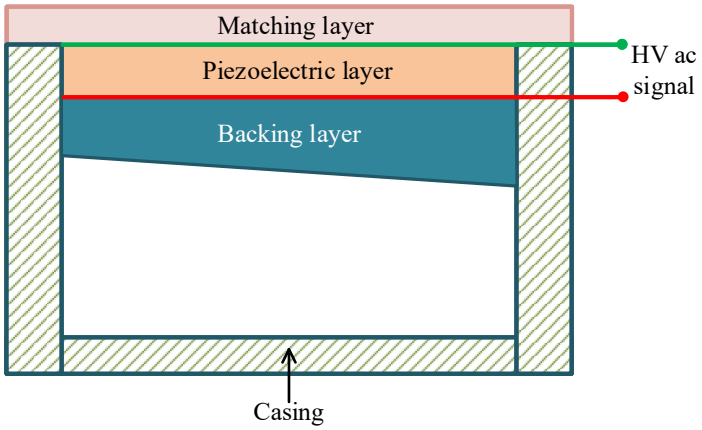



Fig. 1.1 Cross section view of a conventionally used bulk piezoelectric transducer.

resonant frequency of the transducer depends directly on the thickness of this layer. Precise deposition of a thin piezoelectric layer is required for the design of a high frequency ultrasonic transducer [2]. This is a complex and expensive process. Ultrasound can be emitted to and detected from the target located in solid, liquid or a gaseous coupling medium depending on the application. This coupling medium presents an impedance mismatch to the transducer. Especially, when used in fluids, this mismatch is quite large that impacts the performance of the transducer greatly. For example, when these piezoelectric based transducers are used in air, the mismatch in impedance is of the order of $10^5$ which results in a large attenuation of ultrasound signals in air i.e. poor efficiency and also leads to narrow bandwidth operation of the transducers. The impedance of piezoelectric layer is $35{\times}10^6$ kg s/m$^2$ and that of air is 400 kg s/m$^2$. Due to the large mismatch between the acoustic impedance of the piezoelectric layer and the medium (air, water etc), a matching layer is provided between piezoelectric layer and the medium. Placing such a layer lowers the acoustic energy transmitted to the medium and also reduces the bandwidth. Also, depositing a matching layer with precise thickness for high frequency operation is a very challenging process step in the manufacturing of high frequency tranducers [3]. Some other drawbacks of the piezoelectric transducers are manifested by the fact that their operating frequency span is directly related to the size. For high frequency operation, this leads to impractical design requirements. Also, piezoelectric transducers are limited in the operating temperature as they depole at relatively low temperatures [4].

## 1.1 Motivation and research objective

Micromachined Ultrasound Transducers (MUTs) have emerged as an alternative to the conventional ultrasonic transducer over the past decades. Capacitive Micromachined Ultrasonic

Transducer (CMUT) was invented in 1990s as an electrostatic based transducer for airborne applications with operating frequencies in the MHz range [5]. These transducers overcome most of the drawbacks of the conventional piezoelectric transducers in terms of bandwidth, sensitivity and transduction efficiency. Airborne ultrasound has wide variety of applications like high resolution short distance sensing in robotics, range finding, non-destructive evaluation (NDE) and flow measurement. As the frequency of these transducers increases, the resolution increases. The limitation of conventional transducers for airborne applications due to impedance mismatch issues was described in the previous section. The CMUTs also exhibit a wide bandwidth operation in immersion applications as well. Advancements in micromachining techniques enabled the design and manufacture of miniaturized CMUTs with precisely controlled performance parameters. One of the biggest advantages of the CMUTs is its CMOS compatibility. This enables very close integration possibilities with the interface electronics. CMOS compatibility opens up the doors for a monolithic integration of CMUT and CMOS on the same wafer. Thanks to the manufacturing techniques, CMUTs inherit the advantages like batch fabrication and scalability.

A basic cross section view of the CMUT is shown in Fig. 1.2. CMUT consist of a flexible membrane suspended over a thin gap. Insulation posts are provided to support the membrane over the silicon substrate at the bottom. The thin gap can be air filled or can be vacuum sealed. Metal electrodes are provided at the membrane on the top and the substrate at the bottom. This makes the CMUT essentially a miniaturized parallel plate capacitor with a top plate (membrane) and bottom plate (substrate). This constitutes one CMUT cell. Generally, multiple such structures are connected in parallel to form a CMUT element. CMUTs are used as both ultrasonic transmitters and receivers. To use them as transmitters, electrostatic force is applied on the membrane to cause it to vibrate with an alternating voltage. The vibration of the membrane generates ultrasound waves in the medium in which it is being used. In the receive mode, acoustic signals impinge on the CMUT membrane causing it to vibrate. These vibrations modulate the capacitance of the element which is then detected using a read-out circuit. In order to have an electro-mechanical coupling coefficient comparable to that of piezo based transducer, it is required to have a very high electric field in the cavity. This should be in the order of $1{\times}10^8\,\mathrm{V\,m^{-1}}$ or higher [6]. The advancements in MEMS technology have enabled manufacturing of such narrow vacuum gaps with high precision. This is crucial to generate sufficient ultrasonic power in the medium. The height of the gap in-fact determines the ability of a particular CMUT to function as a transmitter or receiver. For example, a good transmitter should be able to generate a large acoustic power into the coupling medium. In order to do this, the membrane should be able to swing very wide under the applied voltage. A large gap enables this. However, a good receiver must have a narrow

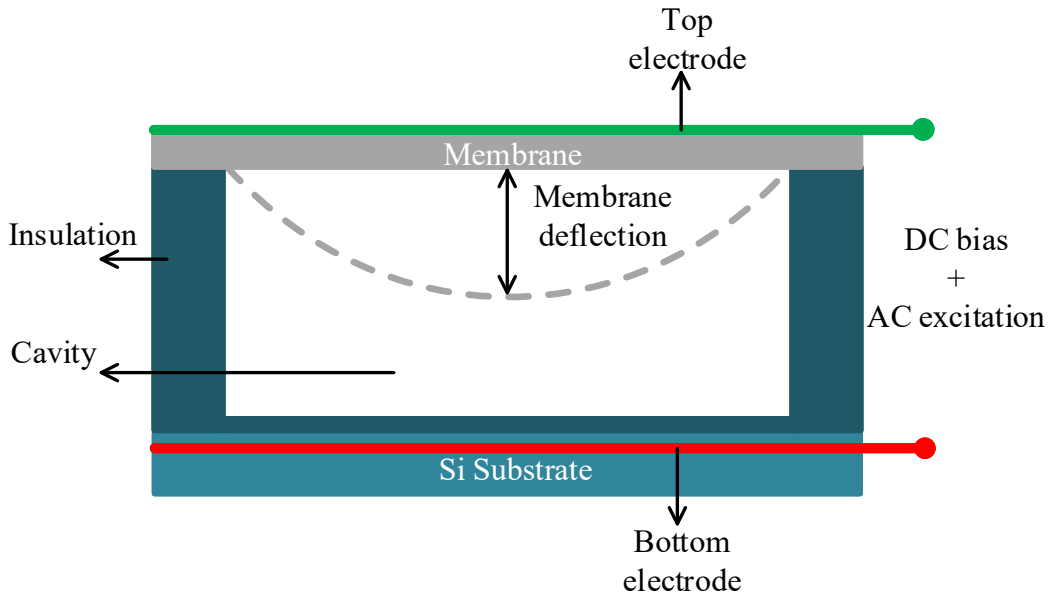



Fig. 1.2 Cross section view of a Capacitive Micromachined Ultrasonic Transducer (CMUT).

gap for maximum sensitivity. When the reflected acoustic waves impinge the membrane, a small vibration should be able to generate a large capacitance change and hence a large current generation should be possible.

For operation of the CMUT, a voltage $V$ is applied across it, resulting in the deflection of the membrane towards the silicon substrate. The mechanical restoring force of the membrane counter balances this electrostatic force [7]. The force experienced by the membrane can be written as given in [5]:

$$F = \frac{1}{2}\varepsilon A\frac{V^2}{d^2} \tag{1.1}$$

where $\varepsilon$ is the dielectric constant of the material in between the two plates, $A$ is the surface area of the plates, $d$ is the gap between the plates and $V$ is the applied voltage. As it can be seen from the equation 1.1, the force experienced by the parallel plate CMUT varies quadratically with the applied voltage causing the second harmonic to be generated [5]. To operate the CMUT with the first harmonic of the applied voltage, a dc bias voltage is first applied on the CMUT, and then an ac voltage is superimposed over it so that the total voltage applied across the CMUT is given by:

$$V(t) = V_{bias} + V_{ac}cos(\omega t + \phi) \tag{1.2}$$

If we make the bias voltage much larger than the ac voltage, the time varying electrostatic force varies linearly with the applied ac voltage and can be written as:

$$F(t) = \frac{\varepsilon A V_{bias} V_{ac}}{d^2} cos(\omega t + \phi) \tag{1.3}$$

It can be said that applying the bias voltage helps to linearize the force. Further, the receive sensitivity of the CMUTs increases due to the spring softening effect [8]. Due to the applied bias voltage, the top CMUT membrane moves closer to the substrate. This makes the device more sensitive to any membrane displacement when an external acoustic force is applied to it. This improves the CMUT performance in the receive mode. When the bias voltage is increased further, the membrane deflection also increases. At a certain voltage, the mechanical restoring force will not be able to counter balance the electrostatic force and the membrane collapses to the substrate. This voltage is called the collapse voltage or pull-in voltage [7]. It was reported in literature [4], [9] and [10] that the CMUTs should be biased close to their collapse voltage to maximize the transduction efficiency. Conventionally, an external RC bias tee circuit is implemented to apply the desired HV dc bias voltage to the CMUT. It has to be made sure that the sum of the dc and ac voltage does not go beyond the collapse voltage of the CMUT.

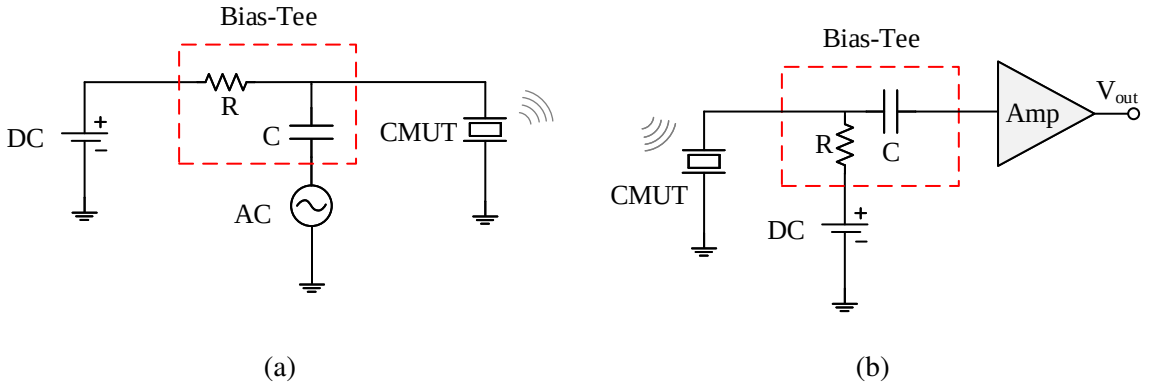



Fig. 1.3 (a) Circuit used to interface the CMUT when operated as an ultrasound transmitter; (b) Circuit interface for the CMUT when used as an ultrasound receiver.

To operate the CMUT in the transmit mode, the circuit shown in Fig. 1.3a is used conventionally. The bias tee circuit is shown in the red dotted box. As it can be seen, the ac voltage is superimposed over the dc bias to actuate the CMUT to generate the ultrasound waves. The receive mode operation of the CMUT is enabled using the electrical circuit interface shown in Fig. 1.3b. The dc bias needs to be applied for the proper operation of the CMUT as explained above. The ac drive is removed now. A pre-amplifier circuit is now connected in the receive path to which the signals generated by the CMUT are ac coupled.

This thesis aims to address the following problems:

- Investigate circuit architectures to design a CMUT transceiver system which eliminates the need to use an external HV bias tee circuit to the CMUT. The R and C in the bias tee are quite large value components, hence from a cost effective point of view it is not practical to integrate it on chip.
- As explained earlier, the receive sensitivity is optimum when the CMUTs are biased close to their pull-in voltage. With the standard driving circuit as shown in Fig. 1.3, the dc and ac voltages combined should be below the maximum allowed voltage of the CMUT. This results in a dc bias voltage which is much lower than the pull-in voltage. Hence, the interface circuit should be capable of maximizing the CMUT transduction sensitivity.
- Eliminate the high voltage isolation switch in the receive path in order to improve the receiver noise performance and lower the chip area.
- Design of a low power transmit beamforming circuit which is integrated as a single chip solution with the transceiver chip.

# Chapter 2

# Ultrasound System

## 2.1 Conventional CMUT driving architecture

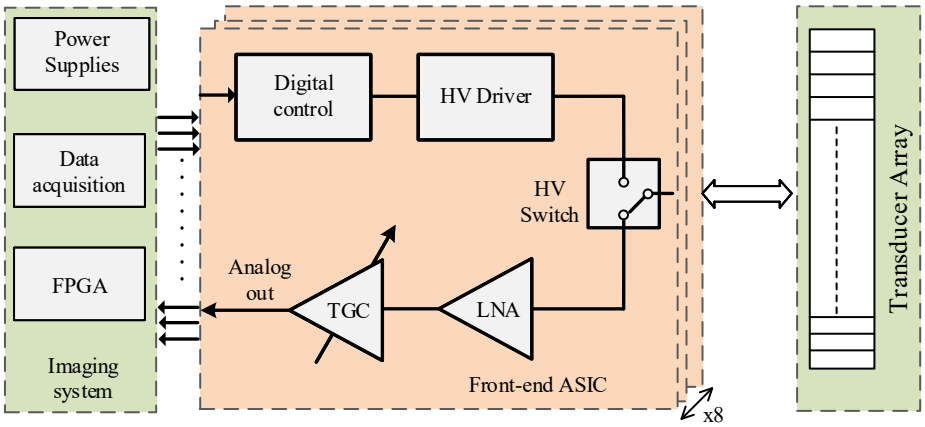



Fig. 2.1 A conventional block diagram of ultrasound based system.

A CMUT can be used as a transmitter, receiver or both depending on the desired operation. In the pitch-catch mode of ultrasound operation, one transducer is used as a transmitter of the acoustic signals and another transducer is used solely as a receiver. In the pulse-echo mode of operation, a single transducer is used as both transmitter and receiver. Most often, a pulse echo mode of operation is desired to reduce the element count. A block diagram of a conventional multi-channel ultrasonic imaging system used for pulse-echo mode of operation is shown in Fig. 2.1. Here an 8 channel front-end application specific integrated circuit (ASIC) interfaces a CMUT array. The back-end imaging system provides the required low voltage and HV power supply signals, control signals and the necessary signal processing operation of the received signals are carried out. As the ASIC contains circuit blocks for

performing both the transmit and receive operation, it can be called an ultrasound transceiver ASIC.

The transmit path of the ASIC consist of the HV driver/pulser circuit which generates the necessary HV ac signals at the desired frequency that are applied to the CMUT. A digital control block provides the low voltage control signals to the driver circuit. A HV switch is used to isolate the low voltage transistors in the receive signal chain from the HV signals. This switch is appropriately controlled to change from the transmit to the receive phase. In the receive path, a low noise pre-amplifier is used to amplify the signals generated by the incident ultrasonic waves. As CMUTs are high impedance sensors, a transimpedance amplifier (TIA) will be used to pre-amplify the signals. This is sometimes followed by a time gain compensation circuit (TGC) which adjusts its gain with time. In this thesis, the TGC circuit is not implemented.

Fig. 2.2 shows the interface circuit architecture for a single CMUT element to perform a pulse-echo operation in the conventional way. It is desired to keep one end of the CMUT (the one that faces the user) at ground or at low voltage for safety purpose. The HV dc bias voltage is applied through an RC bias tee circuit. This is basically a low-pass filter. The pulses from the HV pulser circuit is ac coupled through the HV capacitor during the transmit phase. The corresponding pulse waveforms can be seen in the figure. The transmit-receive (TX-RX) switch can be implemented with a HV MOS transistor. As shown in the figure the HV MOSFET will be represented with a thick drain terminal in the rest of this thesis. These devices have a higher $V_{DSmax}$ and $V_{BSmax}$, however the $V_{GSmax}$ is restricted to the standard low voltage digital levels. Appropriate control signals should be applied to the TX-RX switch. In the receive phase, the HV switch is closed to receive the current signals which are generated by the CMUT when the echos cause the membrane to vibrate thereby modulating the CMUT capacitance. The HV output of the pulser is kept at a high impedance state.

## 2.2 Proposed CMUT driving architecture

As can be seen from the previous section, an RC bias tee is required to apply the necessary bias voltage to the CMUT. The resistor and capacitor values required are large which makes it impractical from a cost-effective point of view to integrate them on chip. It is desired to have a closely integrated sensor solution with the CMUT and electronics to make it possible to develop portable ultrasonic imaging systems. Further, improvement in signal to noise ratio also facilitates better imaging capabilities. For such closely integrated systems, eliminating the off-chip components should be a priority. Especially in applications like ICE and IVUS, in-probe ASICs are used which require reduced cable count and external

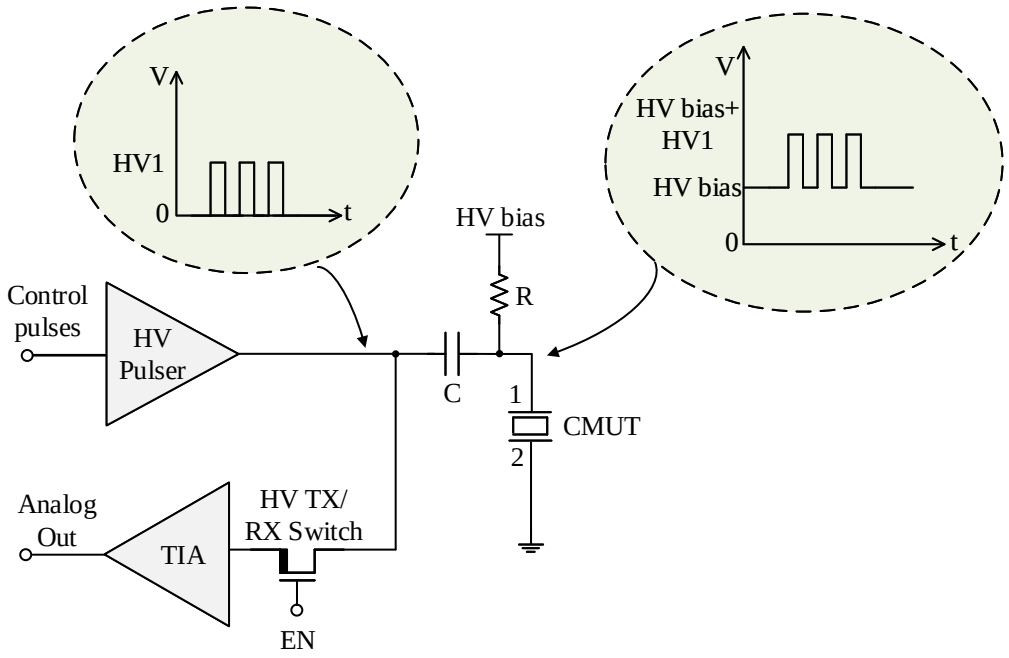



Fig. 2.2 A conventionally used driving structure for a pulse-echo operation.

components [11] [12]. Further, with the driving structure shown in Fig. 2.2, the total voltage applied to the CMUT (dc bias + ac) should be below the collapse voltage of the CMUT. It has been demonstrated that the electro-mechanical coupling efficiency is optimum when the CMUTs are biased close to their collapse voltage [10] [7]. For maximum transmit efficiency, an ac signal is superimposed over a HV bias making sure that the sum does not drive the CMUT into collapse mode. However, in the receive mode, only the dc voltage is applied to the CMUT and this is much lower than the optimum point. For the interfacing structure shown in Fig. 2.2, this results in a receive sensitivity which is reduced. In [13], an on-chip adaptive biasing scheme was implemented to boost the receive sensitivity. An adaptive dc voltage will be added to the existing dc bias to take total voltage close to the collapse voltage. This approach is however not very area efficient as additional circuit blocks like on chip DC-DC converters are needed.

In this thesis, a novel interfacing architecture is proposed that eliminates the need to have an external bias tee circuit for dc biasing as well as improve the receive sensitivity of the CMUT. The proposed structure can be seen in Fig. 2.3. A two-level pulsing scheme is used where the HV pulser switches between two high voltage levels HV1 and HV2 during the transmit phase. This is equivalent to applying a HV dc and superimposing an ac signal. In the receive phase, the pulser output is pulled to the higher of the two high voltage levels. By choosing the HV1 close to the collapse voltage of the CMUT, it is possible to operate the transducer at its optimum electro-mechanical coupling efficiency in the receive mode.

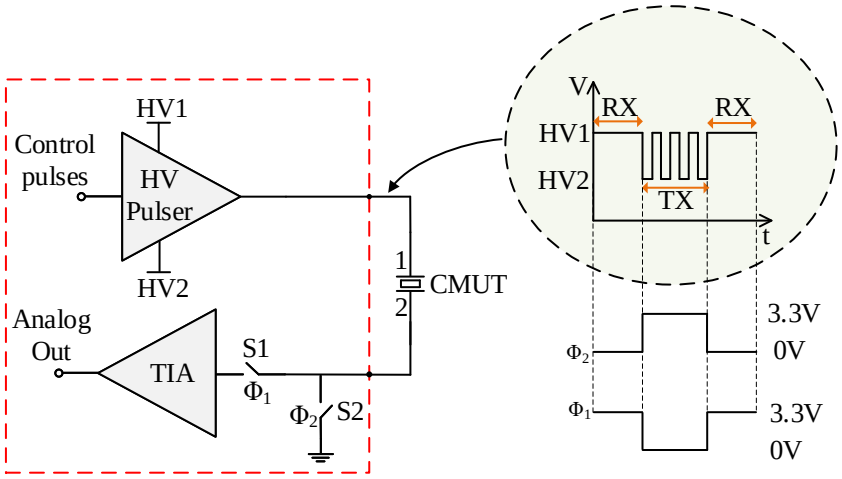



Fig. 2.3 The proposed transmit-receive structure for the pulse-echo operation.

Two switches S1 and S2 are provided in the receive path which can be implemented using low voltage MOSFETs. The CMUT acts like an isolator for the receive path from the HV transmit path in this case. The switches are controlled in such a way that during the transmit mode, the switch S2 closes and connects the CMUT electrode 2 to the ground. S1 is kept open during this phase. When the operation is switched to the receive mode, S2 is opened and S1 connects the CMUT terminal to the input of the TIA. The current generated by the CMUT while receiving an echo is then input to the TIA. The CMUT electrode 2 will have a low dc voltage which is set by the bias voltage of the TIA. This ensures that this CMUT terminal will always be at a low voltage or ground and can be safely exposed to the user in a product. This approach helps us to eliminate the use of HV MOSFETs from the receive path. This is beneficial in lowering the silicon area and also lowers the parasitic capacitance at the TIA input which improves the noise performance of the TIA. The phases controlling the switching operation and a representative pulse waveform applied to the CMUT can also be seen from Fig. 2.3.

## 2.3 Ultrasonic Transceiver Chip Architecture

An ultrasonic transceiver chip with transmit beamforming capability has been designed during the framework of this doctoral work. The new driving architecture explained in the previous section enables the integration of the dc biasing on chip. Three versions of the transceiver chip have been designed using a 0.18 µm HV SOI process XT018 from XFAB during the project time frame, each with incremental performance additions. The first two versions of the chip named ProTaktilUS_A0 and ProTaktilUS_B0 are fully characterized.

A block diagram representation of the final ASIC version is shown in Fig. 2.4. The chip is named ProTaktilUS_C0 and is submitted for fabrication.

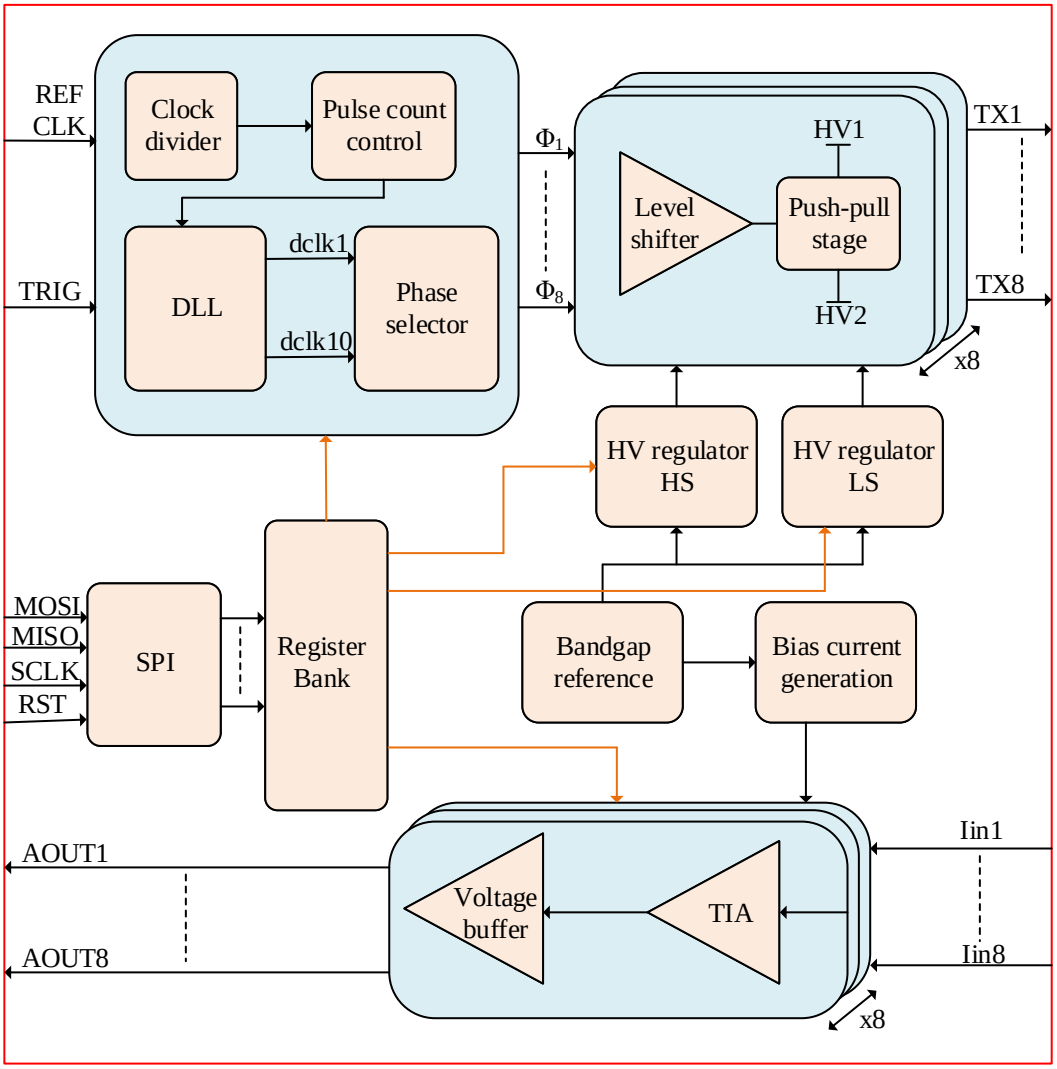



Fig. 2.4 Block diagram representation of the designed CMUT transceiver ASIC.

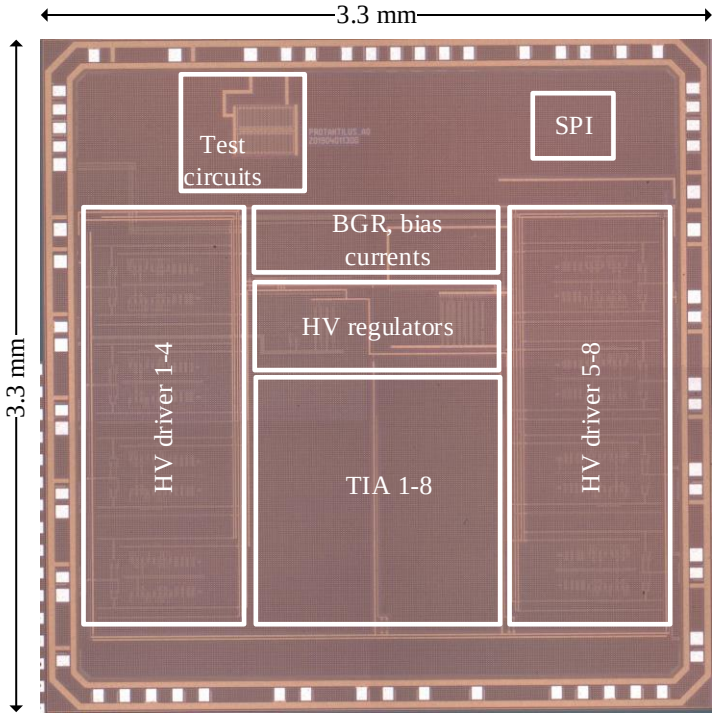



Fig. 2.5 Microphotograph of the ProTaktilUS_A0 chip.

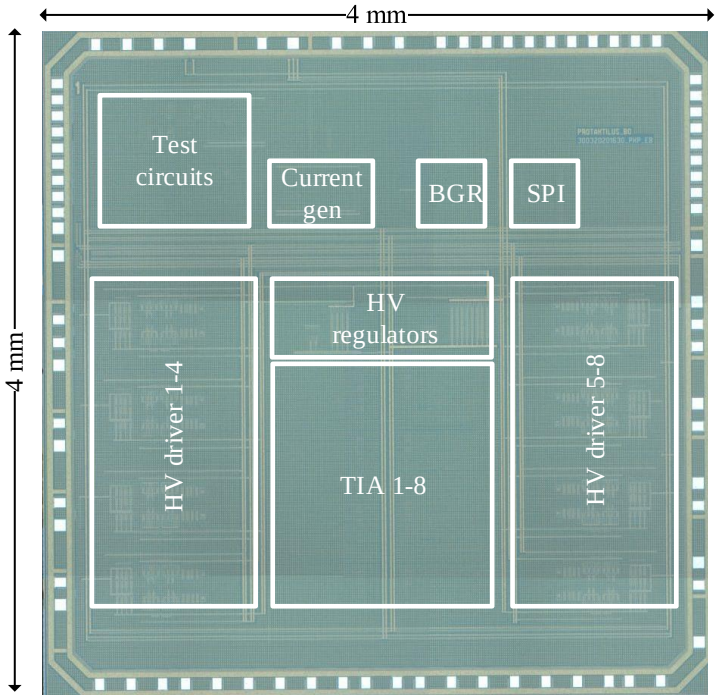



Fig. 2.6 Microphotograph of the ProTaktilUS_B0 chip.

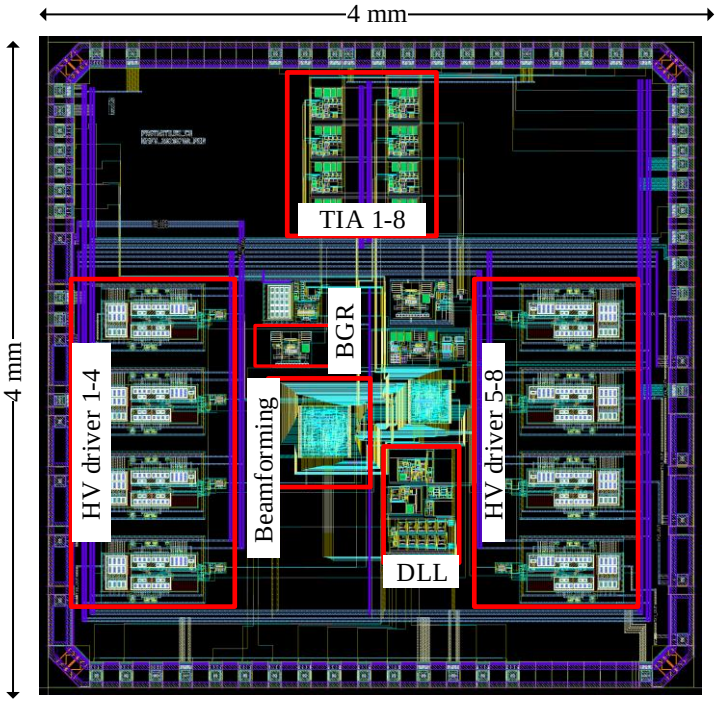



Fig. 2.7 Chip layout of the ProTaktilUS_C0 chip which is under fabrication.

## 2.4 High Voltage Process Technology

Several foundries offer different processes for chip manufacturing. Depending on the project requirements, an appropriate process selection is a key step in the execution of any ASIC design project. In this section, the process used for this work is briefly introduced.

A high voltage CMOS manufacturing process is required for the design of the CMUT transceiver chip. The pulser circuit in the transmit path demands the use of high voltage transistors. As the target voltage requirement for this project is 60 V for the pulser, a technology that supports this voltage level is needed. There are few fabs that offer such high voltage processes. The 0.18 µm high voltage process from XFAB is used for this work. Some of the key desired features for an integrated HV processes are low $R_{on}$, low self heating and faster switching.

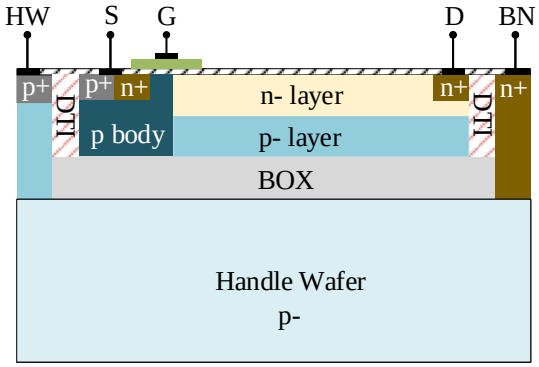



Fig. 2.8 Cross section view of a super junction high voltage NMOS (LNDMOS) transistor [14], [15].

A HV MOS transistors based on partial SOI technology is shown in the Fig. 2.8. Deep Trench Isolation (DTI) is used for lateral isolation of the devices. The lateral super junction formed by horizontal n and p layers in the top silicon which sets the voltage rating of the device. The device consist of a top silicon layer on top of a Buried Oxide (BOX) layer. The SOI diode is reverse biased by connecting the terminals BN (diode cathode) and the HW (anode) to the appropriate high voltage levels. This structure allows for small isolation distance between the devices on the chip. This is very critical for this work where multiple HV and LV ultrasonic channels need to be integrated on the same die. The technology also provides up to 6 metal layers including a thick metal option [16].

For the design of the low voltage circuits, 5 V MOSFETs are used from the process. The transistor symbols used for designs are shown in Fig. 2.9. As it can be seen, the HV MOSFETs are drawn with a thicker drain terminal. This shows the high voltage tolerance of the drain-source terminals. The 100 V devices are used for the design of the HV circuits

in this work. This means that the maximum $|V_{DS}|$ and $|V_{DB}|$ that can be applied across the MOSFETs are 100 V. These transistors have a thin gate oxide like the standard low voltage MOSFETs, hence the maximum $|V_{GS}|$ is 5 V. This helps to achieve better control over the threshold voltage and also they are in the standard $V_{th}$ value. For high gate to source voltages, the transistors must have a thicker gate-oxide. This leads to reduced transconductance and poor threshold voltage control [17]. The bulk terminals are not shown for the HV MOSFETs as they are connected to the source. For the designs used in this thesis, the 5 V MOSFET's bulk is connected to ground and VDD for NMOS and PMOS respectively. Hence, they will not be shown in the schematic explicitly unless they are connected differently.

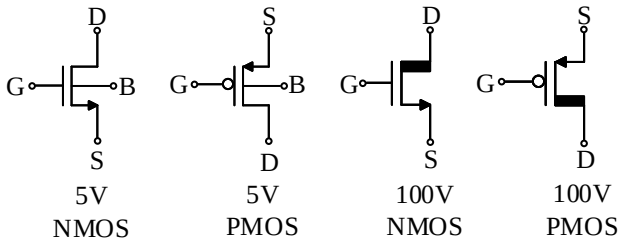



Fig. 2.9 Symbols used for the different MOSFETs used in designs.

# Chapter 3

# Integrated Circuits for CMUT Transceiver Interface

## 3.1 Background

The interface electronics design plays a crucial role in an ultrasound system as much as the transducer design. Conventionally, these electronic circuits are placed in the back-end imaging system which connects to the probe with long coaxial cables. So, each transducer element needs one cable connecting it to the circuits. As explained in the previous chapter, the advancement of CMUTs have enabled the development of large 1D and 2D arrays of CMUTs. In such cases, it is not practical to run long cables from the transducer probe to the imaging system. Also, since the aim is to develop a portable, hand-held ultrasound imaging system, it is imperative that we build a system where the sensor solution consisting of the transducers and interfacing electronics are closely integrated. A hybrid multi-chip solution or a monolithic solution is desired for this. This drives the design of application specific integrated circuits, which has both the high voltage transmitter circuitry and the low voltage receive and other control circuits on the same chip. A low-power, area efficient HV transceiver ASIC with 8 channels is designed in this work with the aim of interfacing an 8 channel CMUT array.

This chapter presents the design of the key circuit blocks of the CMUT interface ASIC. The circuit topology selection and circuit analysis are presented first, then a systematic approach to the design is presented. This is followed with relevant simulation results and finally, the measurement results from the tape-outs are also presented.

## 3.2 High Voltage Transmit Pulser Circuit

As explained in Chapter 2, a two-level HV pulser is one of the most critical block in the transmit path of the CMUT transceiver chip of this thesis. A block diagram representation of the pulser circuit is shown in the Fig. 3.1. The pulser circuit at the core has two high voltage transistors $M_P$ and $M_N$ at the output forming a push-pull stage. The circuit switches between the two high voltage levels $V_{DDH,HS}$ and $V_{SSH,LS}$. These output stage transistors are driven by two level shifters. The level shifter on the high side drives the $M_P$ and the level shifter on the low side drives the $M_N$. The level shifters convert the low voltage control signals ($V_{in,T}$, $V_{in\_n,T}$, $V_{in,B}$ and $V_{in\_n,B}$ ) in the 0 V - 3.3 V domain to the HV levels. The low voltage control signals are generated using a 4 phase non-overlapping clock generator circuit.

Two HV linear regulators form critical circuit blocks in the pulser circuit. The linear regulator on the high side (HV Regulator HS) is basically used to bias the protection transistors in the high side level shifter. The regulator on the low side has a more demanding design requirement. As can be seen from the Fig. 3.1, the low side regulator also serves as the bottom side rail of the transistor $M_N$. During the discharge phase of the CMUT, a large amount of current is discharged through $M_N$. When used for a CMUT array, this rail should be able to sink a large amount of current ($\sim$ few tens of milli-amperes). Hence, a HV linear regulator with high current sink capability is designed for this purpose.

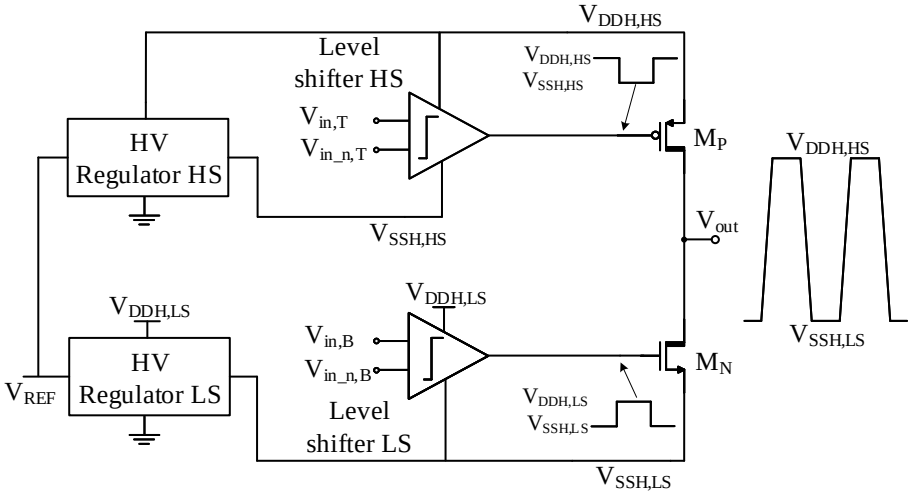



Fig. 3.1 The top-level block diagram of the high voltage pulser circuit.

### 3.2.1 Static level shifter based pulser design

For the design of the HV pulser circuit, different architectures from the literature have been studied. The most common type of the level shifter is based on limiting the $V_{GS}$ by using a diode or a diode connected transistor. In Fig. 3.2, a HV pulser circuit based on a static level shifter can be seen [17] [18]. This is a cross coupled voltage mirror based level shifter from [19]. The voltage mirror structure consist of a HVNMOS M1 with a load formed by a low voltage PMOS M3. M3 is a diode-connected MOSFET whose $V_{GS}$ sets the voltage at node $V_a$. The transistor $M_4$ is a pull-up transistor which makes sure that the node $V_a$ is pulled up to $V_{DDH}$ in the off-state.

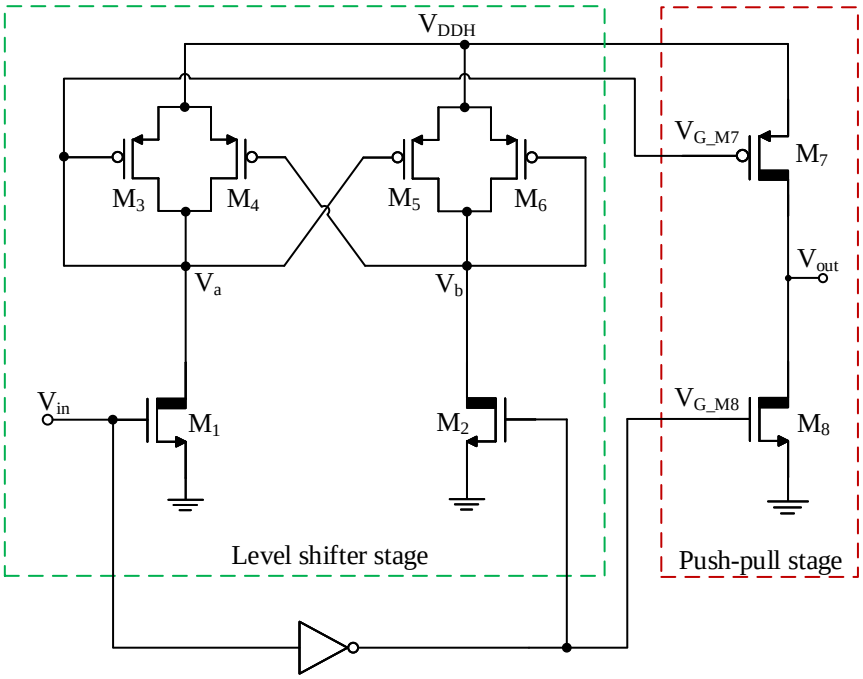



Fig. 3.2 Static level shifter based pulser circuit

The low voltage control signal $V_{in}$ is applied to M1 and M2 is driven by its inverted signal. When $V_{in}$ is high, M1 is turned on and a current is drawn from the HV supply $V_{DDH}$. Depending on the device dimensions, the node $V_a$ will have a voltage given by $V_{DDH} - V_{SG3}$. This level shifted signal is then used to drive the gate of $M_7$ which forms the high-side transistor of the push-pull output stage. The design equations can be derived by equating the current through the transistors. When $M_1$ is turned on by applying a $V_{DD}$, it turns on in saturation (assuming that $V_{DDH} \gg V_{DD}$). By equating the currents through $M_1$ and $M_3$, we can write:

$$\frac{\beta_1}{2}(V_{in} - V_{th1})^2 = \frac{\beta_3}{2}[(V_{DDH} - V_a) - V_{th3}]^2 \tag{3.1}$$

By re-arranging, we get:

$$V_{\mathrm{a}} = V_{\mathrm{DDH}} - \left[\sqrt{\frac{\beta_1}{\beta_3}}\,(V_{\mathrm{in}} - V_{\mathrm{th1}}) + |V_{\mathrm{th3}}|\right] \tag{3.2}$$

where, $\beta 1 = \mu_n.C'_{ox}.\frac{W_1}{L_1}$ and $\beta 3 = \mu_p.C'_{ox}.\frac{W_3}{L_3}$

$\mu_n$: mobility of electrons

$\mu_p$: mobility of holes

$C'_{ox}$:gate oxide capacitance

By properly choosing the aspect ratio of the transistors, the node voltage $V_{\mathrm{a}}$ can be set. It can be made sure that this voltage is within the limits of the gate-oxide breakdown of the technology.

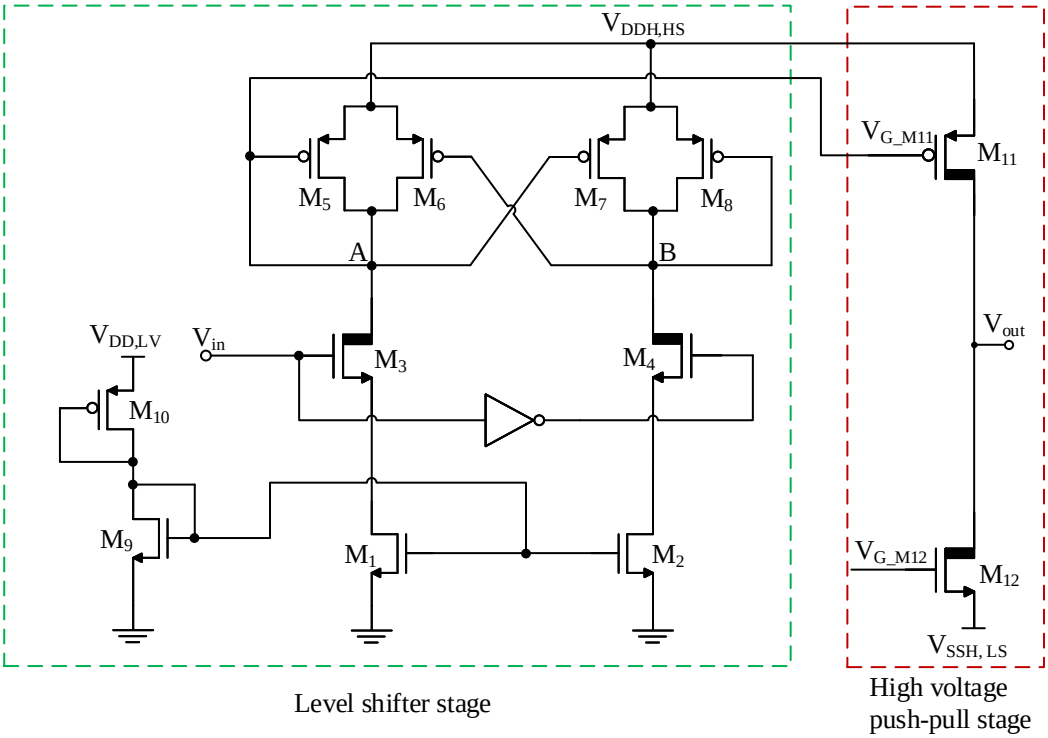



Fig. 3.3 Current limited static level shifter based pulser circuit.

This basic static level shifter based design is one of the most robust and area efficient pulser design, however these have some drawbacks as well. One of the main drawbacks of this circuit is the continuous power dissipation through either side of the level shifter stage. The current drawn is limited by the device dimensions which is in turn set by the node voltage $V_{\mathrm{a}}$. A few milli-amperes of current drawn from the high voltage supply $V_{\mathrm{DDH}}$ can lead to a large power dissipation. This is not acceptable for a portable system where

power consumption is a very crucial parameter. An improved current-limited static level shifter based pulser circuit is shown in Fig. 3.3. Here a current limit is introduced by using the transistors $M_9$, $M_1$ and $M_2$. The diode connected load $M_{10}$ sets the current through the current mirrors. The bottom side transistor $M_{12}$ is driven by an identical level shifter. For clarity and ease of explanation, only the high side level shifter is shown here.

The two-level pulser circuit based on the static level shifter is designed for the HV levels of 60 V to 10 V switching. The simulation results are shown in Fig. 3.4, 3.5 and 3.6.

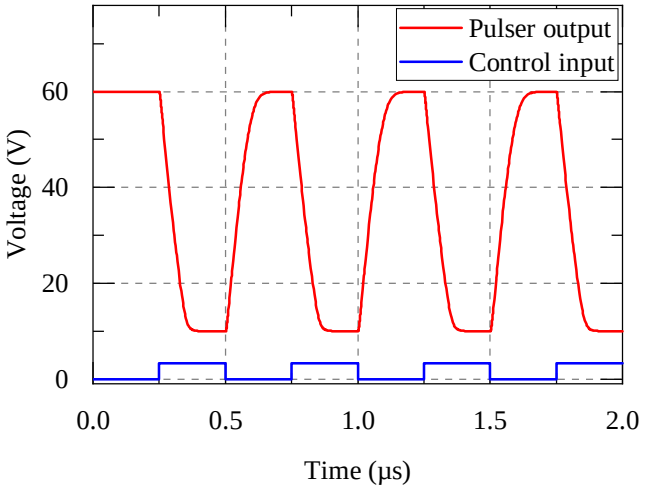



Fig. 3.4 High voltage output of the pulser circuit.

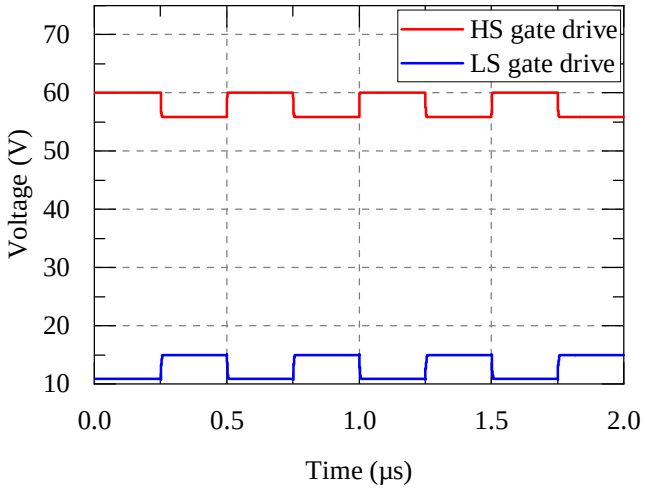



Fig. 3.5 Gate drive signals of the push-pull stage.

The high voltage output of the pulser circuit is shown in Fig. 3.4. As it can be seen, the pulser output switches between the voltage levels 60 V and 10 V. The low voltage control signal is applied at a frequency of 2 MHz. From Fig. 3.5, the gate drive signals of the output push-pull stage can be seen. This is in fact the output of the two level shifters. The high-side

(HS) gate drive signal switches between 60 V and ∽ 55 V. This ensures that the $V_{SG}$ of $M_{11}$ is below its $V_{SGmax}$ (which is 5.5 V in this technology). For the low-side (LS), another level shifter up-shifts the low voltage control signal to 15 V to ∽ 10 V range. Fig. 3.6 shows the current pulses through the transistors $M_1$ and $M_2$. It can be seen that there is a continuous current consumption of around 480 µA during each half cycle through either branch from the 60 V supply. This amounts to an average power consumption of 36 mW of power per pulser. For a large CMUT array, this leads to a large power budget and heating problems. The power consumption is reduced significantly with this architecture as compared to the basic static level shifter. However, the input to output delay increases with this. Hence, it is not possible to lower the currents to very low values as it affects the switching speed considerably. So, a low power architecture is desired.

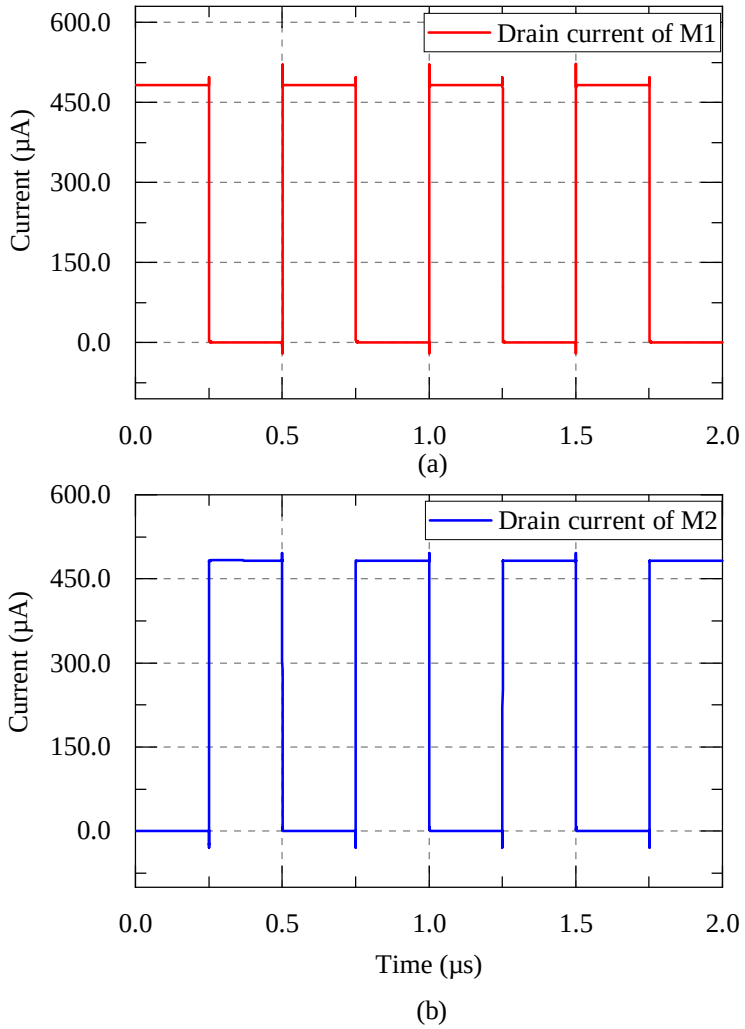



Fig. 3.6 Current through transistors $M_1$ and $M_2$.

### 3.2.2 Gate charge recycled level shifter based pulser

A low power level shifter architecture for driving the high side switch in a DC-DC converter of an implantable device was presented in [20]. The similar approach was previously presented for HV display driver design in [21] [22]. Power consumption from the HV rail is minimized using a gate charge recycling technique. The schematic of the gate charge recycled level shifter based pulser circuit is shown in Fig. 3.7. This is a slight modification from what is presented in [21]. Low voltage current limiting transistors $M_1$, $M_2$ and $M_9$ limit the current consumed during each cycle.

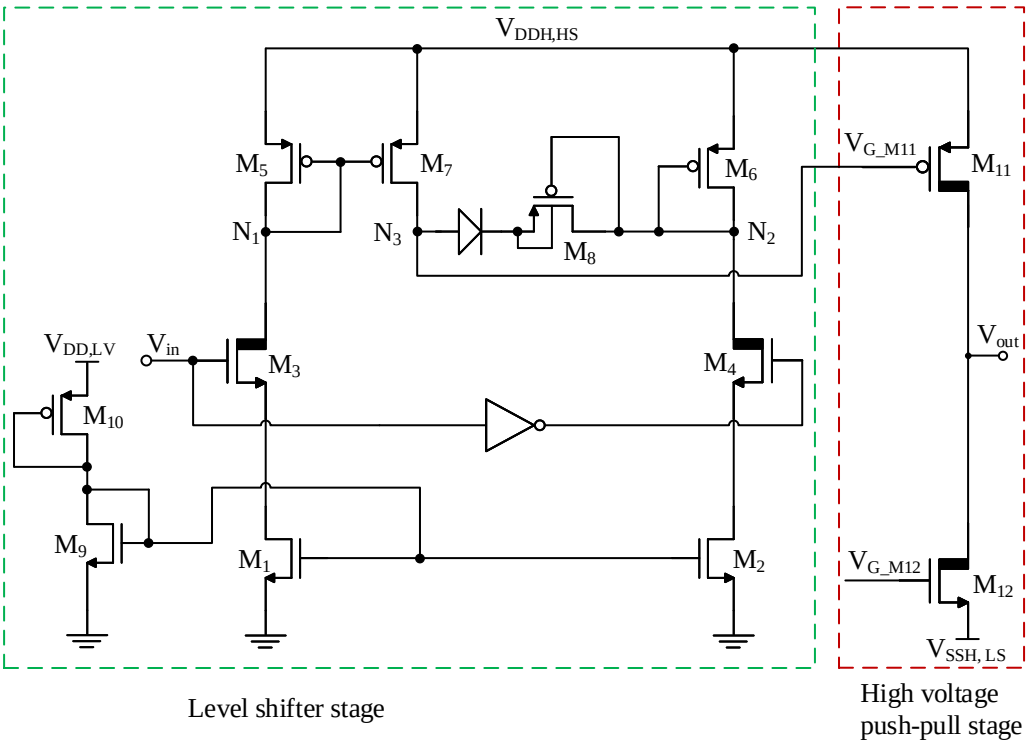



Fig. 3.7 Gate charge recycled level shifter based pulser circuit.

An edge detector circuit (not shown in the schematic) is used to generate short duration pulses that are applied at the input HV MOSFETs $M_3$ and $M_4$. When $V_{in}$ is HIGH (3.3 V), $M_5$ is turned ON. This turns $M_7$ also ON which pulls the node $N_3$ to $V_{DDH,HS}$. This turns the high side push-pull MOSFET $M_{11}$ OFF. Once $V_{in}$ goes LOW, $M_5$ and $M_7$ turns OFF. Also $M_4$ is OFF which causes the node $N_3$ to be electrically isolated and it retains its previous charge which is stored in the parasitic gate capacitance of $M_{11}$.

When we have a HIGH pulse at the gate of $M_4$ and $M_3$ stays LOW, a current flows through the diode connected transistor $M_6$. The node $N_3$ is discharged through $M_8$ and this turns ON $M_{11}$. Once the control signal at the gate of $M_4$ goes LOW, $M_4$ and $M_6$ turns OFF. Since $M_7$ is also OFF the node $N_3$ is isolated and retains the gate charge of $M_{11}$. This way,

we can make sure that the level shifting operation is performed and there is no continuous power drawn from the HV supply. There is a current consumtion only as long as the input pulses at the gates of $M_3$ and $M_4$ are HIGH. This can be controlled to make very short pulses at the input. Similar to the previous section, the low side level shifter is not shown here. An identical level shifter is used to drive the low side transistor $M_{12}$ of the push-pull stage. The circuit has been designed and simulations are performed to verify the design.

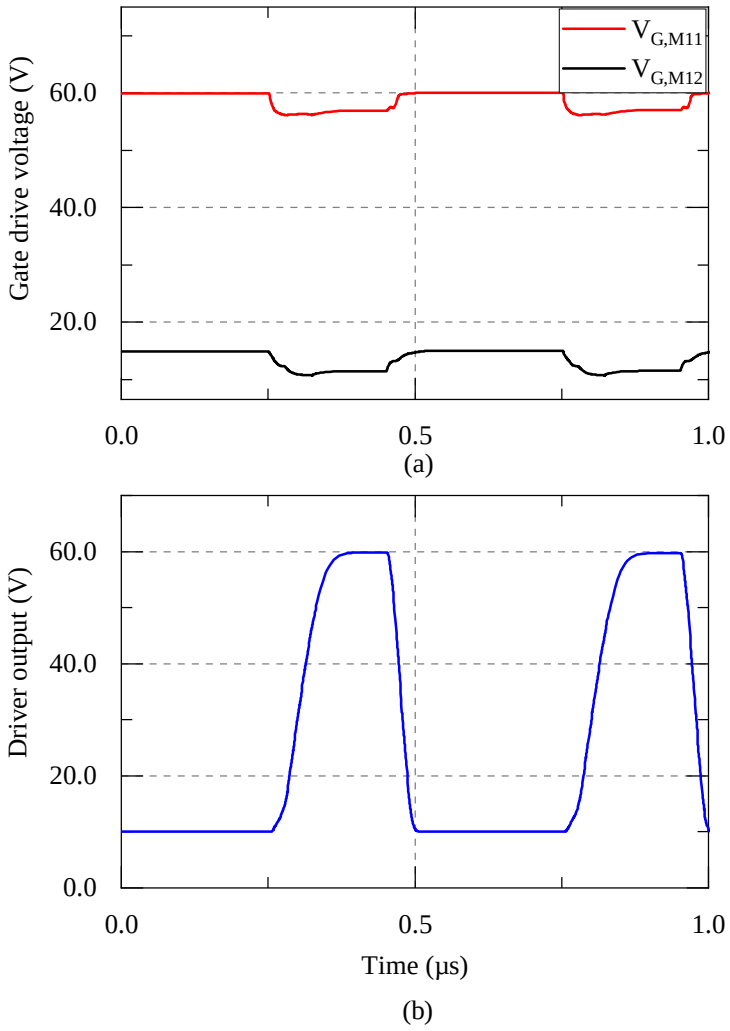



Fig. 3.8 (a) Simulation results showing gate drive signal of the low-side and high-side; (b) Output of the pulser circuit.

It can be seen from the simulation results in Fig. 3.9, that the circuit draws current from the HV supply on as long as the control input stays high. For the design used here, the pulses are 250 ns wide. A current of roughly 50 µA is drawn. From Fig. 3.8, the level shifted gate drive voltages can be seen. The transistor $M_6$ can be sized appropriately to limit this voltage within the safe operating region. The charge on the gate is reset when a high pulse

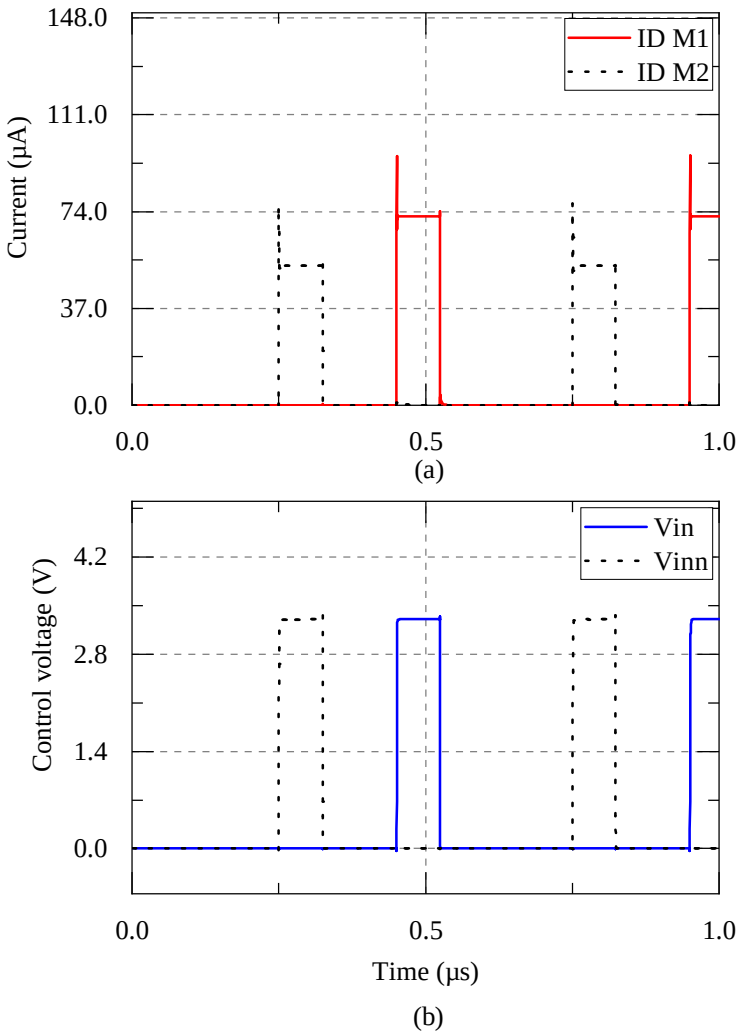



Fig. 3.9 (a) Currents through the transistors $M_1$ and $M_2$; (b) Input control signals.

appears on the other input leg. Using this architecture, it is possible to reduce the power consumption by roughly 3/4th as compared to the static current limited level shifter presented in section 3.2.1. However from simulations, it is observed that even though this topology lowers the power consumption compared to the static level shifter topology, there are certain drawbacks. It can be observed from the Fig. 3.8, the output of the pulser circuit has a large rise and fall times. The gate drive signals does not have a sharp rising and falling edge. Also, from corner simulation it is observed that it is difficult to make this circuit reliable across PVT variations. This could be due to the fact that the circuit works based on the charge storage and recycling using the parasitic capacitance at a node. Large deviation in the gate drive signals are observed across process corners. This is unacceptable for a reliable ASIC design. Also, it can be expected that with multiple such channels present on a chip, there is a possibility that during a large HV swing on another channel, a small cross coupling effect

could produce an unacceptable behavour in a neighboring channel. Hence a more reliable design is explored for the level shifter design.

### 3.2.3 Nanosecond delay dynamic level shifter based pulser circuit

The current limited static level shifter based pulser and the gate charge recycled level shifter based pulser both have drawbacks in terms of power consumption, speed of operation and reliability. The high power consumption of static level shifter based pulser makes it unsuitable for portable or battery powered applications. Hence, a nanosecond delay dynamic level shifter based pulser circuit is designed [23] [24]. A very low power consumption design is achieved with a cross-coupled design. The circuit consumes no static power from the high voltage rails. The current is drawn from the high voltage supply only during a transition which lasts only for a few nano-seconds. The schematic of the pulser circuit is shown in Fig. 3.10. For clarity and ease of explanation only the high side level shifter is shown here. The low-side MOSFET $M_{12}$ of the push-pull stage is driven by a similar level shifter. This is a modified version of the conventional HV level shifter reported in [25] and [26].

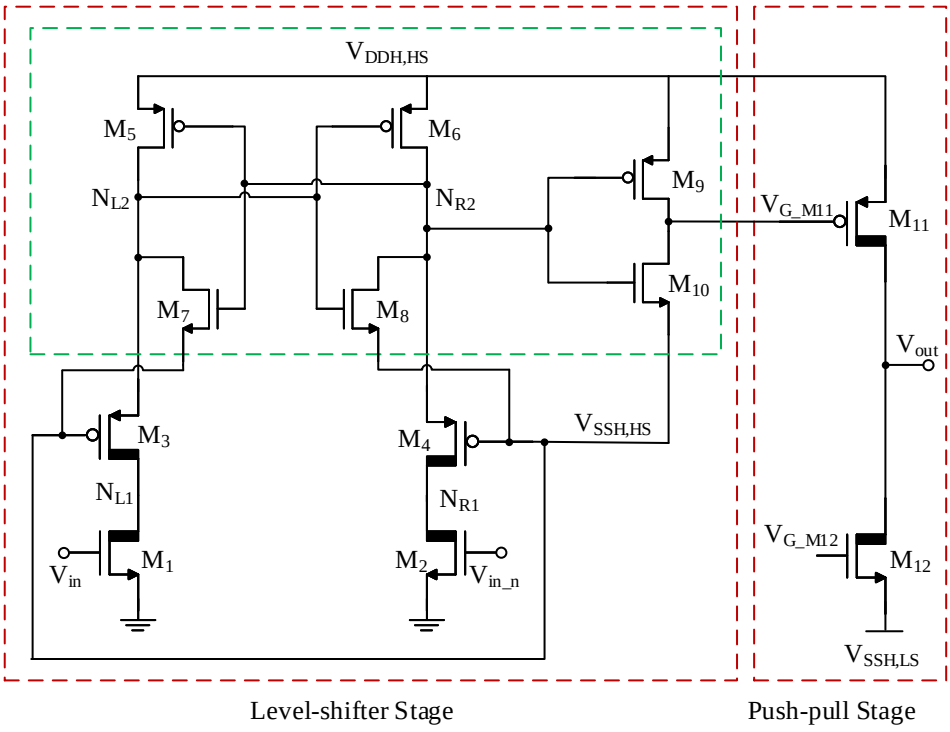



Fig. 3.10 Dynamic level shifter based pulser circuit.

The low voltage control signals drive the pull-down high voltage NMOS (HVNMOS) transistors $M_1$ and $M_2$. High voltage PMOS (HVPMOS) transistors $M_3$ and $M_4$ protect the floating LV MOSFETs. The gates of $M_3$ and $M_4$ are biased to a HV level $V_{SSH,HS}$. The LV

MOSFETs $M_5$ - $M_{10}$ are floating at a HV level between $V_{DDH,HS}$ and $V_{SSH,HS}$. It should be made sure that this difference is less than or equal to 5 V. Transistors $M_7$ and $M_8$ are used as active pull-downs which will pull the nodes $N_{L2}$ and $N_{R2}$ to $V_{SSH,HS}$. In order to ensure that the latch flips its state, $M_7$ and $M_8$ should be made much weaker than $M_5$ and $M_6$.

The working of the circuit is explained as follows. Let us assume that initially the node $N_{L2}$ is pulled to $V_{DDH,HS}$ and node $N_{R2}$ is at $V_{SSH,HS}$. Now, in order to flip the states, a logical high is applied to the gate of $M_1$ (3.3 V). An inverted signal is applied to the gate of $M_2$. $M_1$ pulls node $N_{L1}$ to ground. Transistor $M_3$ turns ON in saturation and this pulls $N_{L1}$ down. When this node is pulled a $V_{thp}$ below $V_{DDH,HS}$, $M_6$ turns ON and the latch flips state. The ratio of $M_3$ to $M_5$ decides how fast the node $N_{L2}$ is discharged. To derive the equations for DC operation of the circuit, we can equate the current through the transistors in each branch. As the circuit is symmetrical, the equations for only one side is shown here. The other side follows the same way. At the beginning of the transition, we can take $M_5$ to be in deep-triode region of operation. The current through this transistor can be written as:

$$I_{D5} = K_{p5}\left(\frac{W}{L}\right)_5 (V_{SG5} - V_{th5})\, V_{SD5} \tag{3.3}$$

$$I_{D5} = K_{p5}\left(\frac{W}{L}\right)_5 (V_{DDH} - V_{SSH} - V_{th5})\, V_{th6} \tag{3.4}$$

Since $M_3$ turns ON in saturation, the current equation can be written as:

$$I_{D3} = \frac{K_{p3}}{2}\left(\frac{W}{L}\right)_3 (V_{SG3} - V_{th3})^2 \tag{3.5}$$

$$I_{D3} = \frac{K_{p3}}{2}\left(\frac{W}{L}\right)_3 (V_{DDH} - V_{th6} - V_{SSH} - V_{th3})^2 \tag{3.6}$$

Combining (3.6) and (3.4) to get the aspect ratio, we can write:

$$\frac{(W/L)_3}{(W/L)_5} = \frac{2 \cdot K_{p5}\,(V_{DDH} - V_{SSH} - V_{th5})\, V_{th6}}{K_{p3}\,(V_{DDH} - V_{th6} - V_{SSH} - V_{th3})^2} \tag{3.7}$$

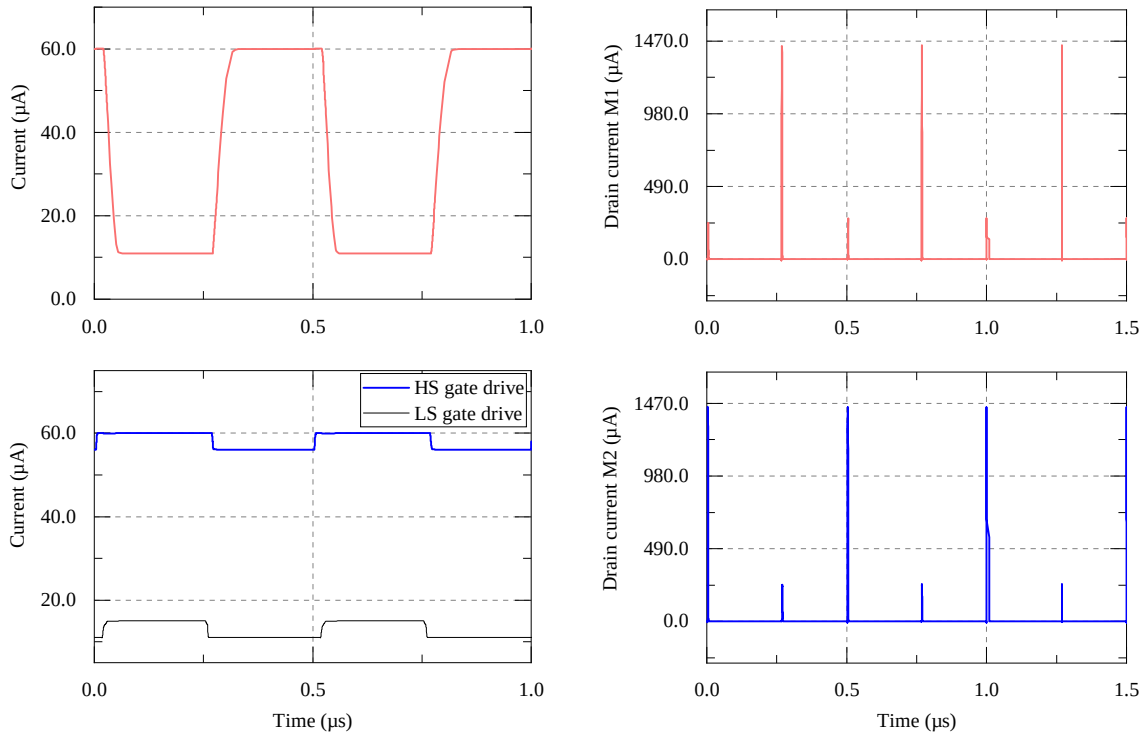
Similarly, $M_1$ is sized relative to $M_5$ to ensure sufficient current to flip the state of the latch. The current in $M_1$ can be written as:

$$I_{D1} = \frac{K_{p1}}{2}\left(\frac{W}{L}\right)_1 (V_{in} - V_{th1})^2 \tag{3.8}$$

Combining (3.8) and (3.4), we can write;

$$\frac{(W/L)_1}{(W/L)_5} = \frac{2 \cdot K_{p5} \left(V_{\mathrm{DDH}} - V_{\mathrm{SSH}} - V_{th5}\right) V_{th6}}{K_{p1} \left(V_{\mathrm{in}} - V_{\mathrm{th1}}\right)^2} \tag{3.9}$$

Using (3.9) and (3.7), we can size the MOSFETs in the level shifter. In the equations, only sizing information for $M_1$, $M_3$ and $M_5$ are shown. The MOSFETs on the right branch $M_2$, $M_4$ and $M_6$ follows the same design criteria. Post-layout simulations are performed to verify the design under various operating conditions before the tape-out. Some of the key simulations are shown here. It can seen from Fig. 3.11 (a) the gate drive control signals of the output push-pull stage. The level shifters make sure that transistors $M_{11}$ and $M_{12}$ have a HV level shifted control signal which is within the maximum allowed gate-source voltage limit. Fig. 3.11b shows the switching current through $M_1$ and $M_2$. It can be seen that a current of around 1.4 mA is drawn from the HV supply only during a transition. During the remaining times, there is no static current drawn from the HV supply by the level shifter. This makes the designed pulser circuit very useful for low-power applications.




(a) (b)

Fig. 3.11 (a) Post-layout simulation showing the HV pulser output and the high side and low side gate drive voltages of the push-pull stage; (b) Simulation showing the drain currents through the transistors $M_1$ and $M_2$.

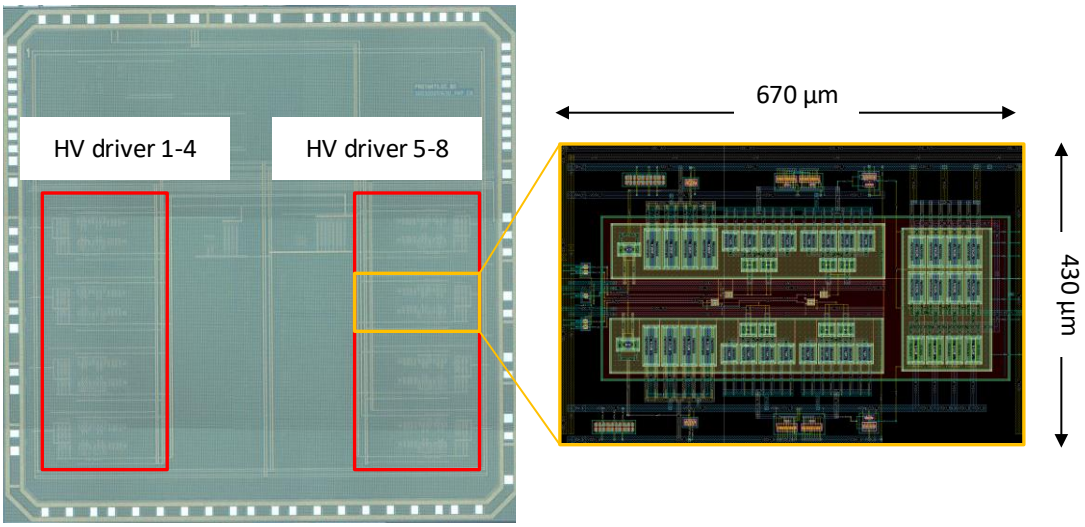



Fig. 3.12 Die photo and layout of the pulser circuit highlighted.

### Frequency control and pulse counter

A clock divider and pulse count control digital block is also implemented on chip. The digital block can be activated by an external trigger signal. A fixed input clock is fed into a frequency divider block. The frequency divider block takes in an input clock and provides the control signals blocks with a divided down frequency based on register settings of a 6 bit divide by N register. This block also provides an option to select between a continuous pulsing and fixed pulsing scheme. An 8 bit pulse count register sets the number of pulses. The first 7 bit sets the pulse count and the 8th bit selects between continuous pulsing and fixed pulsing mode. The 6-bit divide by N counter sets the output pulse width as shown in table 3.1. The trigger input needs to stay high for atleast 3 clock cycles. Once the trigger is detected, the pulsing operation will be started and the low voltage divided clock signals are input to the HV pulser circuit. A 6 bit pulse counter block can be programmed to generate upto 128 pulses.

### Chip measurement results

The HV pulser circuit has been taped-out in a 0.18 µm HV SOI process. The die photograph and highlighted layout can be seen from Fig. 3.12. The transceiver chip has 8 HV pulser circuits each occupying an area of 0.28 $mm^2$. The chip is packaged in a QFN 80 package. To verify the performance parameters of the chip, a PCB has been designed with 2 chips soldered on it. The required control signals and the SPI master is implemented using a STM32 Nucleo microcontroller. All the required power supplies are applied externally using

Table 3.1 6 bit clock division

| B5 | B4 | B3 | B2 | B1 | B0 | N | Output pulse width(s) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 64 | 64/fclk |
| 0 | 0 | 0 | 0 | 0 | 1 | 63 | 63/fclk |
| 0 | 0 | 0 | 0 | 1 | 0 | 62 | 62/fclk |
| . | | | | | | | |
| . | | | | | | | |
| . | | | | | | | |
| 1 | 1 | 1 | 1 | 0 | 1 | 3 | 3/fclk |
| 1 | 1 | 1 | 1 | 1 | 0 | 2 | 2/fclk |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1/fclk |

a 4 quadrant power supply (Keysight N6705c DC power analyzer). The supply ramp-up and sequencing can be controlled using this power supply. A photo of the PCB can be seen in Fig. 3.13.

The chip is set in its default state for the pulser measurements. Two HV inputs 60 V and 15 V are externally applied to the chip. The low voltage supply used is 3.3 V. Two on-chip HV linear regulators generate 56 V and 11 V. These form the $V_{SSH,HS}$ and $V_{SSH,LS}$ of the chip. The HV pulser circuit has an output load of roughly 15 pF which includes the PCB parasitics and probe capacitance. The output of the pulser circuit switching at 2 MHz can be seen from Fig. 3.14a. The pulser circuit produces a peak to peak output voltage of 49 V at 2 MHz switching frequency.The circuit has an input-output delay of 28 ns. The rise and fall times are measured to be 26 ns and 30 ns respectively. The pulser can handle frequencies upto 8 MHz.

Fig. 3.14b illustrates the performance of the frequency control and pulse counter block. As it can be seen from the figure, a trigger input of 5 µs duration was applied externally. Once the trigger is detected, the pulser starts pulsing for 10 cycles. It can be seen that before and after pulsing, the pulser output is pulled to the $V_{DDH,HS}$. The pulsing frequency is set to 1 MHz for this measurement.

In order to measure the crosstalk between two adjacent HV pulsers, one HV channel is enabled and pulsed at 2 MHz and the adjacent HV channel is disabled. The output of both the channels are measured using the oscilloscope. In Fig. 3.15a, a transient response of the two channels are shown. A fast fourier transform (FFT) performed on this measurement result gives the spectra of the two channels. This is shown in Fig. 3.15b. We can see that the crosstalk between the two channels is −108 dB at 2 MHz. This is negligible and shows that the channels are well isolated from each other.

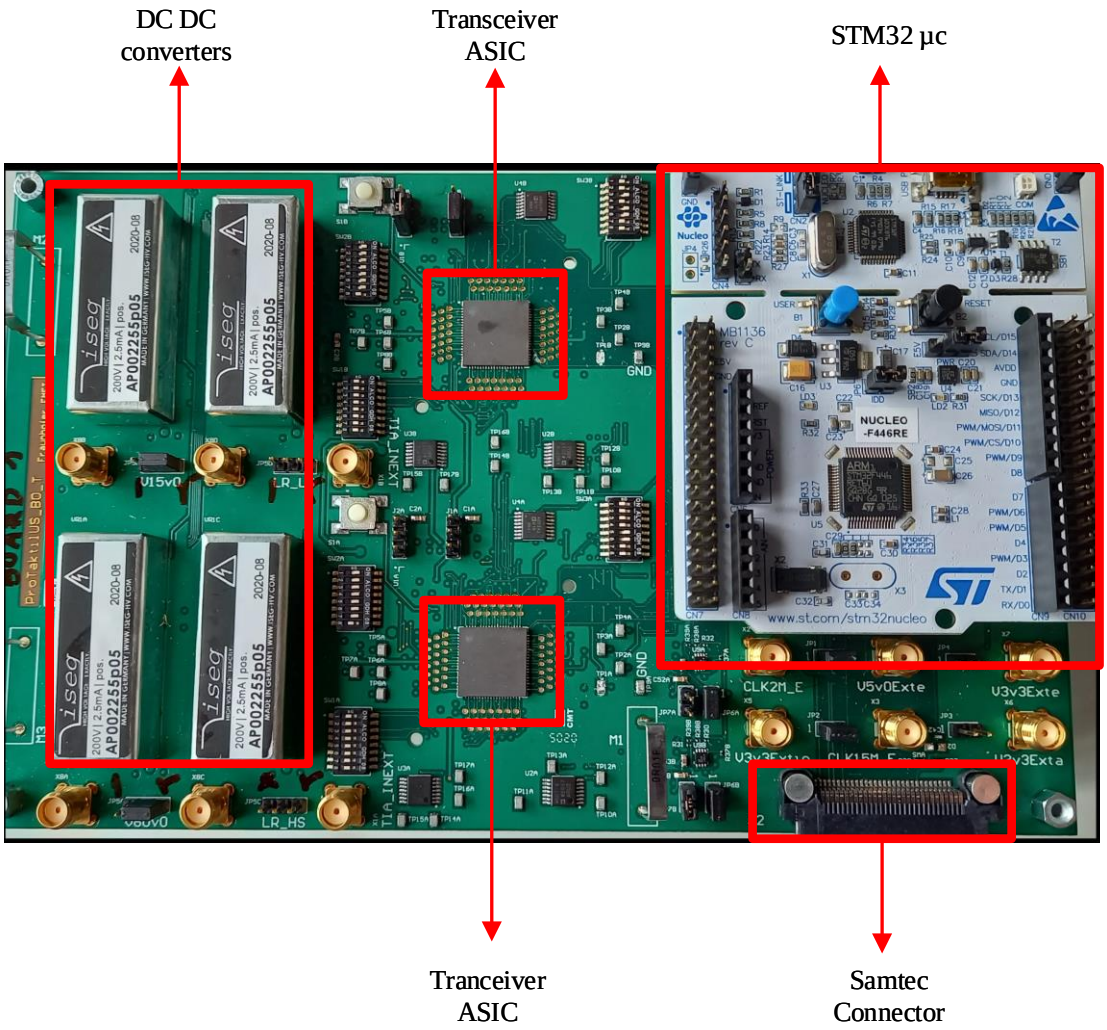
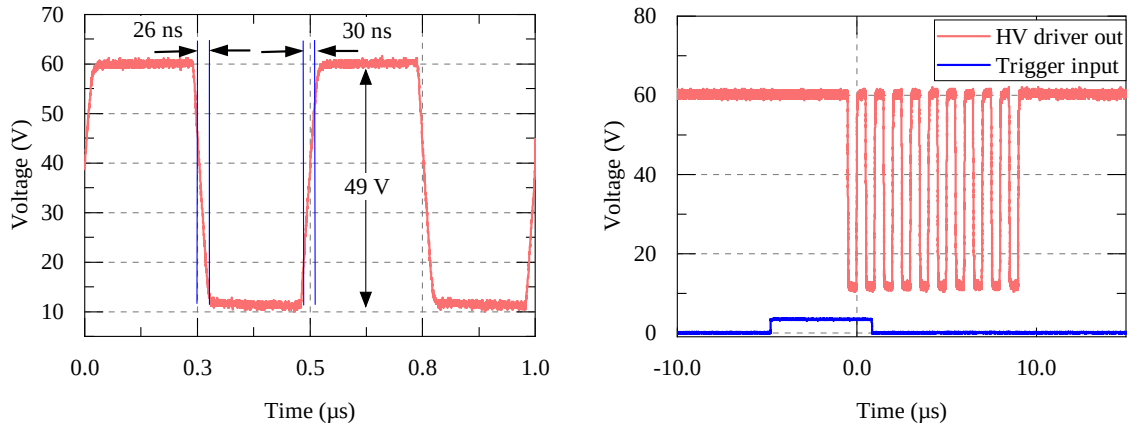


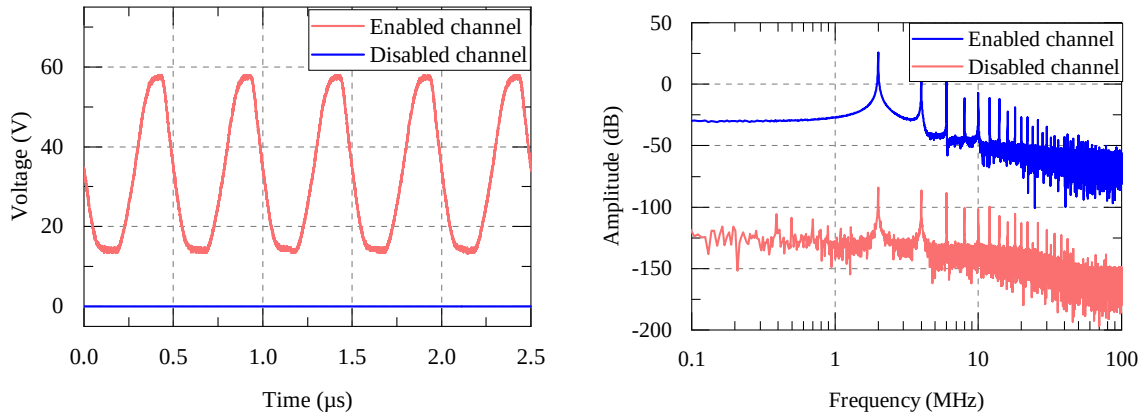

Fig. 3.13 The test PCB with the two transceiver chips and external control and power circuits.

The measured performance parameters of the HV pulser circuit are listed in table 3.2 and are compared with previously published similar works. It can be seen that our work obtains the best performance in terms of input to output delay and rise and fall times of the pulses for output capacitive loads which are very similar in values. The maximum pulse frequency handled by the pulser also compares favorably, only [27] has a higher frequency capability. It can be noted that the area occupied by our work is the largest as compared to the other works which are implemented in the same process node. This can be attributed to the fact that in this work, the focus has been to implement a transceiver topology with on-chip HV biasing. The use of two level shifters per pulser results in nearly doubling of the area requirement per pulser channel. A direct comparison of the power/current consumption is difficult as it largely depends on the number of pulse cycles used, which in turn depends on the application.




(a) (b)

Fig. 3.14 (a) Measured output of the HV pulser circuit at 2 MHz; (b) pulser output showing response to an input triggering signal.




(a) (b)

Fig. 3.15 (a) Measured crosstalk between two adjacent HV pulser channels; (b) Frequency spectrum of the two channels.

Hence, whereever available, a current consumption value is reported and it can be seen that this work compares positively in terms of power consumption as well. A figure of merit (FOM) can be defined combining the different pulser parameters to compare our work with the state of the art. The FOM can be defined as give below:

$$\text{FOM} = \frac{V_{\text{pp}}\,[\text{V}]\, f\,[\text{MHz}]\, C_{\text{L}}\,[\text{pF}]}{A\,[\text{mm}^2]\, t_{\text{delay}}\,[\text{ns}]} \tag{3.10}$$

Where $V_{\text{pp}}$ is the peak to peak HV pulse, $f$ is the pulse frequency, $C_{\text{L}}$ is the load capacitor, $t_{\text{delay}}$ is the input-output delay and $A$ is the area of the pulser circuit. It can be seen that this

Table 3.2 Measured performance parameter of the HV pulser circuit compared with prior art

| Parameter | This Work | [28] | [29] | [30] | [27] |
|---|---|---|---|---|---|
| Technology | 0.18$\mu$m HV SOI | 0.18$\mu$m BCD | 0.18$\mu$m CMOS | 0.35$\mu$m HV CMOS | 0.18$\mu$m HV BCD |
| Pulse voltage ($V_{pp}$) | 49 | 9.8 | 15 | 60 | 60 |
| Pulse frequency (MHz) | 8 | 1.25 | 2.56 | 1.38 | 9 |
| Output load (pF) | 15 | 15 | 12 | 18 | 18 |
| Input-output delay (ns) | 28 | 22.5 | 30.8 | 34 | N.A |
| Rise/fall time (ns) | 26/30 | 40-50 | 57/30 | 68/65 | N.A |
| Current/power consumption | 1.38 mA dynamic | 19.9 mA dynamic | N.A | 98.1 mW (static) | 852 µW/ch |
| Area ($mm^2$) | 0.28 | 0.022 | 0.15 | 0.08 | 0.17 |
| FOM | 750 | 371 | 99.7 | 547 | - |

work has the best FOM among the state of the art compared in the table 3.2. The value of the current is ommited from the FOM calculation as it is not clearly mentioned in the reported works and an inaccurate number could grossly misrepresent the FOM calculation. Moreover, the input-output delay is directly proportional to the current consumed in the circuit which indirectly represents the current in the FOM.

## 3.3 High Voltage, Fast Transient Response and High Current Sinking Linear Regulator

In the previous sections, it is explained that the low side of the two-level high voltage pulser circuit needs to sink a large amount of current when the CMUTs are being discharged. This necessitates the use of a HV regulator with high current sinking capabilities and fast transient response. The project requirements restricts the use of externally supplied HV rails to two. Hence, it is required to design an integrated HV regulator that meets this requirement. A straightforward way to have an on chip implementation is to design a linear regulator as opposed to a switching converter.

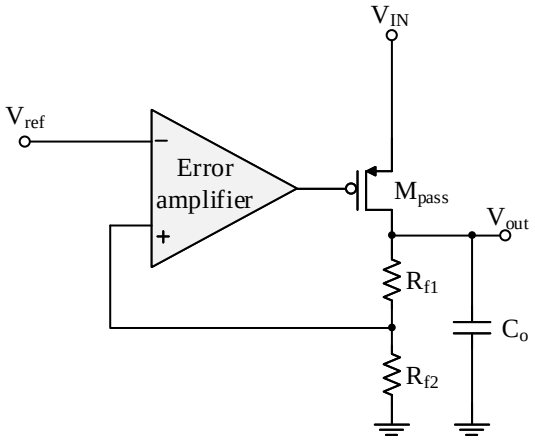



Fig. 3.16 A PMOS pass transistor LDO.

A conventional topology of a low-dropout linear regulator (LDO) is shown in Fig. 3.16. A classical PMOS pass transistor based topology is shown here. The reference voltage is supplied by a bandgap reference (BGR) circuit. The output voltage sensing feedback resistors $R_{f1}$ and $R_{f2}$ feeds a portion of the output voltage back to the error amplifier. The error amplifier adjusts the gate voltage of the $M_{pass}$ to control the $V_{out}$ to finally make its two input terminals equal. Two main drawbacks of this circuit topology make it unsuitable for our application. This circuit is not capable of sinking a large current in a short period of time. As it can be seen, any large load current discharged into the output node needs to be sunk through the feedback resistors to the ground. In most conventional applications which use LDOs, this is acceptable since they are used as local power supplies to source the desired current to the load. The second problem is that, it is not possible to separate the input voltage from the supply voltage of the amplifier. Hence, when HV inputs are used, it is indispensable to use a HV error amplifier.

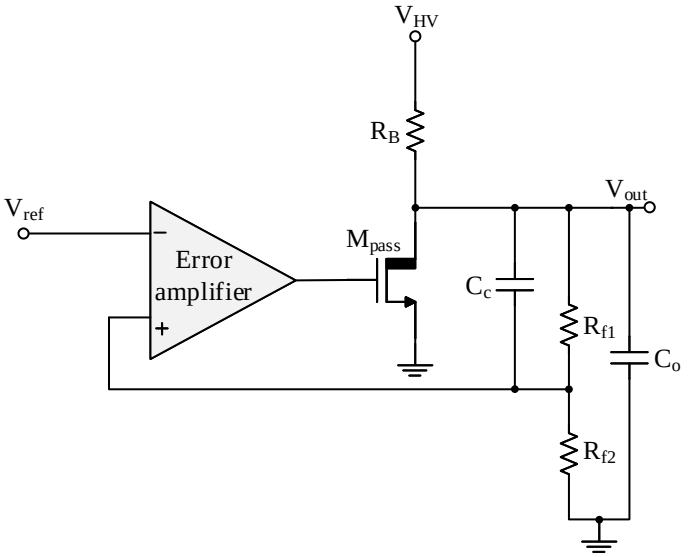



Fig. 3.17 The designed HV linear regulator topology with current sinking capability.

We propose a new topology with high current sinking capability and isolation of input voltage from the error amplifier supply. This is based on our previously published work [31]. The circuit is shown in Fig. 3.17. The pass transistor is referenced to ground to sink a large amount of current. This also allows us to isolate the low voltage error amplifier from the high input voltage. The resistive feedback network $R_{f1}$ and Rf2 sets the output voltage. The biasing resistor $R_B$ sets the quiescent current. An output filter capacitor $C_o$ is placed at the output since the regulator can not respond instantaneously to the load current change. The $C_o$ prevents the output voltage from drifting too far away from the design value until the feedback loop reacts to correct the variation.

The feedback factor can be written as:

$$\beta = \frac{R_{f2}}{R_{f1} + R_{f2}} = \frac{V_{ref}}{V_{out}} = \frac{1.2}{11} \tag{3.11}$$

The quiescent current flow through the feedback resistors can be written as:

$$I_f = \frac{V_{out}}{R_{f1} + R_{f2}} = \frac{11}{R_{f1} + R_{f2}} \tag{3.12}$$

For a 100 $\mu$A current, the equations (3.11) and (3.12) are solved to get the feedback resistor values. This is estimated to be $R_{f1}$= 95 k$\Omega$ and $R_{f2}$= 12 k$\Omega$. For 10 $\mu$A quiescent current through the pass transistor, the $R_B$ is set at 36.3 k$\Omega$. Initially during a load transient, when the circuit is not regulating, all of the load current needs to be taken in by the output capacitor. Considering that the maximum allowed voltage overshoot at the output is 1 V and

the current spikes have a maximum width of 50 ns, for a load current of 100 mA the output capacitor can be calculated as:

$$C_o = \frac{\int i(t).dt}{\triangle Vout} = \frac{100\,\text{mA}.50\,\text{ns}}{1\,V} = 5\,\text{nF} \tag{3.13}$$

This is the minimum capacitance value to be used. So we use 6 nF and it will be off-chip.

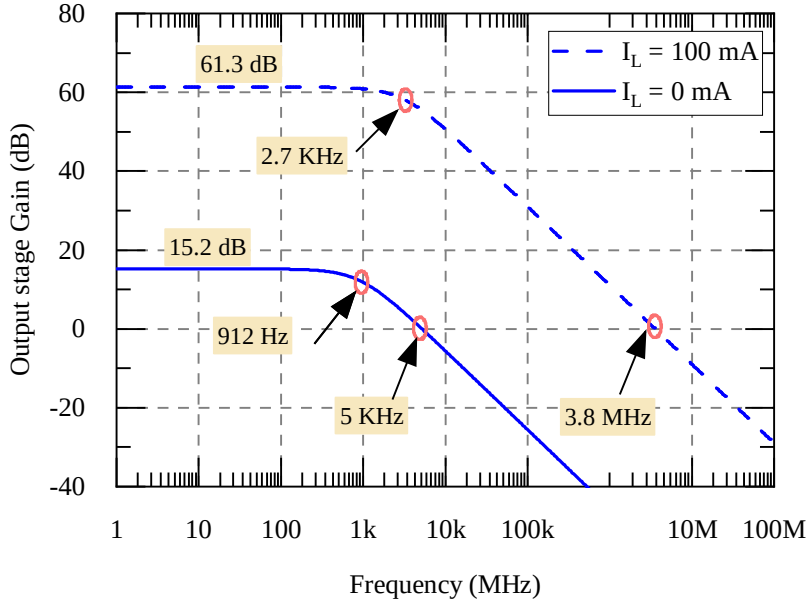



Fig. 3.18 Small-signal gain presented by the output stage for maximum and minimum load conditions.

In order to determine an optimum compensation for the regulator, it is required to determine the regulator's behavior for different load conditions. As we know the extreme load currents as 100 mA and 0 mA, we can determine the regulator dynamic behavior under these two conditions and design a compensation method for the worst case condition. The output stage of the regulator is an NMOS common source stage, it presents a gain which is part of the loop-gain of the system. With change in current, the $g_{m,p}$ changes which results in a change in open loop DC gain and the bandwidth. An ac simulation is carried out to determine this. The simulation result is plotted in Fig. 3.18. It can be seen that at maximum load condition, the pole at the output node moves to higher frequencies. Since, the dominant pole is at the output node, this could cause the output pole to come close to the error amplifier pole and result in reduced phase margin and potential instability.

To determine the small-signal dynamics of the system, a small-signal equivalent circuit is required. For the regulator, the error amplifier, pass transistor, feedback network and the output capacitor constitute the small-signal network. A small-signal circuit and its small-signal equivalent models are shown in Fig. 3.19 and Fig. 3.20. The compensation capacitor

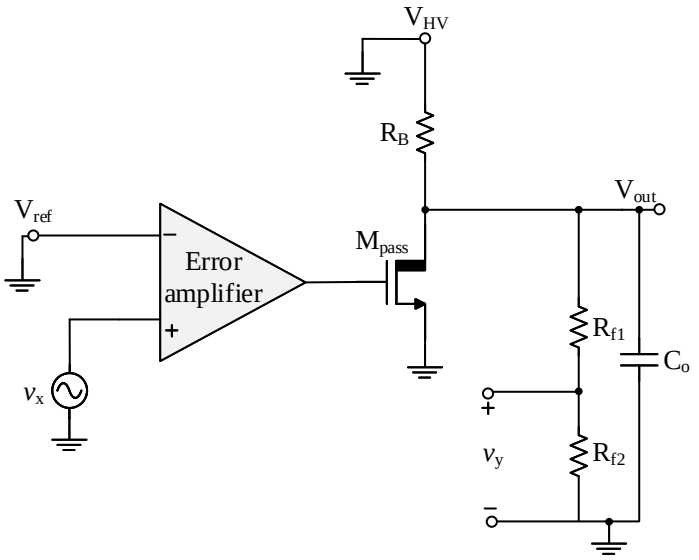



Fig. 3.19 AC circuit of the linear regulator used to derive the small-signal equivalent circuit.

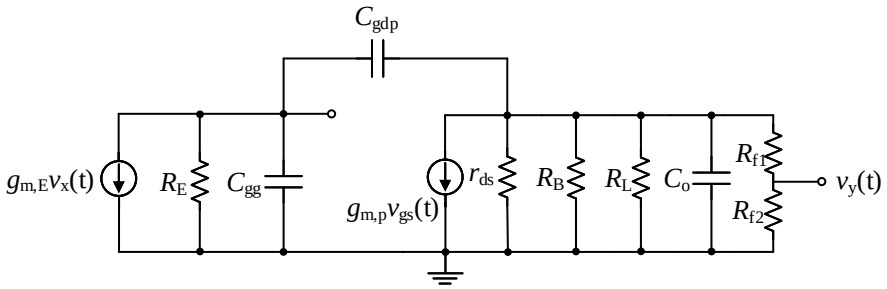



Fig. 3.20 Small-signal equivalent circuit of the HV regulator. The compensation capacitor is not shown.

is not shown now to simplify the loop gain calculations. It is required to virtually break the loop to estimate the loop gain of the system. This is done as shown in Fig. 3.19. The loop gain can be estimated as shown by [32]:

$$\mathrm{T(s)} = \frac{-v_y}{v_x} \tag{3.14}$$

The DC loop gain can be written as:

$$\mathrm{T_0} = g_{\mathrm{m,E}}.R_{\mathrm{E}}.g_{\mathrm{m,p}}.R_o.\beta \tag{3.15}$$

where $R_{\mathrm{o}}$ is:

$$R_{\mathrm{o}} = r_{\mathrm{ds,p}} \parallel R_{\mathrm{L}} \parallel (R_{\mathrm{f1}} + R_{\mathrm{f2}}) \tag{3.16}$$

The high frequency loop gain can be evaluated to:

$$\mathrm{T(s)} = \frac{g_{\mathrm{m,E}}.R_{\mathrm{E}}.g_{\mathrm{m,p}}.R_o.\beta(1 - sC_{\mathrm{gd}}/g_{\mathrm{m,p}})}{(1 + sR_{\mathrm{E}}.C_{\mathrm{gg}})(1 + sR_{\mathrm{o}}.C_{\mathrm{o}})} \tag{3.17}$$

It can be seen from (3.17), the system has two poles and one zero. The zero is created by the parasitic gate-drain capacitor of the pass transistor. This can be neglected as it will be in the high GHz range of frequencies. One pole is formed by the output capacitance and output resistance ($f_{\mathrm{p1}}$) and the second pole is formed by the pass transistor gate capacitance and the output resistance of the error amplifier ($f_{\mathrm{p2}}$). The output pole will be the dominant pole in our case since the output capacitance used for design will be very high value to have a small output voltage overshoot during a large load transient. The system will have a small phase margin when the error amplifier pole gets closer to the output dominant pole. This could result in unstable regulator behavior.

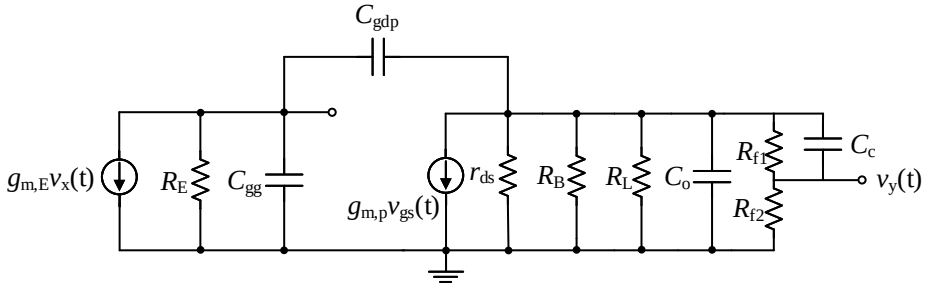



Fig. 3.21 Small-signal equivalent circuit of the HV regulator with lead compensation capacitor connected.

To guarantee a stable frequency response, the closed loop system should have sufficient phase margin. Compensation techniques are used to achieve this by ensuring that the two closed loop poles are placed apart in frequency [33]. A widely used technique for compensating the opamps is using miller compensation [34]. However this technique is not suitable for our application as the dominant pole is formed by the large output capacitance. Another method of compensating the regulator is to use a feed-forward capacitor to produce a left half plane (LHP) zero. This is achieved by connecting the compensation capacitor across the feedback resistor $\mathrm{R_{f1}}$ which creates a bypass path for the loop gain at high frequencies [35]. This method creates a pole-zero pair where the non-dominant pole is canceled with the zero. It has to be made sure the newly created pole is beyond the unity gain frequency. The transfer function of the compensation network can be written as [31], [35]:

$$H(s) = \frac{(1 + sC_{\mathrm{c}}R_{\mathrm{f1}})}{1 + sC_{\mathrm{c}}\left(\frac{R_{\mathrm{f1}}R_{\mathrm{f2}}}{R_{\mathrm{f1}}+R_{\mathrm{f2}}}\right)} \tag{3.18}$$

This newly created pole ($f_{p3}$) should be placed beyond the unity gain bandwidth. This can be written as:

$$f_{p3} \geqslant 2.2 \cdot \mathrm{GBW}_{max} \tag{3.19}$$

From (3.18):

$$f_{p3} = \frac{1}{2\pi(R_{f1} \parallel R_{f2})C_c} \geqslant 2.2 \cdot \mathrm{GBW}_{max} \tag{3.20}$$

Using the information from Fig. 3.18 in (3.19), we get $f_{p3} \geqslant 7.6$ MHz. This gives:

$$C_c \leqslant 1.8\,\mathrm{pF} \tag{3.21}$$

The bandwidth requirement of the error amplifier can be estimated from this. The value of the compensation capacitor determines the LHP zero. It has to be ensured that the non-dominant pole of the uncompensated regulator ($f_{p2}$) is placed close to this frequency. This gives:

$$f_{p2} = f_z = \frac{1}{2\pi R_{f1} C_c} \tag{3.22}$$

This gives $f_z = 930\,\mathrm{kHz}$. The complete schematic of the HV regulator is shown in the Fig. 3.22. A flipped voltage follower based class AB amplifier is implemented as the error amplifier for high slew rate performance [36], [37]. The design of the high side linear regulator follows the same principle as explained so far. It is not presented here for this reason. Also, the load current requirement of the HS regulator is much lower as this is used to bias the HV protection transistors in the HV pulser circuit. It needs to sink only a few mA of current which happens due to the flipping of the latch in the pulser circuit.

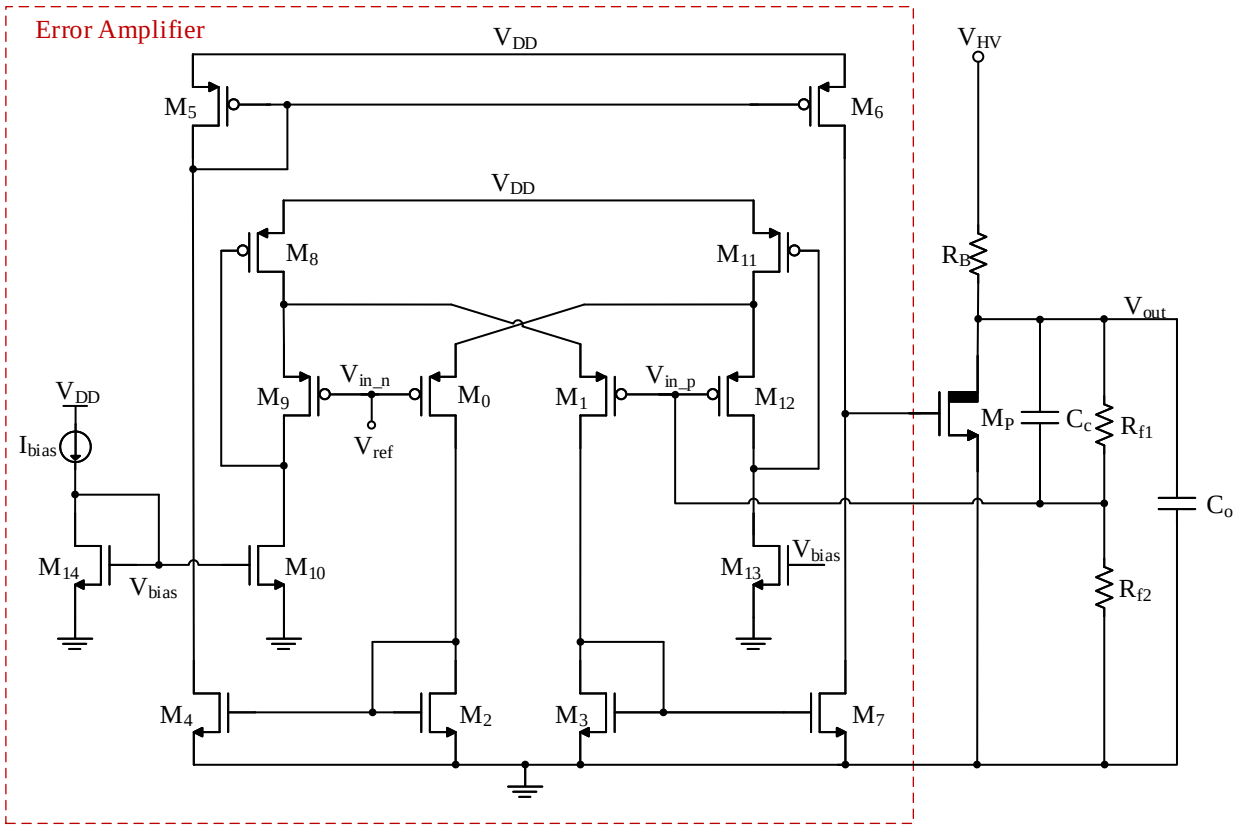



Fig. 3.22 Schematic of the linear regulator with a class AB error amplifier.

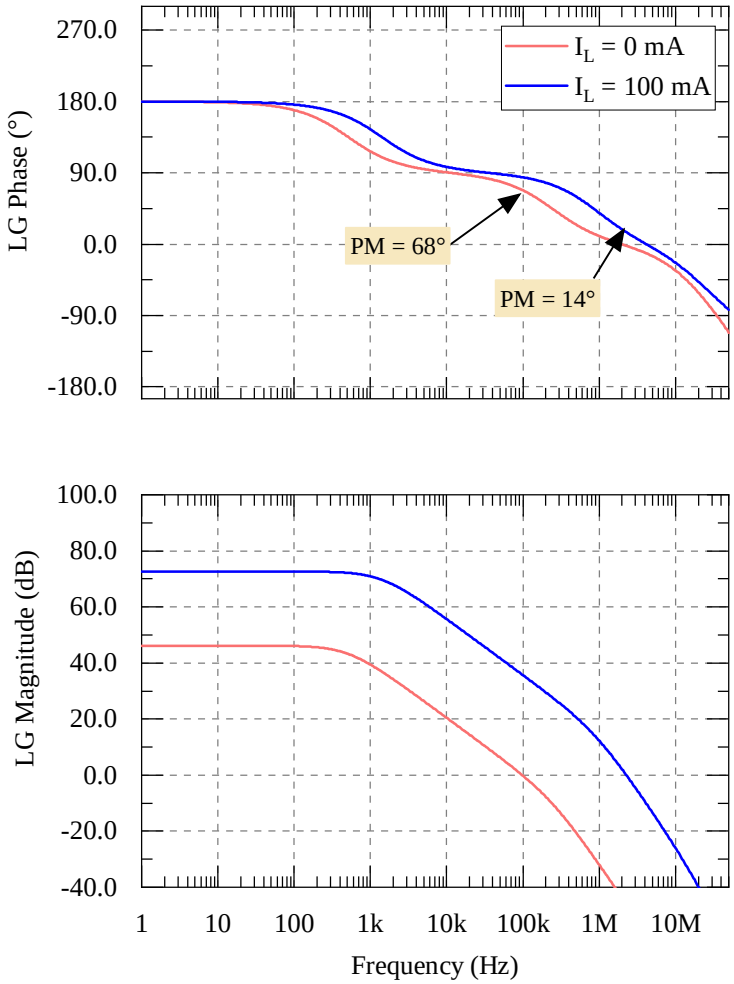



Fig. 3.23 Magnitude and phase response plot of the loop-gain of the uncompensated regulator at the two dc operating points.

Loop-gain analysis is performed to estimate the stability of the circuit. The magnitude and phase response plots of the uncompensated regulator loop-gain for the two operating points (no load condition and 100 mA load condition ) are illustrated in Fig 3.23. It can be seen that, when the load current increases, the loop-gain of the regulator increases, which brings the non-dominant pole inside the unity gain bandwidth thereby degrading the phase margin. Also, with increase in the load current, the small signal output resistance of the pass transistor is reduces, which reduces the overall output resistance of the node thereby pushing the dominant pole $f_{p1}$ to higher frequencies. The loop-gain response of the compensated regulator is shown in Fig. 3.24. It can be seen that the circuit now exhibits a phase margin of more than 60° at both the operating conditions.

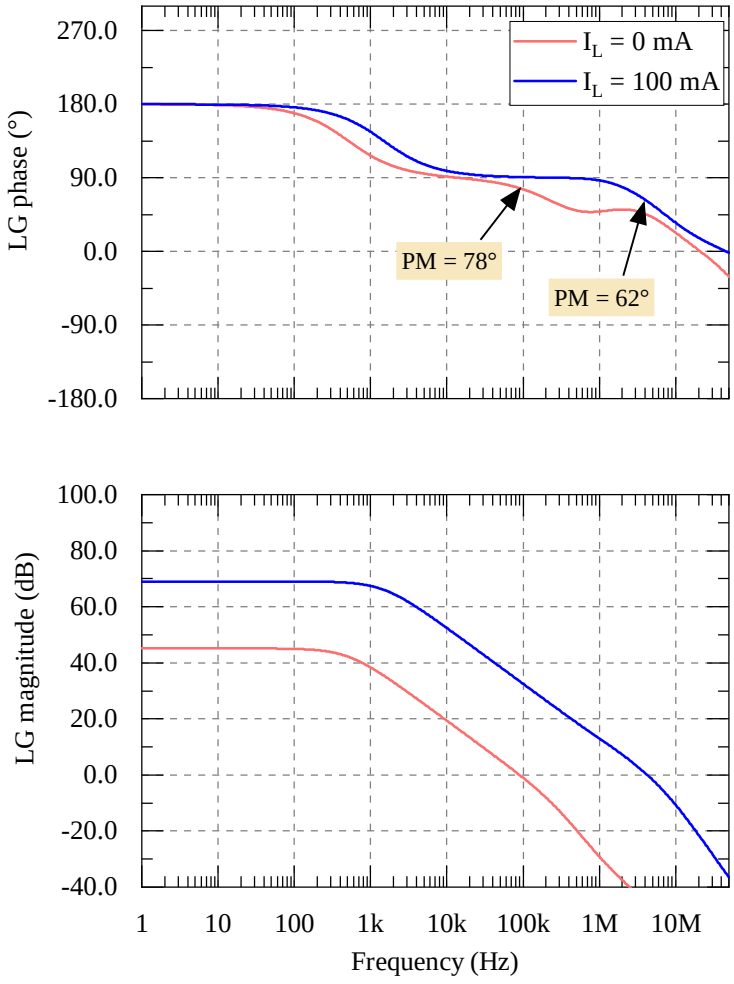



Fig. 3.24 Magnitude and phase response plot of the loop-gain of the regulator at the two dc operating points after adding the compensation capacitor.

### 3.3.1 Measurement results

The die micro-photograph highlighting both the designed regulators are shown in the Fig. 3.25. It can be seen that the high side regulator occupies smaller layout area as the pass transistor in this case is much smaller due to the smaller load current requirement. To check the start up behavior, the 15 V supply is ramped up with 10 ns rise time. The regulator takes roughly about 270 ns to start up and settle to its final value. This is illustrated in Fig. 3.26.

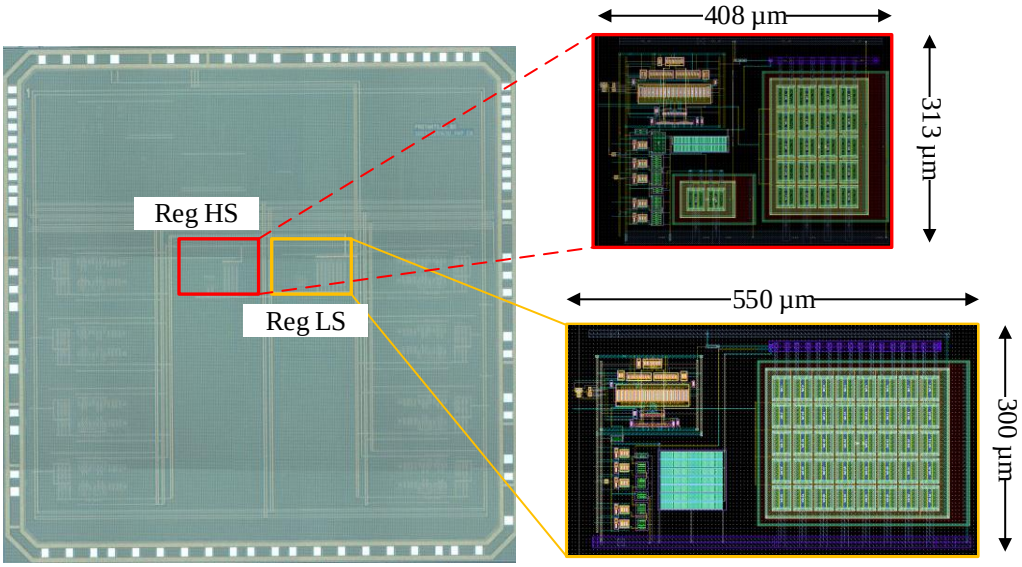



Fig. 3.25 Die photo and layout of the HV linear regulators highlighted.

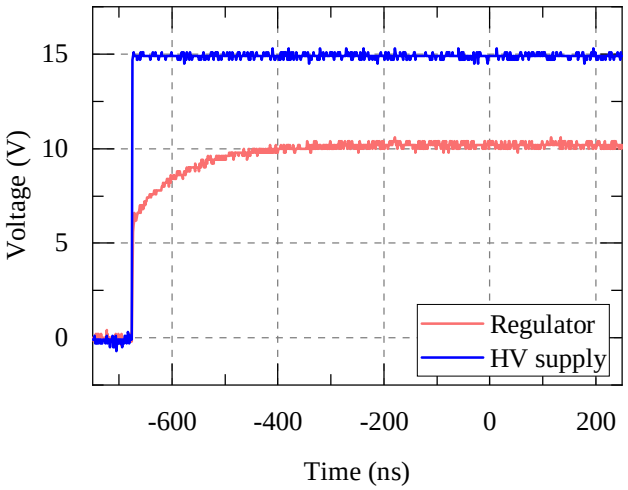



Fig. 3.26 Measurement results showing the start up behavior of the low side HV regulator. The regulator settles to around 10.2 V in 270 ns.

The line regulation performance is measured and is illustrated in Fig. 3.27. The measured line regulation is estimated to be 100 mV/V. The load transient performance of the regulator

when used in the CMUT pulser system is shown in Fig. 3.28. The result shows the case when all 8 pulsers of the transceiver system are switching together. In Fig. 3.28a, the DC coupled result and in Fig. 3.28b, the regulator output is AC coupled for easy measurements. It can be seen that the maximum voltage overshoot seen at the regulator output is 700 mV. The circuit takes around 200 ns to settle to a stable value after experiencing the load current transient. This matches well with the design specifications.

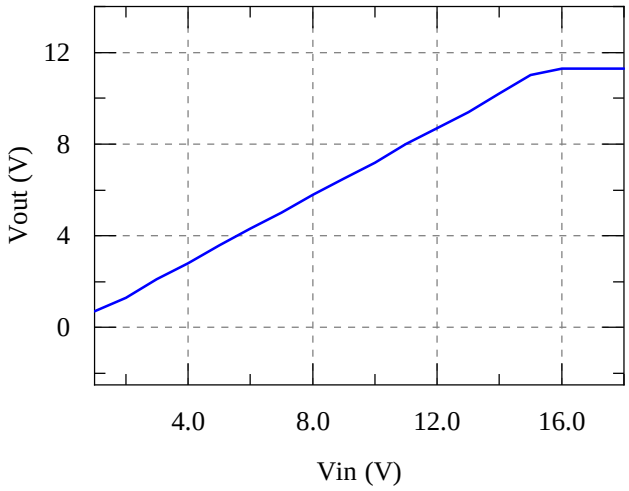



Fig. 3.27 Measurement result showing the line regulation behavior of the low-side regulator.

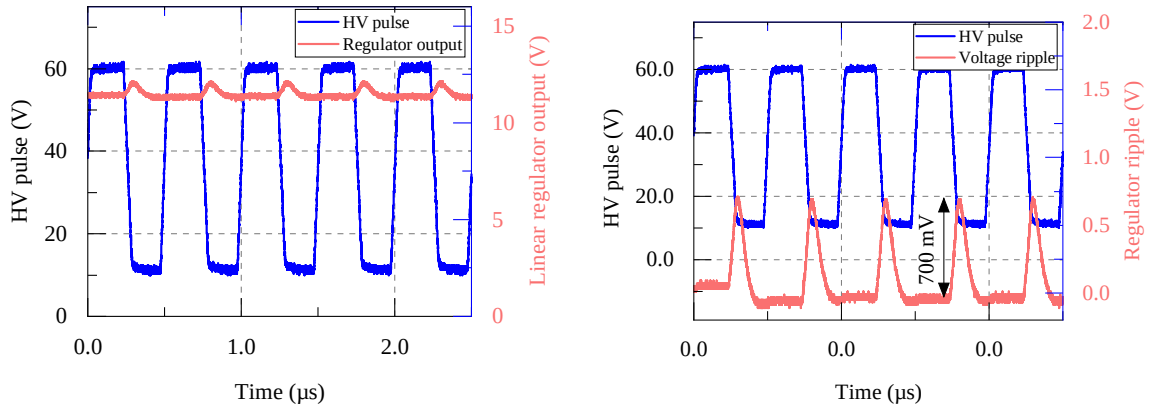



Fig. 3.28 (a) Measurement result showing the transient load response of the 11 V linear regulator when all 8 channels of the HV pulsers are turned on; (b) The regulator output ripple voltage after AC coupling the output voltage.

Table 3.3 Performance parameters of the low side linear regulator.

| Parameter | Value |
|---|---|
| $V_{in}$ | 15 V |
| $V_{out}$ | 11 V |
| $I_{L,max}$ | 0 mA |
| $I_{L,min}$ | −100 mA |
| $I_Q$ | 110 µA |
| Line regulation | 100 mV/V |
| Load regulation | 100 mV/mA (simulation) |
| Power efficiency | 73 % |
| $C_{ext}$ | 6 nF |

## 3.4 Low Voltage Receiver Front-End Design

As described in chapter 2, a single CMUT element can be used as both a transmitter and receiver of acoustic signals at ultrasonic frequencies. The circuit architectures to use the CMUT in the transmit mode of operation are presented in the previous sections of this chapter. To operate the CMUT in the receive mode, a dc bias voltage is applied to the CMUT. This bias should be close to the pull-in voltage (collapse voltage) for optimum electro-mechanical transduction efficiency [10] [7]. The interfacing scheme proposed in this work ensures that the bias voltage can be close to the pull-in voltage. The ultrasound signals incident on the CMUT membrane will cause the membrane to vibrate causing it to change its capacitance which in turn produces an alternating current. A pre-amplifier circuit can be used to readout this current signals. A small CMUT element has a large resistance. To interface such a high impedance sensor, a current input amplifier is required. A transimpedance amplifier (TIA) is used to convert the CMUT current to a voltage output. Before going into the details of the designed TIA circuit, different current amplification methods are briefly discussed below.

### 3.4.1 Open-loop transimpedance amplifiers

The simplest TIA that can be implemented to convert an input current into an output voltage is by using a resistor. The TIA implementation with a single resistor is shown in Fig. 3.29.

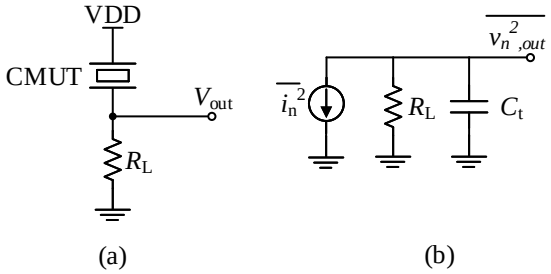



Fig. 3.29 (a) Conversion of CMUT current to voltage output; (b) Equivalent circuit.

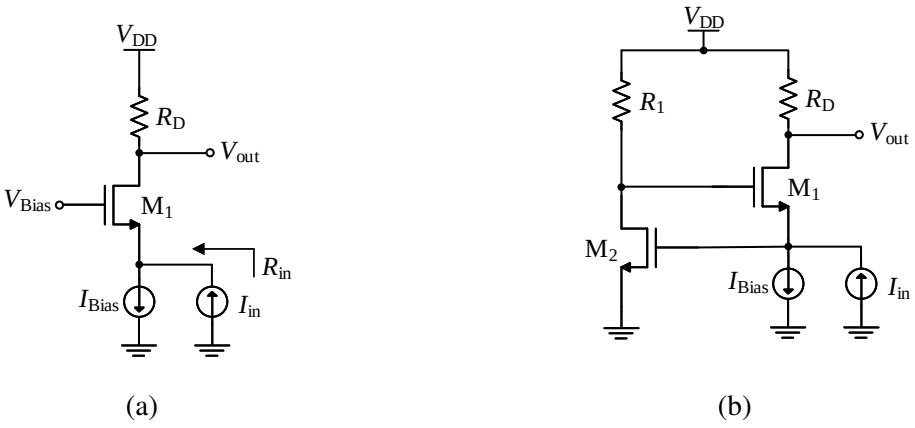
The circuit provides a transimpedance gain of $R_L$. If we represent the total parasitic capacitance including the CMUT capacitance at the node $V_{out}$ as $C_t$, the bandwidth can be written as $1/2\pi R_L C_t$. This shows that there is a direct trade-off between noise, bandwidth and gain. From the equivalent circuit in Fig. 3.29, the total input referred noise current can be written as:

$$\overline{I_{n,in}^2} = \frac{kT}{R_L^2 C_t} \tag{3.23}$$

This shows that to minimize the noise, the value of $R_L$ has to be maximized. This also increases the transimpedance gain, however reduces the bandwidth. Typically, this resistor termination is followed by an amplifier. This direct trade-off between key performance parameters indicates that this simplistic approach is not suitable for high performance applications. Hence, other topologies have to be considered.

Another open loop transimpedance amplifier which is commonly used for high impedance sensors, is the common-gate (CG) based TIA. This is shown in Fig. 3.30a. The input current is applied at the source and the output is taken from the drain of the transistor $M_1$. All of the input current flows through $R_D$. Hence the transimpedance gain can be written as:

$$A_T = R_D \tag{3.24}$$




(a) (b)

Fig. 3.30 (a) Schematic of the CG-TIA; (b) Regulated cascode CG-TIA.

The input resistance of the CG-TIA topology can be derived from its small-signal model and it can be written as [38]:

$$Rin \approx \frac{1}{g_m + g_{mb}} + \frac{R_D}{(g_m + g_{mb})\, r_o} \tag{3.25}$$

If $r_o \to \infty$, the input resistance becomes:

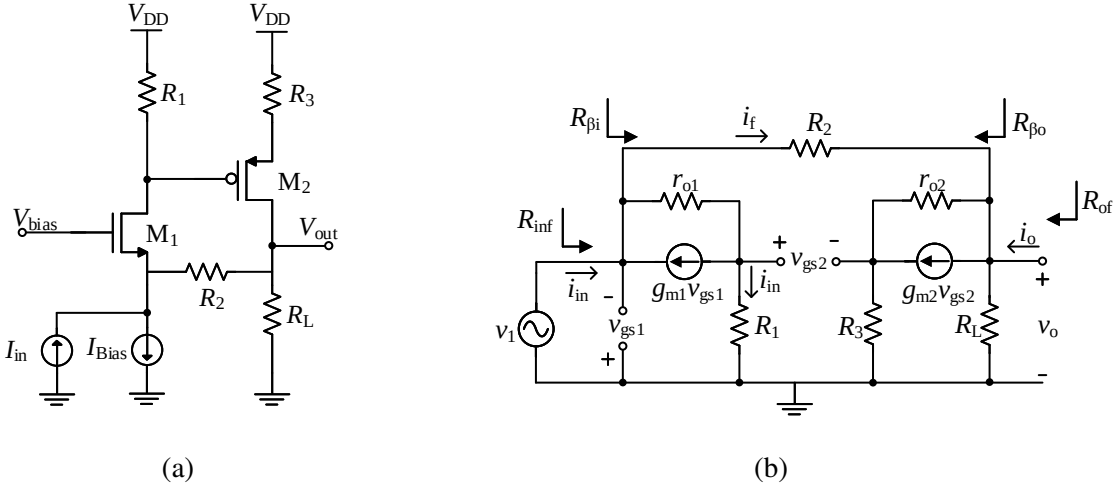
$$Rin \approx \frac{1}{g_m + g_{mb}} \tag{3.26}$$

With advanced process nodes, the value of $r_o$ is not very high and the second term in (3.25) is not negligible. This increases the input resistance of the TIA. Another drawback of the CG-TIA is that the noise of the biasing current source and the load resistor $R_D$ are referred to the input with a factor of one. This makes the total input referred noise of this

topology to be higher compared to other closed loop TIA topologies [39] [38]. Further, for higher gain, the value of $R_D$ needs to be maximized. This brings a direct trade-off between transimpedance gain and output swing. A regulated cascode TIA (RGC-TIA) is illustrated in Fig. 3.30b. This topology aims to boost the $g_m$ of the CG transistor $M_1$ by using negative feedback. The negative feedback is implemented using a CS amplifier stage formed by $M_2$ and $R_1$. The $g_m$ is multiplied by a factor which equals the gain of the boosting amplifier. This lowers the input impedance and also extends the bandwidth. As the $g_m$ is boosted by a factor of $(1+A_{gb})$, the noise performance is expected to improve as compared to the CG TIA [39]. The issue with the headroom still remains with this topology. Hence, feedback TIA topologies are investigated.

### 3.4.2 Feedback transimpedance amplifiers

As explained in the previous section, trade-offs in terms of noise, voltage swing and power consumption of open loop TIAs force us to use feedback amplifier topologies for the TIA design. A shunt-shunt feedback amplifier configuration can be used. In this configuration, the output voltage is sampled by a feedback network and a proportional current mixing is performed at the input. Hence the name shunt-shunt feedback. This results in lowering both the input and output resistances. Hence, such a topology is well suited for a current to voltage conversion.




(a) (b)

Fig. 3.31 (a) A feedback TIA with common gate input stage (Shunt-shunt feedback amplifier); (b) Closed loop small-signal model.

A small-signal analysis can be performed, to identify the small signal parameters of this feedback amplifier. In these kind of feedback amplifiers, it is required to consider the

loading effect of the feedback network ($\beta$ network) on the input and output of the amplifier. An analysis technique based on [40] is followed. The closed loop small-signal model of the common gate shunt-shunt feedback amplifier is shown in Fig. 3.31b. $R_{\beta i}$ and $R_{\beta o}$ are the equivalent resistances seen looking into the $\beta$ network from the input and output of the amplifiers. The open loop small-signal model derived from the closed loop model is shown in Fig. 3.32.

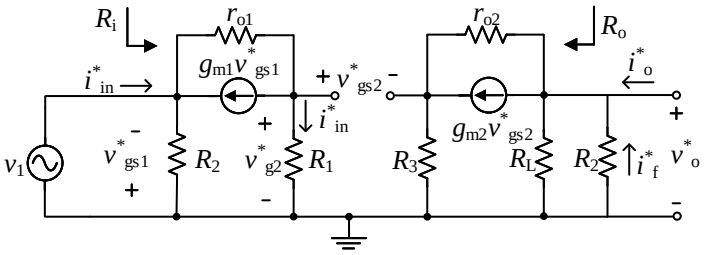



Fig. 3.32 Open loop small-signal model of Fig. 3.31b.

The open loop gain can be expressed as:

$$A_{OL} = \frac{v^*_o}{v^*_{g2}} \cdot \frac{v^*_{g2}}{i^*_{in}} \tag{3.27}$$

The feedback factor can be estimated from the open loop small-signal model in Fig. 3.32.

$$\beta = \frac{i^*_f}{v^*_o} = -\frac{1}{R_2} \tag{3.28}$$

For large values of $A_{OL}$ closed loop gain can be written as:

$$A_{CL} = \frac{v_o}{i_{in}} = \frac{A_{OL}}{1 + A_{OL}\beta} = -R_2 \tag{3.29}$$

This circuit topology still exhibits the problem of output voltage swing. Hence, a feedback TIA where a common-source amplifier as a core amplifier is used for this work. A feedback resistor $R_F$ around this stage provides the required transimpedance gain. A typical implementation of this TIA circuit is shown in Fig. 3.33. The source follower isolates the high impedance node from loading effects of the feedback resistor $R_f$ and also from the input capacitance of the next stage. Additionally, this improves the loop gain of the circuit.

Small-signal analysis can be done to estimate the closed loop parameters of this resistive feedback common-source TIA. The closed loop small-signal model of the circuit in Fig. 3.33 is shown in Fig. 3.34. The loading effect of the feedback resistor is estimated as in the previous circuit topology and the open loop small-signal model is derived. This is illustrated

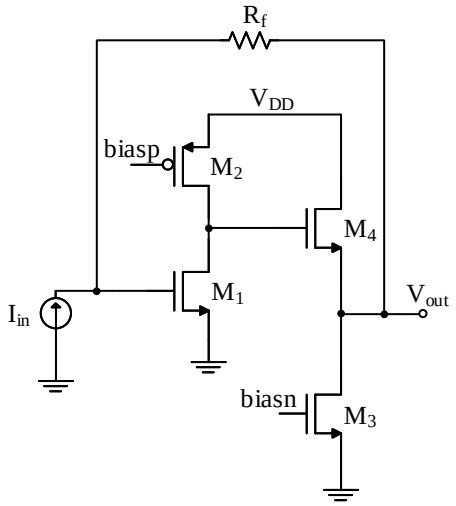



Fig. 3.33 Schematic diagram of a resistive feedback transimpedance amplifier.

in Fig. 3.35. The open-loop circuit parameters are estimated from the open-loop small signal model.

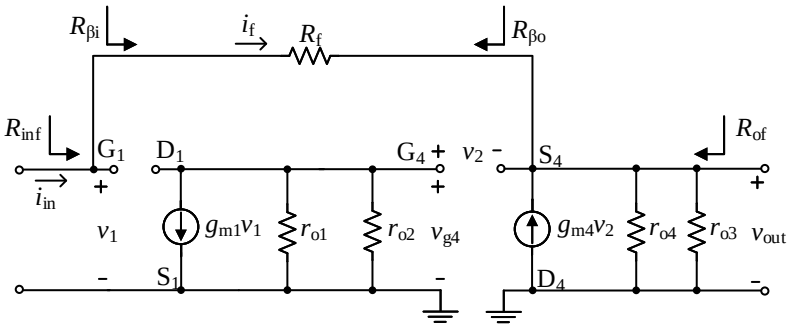



Fig. 3.34 Closed-loop small signal model of the TIA.

Referring to Fig. 3.35, the open loop gain can be written as:

$$A_{\mathrm{OL}} = \frac{v^*_{\mathrm{out}}}{i^*_{\mathrm{in}}} = \frac{v^*_{\mathrm{out}}}{v^*_{\mathrm{g4}}} \cdot \frac{v^*_{\mathrm{g4}}}{i^*_{\mathrm{in}}} \tag{3.30}$$

$$v^*_{\mathrm{out}} = g_{\mathrm{m4}} v^*_2 \left(r_{\mathrm{o4}} \parallel r_{\mathrm{o3}} \parallel R_{\mathrm{f}}\right) \tag{3.31}$$

We can write $v^*_2$ as:

$$v^*_2 = v^*_{\mathrm{g4}} - v^*_{\mathrm{out}} \tag{3.32}$$

We can write (3.31) as:

$$v^*_{\mathrm{out}} = g_{\mathrm{m4}} \left(v^*_{\mathrm{g4}} - v^*_{\mathrm{out}}\right) \left(r_{\mathrm{o4}} \parallel r_{\mathrm{o3}} \parallel R_{\mathrm{f}}\right) \tag{3.33}$$

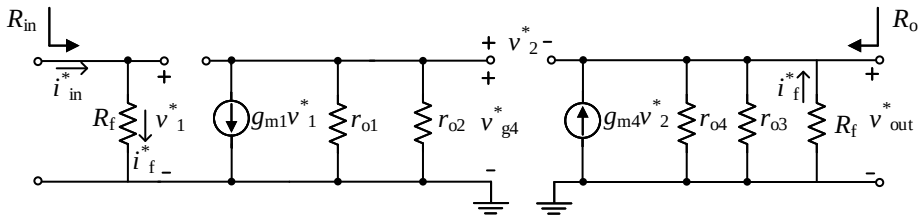



Fig. 3.35 Open-loop small signal model of the TIA.

Rearranging this gives:

$$\frac{v^*_{out}}{v^*_{g4}} = \frac{g_{m4}\left(r_{o4} \parallel r_{o3} \parallel R_f\right)}{1 + g_{m4}\left(r_{o4} \parallel r_{o3} \parallel R_f\right)} \approx 1 \tag{3.34}$$

Now, estimating the 2nd component of (3.30),

$$v^*_{g4} = -g_{m1} v^*_1 \left(r_{o1} \parallel r_{o2}\right) \tag{3.35}$$

$$v^*_1 = i^*_{in} \cdot R_f \tag{3.36}$$

Substituting (3.36) in (3.35) and rearranging, we can write:

$$\frac{v^*_{g4}}{i^*_{in}} = -g_{m1} R_f \left(r_{o1} \parallel r_{o2}\right) \tag{3.37}$$

Combining (3.34) and (3.37) open loop gain can be written now as:

$$A_{OL} = -g_{m1} R_f \left(r_{o1} \parallel r_{o2}\right) \tag{3.38}$$

The open loop input resistance can be estimated as:

$$R_{in} = R_f \tag{3.39}$$

To calculate the output resitance, we apply a test voltage $v_t$ at the output and measure the resulting test current $i_i$. All the other independent sources need to be nulled.

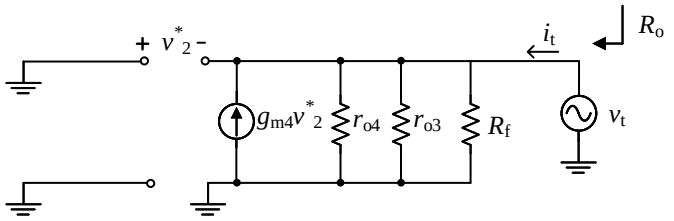



Fig. 3.36 Open loop small-signal model to calculate the output resitance of the TIA.

We can write:

$$v_t = (g_{m4} v_2^* + i_t)\,(r_{o3} \parallel r_{o4} \parallel R_f) \tag{3.40}$$

Substituting for $v_2^* = -v_t$ and rearranging, we get:

$$R_o = \frac{v_t}{i_t} = \frac{r_{o3} \parallel r_{o4} \parallel R_f}{1 + g_{m4}\,(r_{o3} \parallel r_{o4} \parallel R_f)} \approx \frac{1}{g_{m4}} \tag{3.41}$$

To estimate the feedback factor $\beta$, refer the Fig. 3.35. $\beta$ can be written as:

$$\beta = \frac{i_f}{v_{out}^*} \tag{3.42}$$

At the output, we can write:

$$v_{out}^* = -i_f^* R_f \tag{3.43}$$

From this we can write:

$$\beta = \frac{i_f^*}{v_{out}^*} = -\frac{1}{R_f} \tag{3.44}$$

Now, the closed loop parameters of the circuit can be estimated. The closed loop gain can be written as:

$$A_{CL} = \frac{v_{out}}{i_{in}} = \frac{A_{OL}}{1 + A_{OL}\beta} = \frac{-g_{m1} R_f\,(r_{o1} \parallel r_{o2})}{1 + -g_{m1} R_f\,(r_{o1} \parallel r_{o2})\,\frac{-1}{R_f}} \approx -R_f \tag{3.45}$$

The loop gain is calculated as:

$$A_{LG} = 1 + A_{OL}\beta = 1 + -g_{m1} R_f\,(r_{o1} \parallel r_{o2}) \cdot \frac{-1}{R_f} = 1 + g_{m1}\,(r_{o1} \parallel r_{o2}) \tag{3.46}$$

Since, we have a shunt-shunt feedback, the input and output resistances with feedback can be written as:

$$R_{inf} = \frac{R_f}{1 + g_{m1}\,(r_{o1} \parallel r_{o2})} \tag{3.47}$$

$$R_{of} = \frac{\frac{1}{g_{m4}}}{1 + g_{m1}\,(r_{o1} \parallel r_{o2})} \tag{3.48}$$

The bandwidth of the resistive feedback TIA is equal to [38]:

$$f_{-3dB} = \frac{1}{2\pi} \frac{\sqrt{2} A_{OL}}{R_f C_{in}} \tag{3.49}$$

Where, $A_{OL}$ is the open-loop gain of the core amplifier, $R_f$ is the feedback resistance and $C_{in}$ is the total capacitance at the input of the TIA including the parasitic capacitance and the CMUT capacitance.

The input-referred noise current of the circuit is given by [38] :

$$\overline{I_{n,in}^2} = \frac{4kT}{R_f} + \frac{\overline{V_{n,in,core}^2}}{R_f^2} \tag{3.50}$$

In order to have a higher open loop and hence loop gain, a cascoded common source amplifier is used as the core amplifier in the final implementation. This is followed by a NMOS source follower. The circuit is illustrated in Fig. 3.37. The feedback resistor is implemented using a P-doped poly resistor. This type has a relatively high sheet resistance and very low temperature coefficient. Four different resistance values 100 kΩ, 200 kΩ, 250 kΩ and 300 kΩ are provided in the feedback path which can be selected using an SPI interface. Hence, a discrete adjustable gain TIA is implemented. The transistor $M_5$ has its source and bulk connected together to eliminate the body-effect. This lowers the $V_{th}$ of $M_5$ and hence increases the output voltage swing of the TIA. The deep-trench isolation (DTI) provided by the technology allows the NMOS transistors to be placed in its own well. This comes with a small area penalty though.

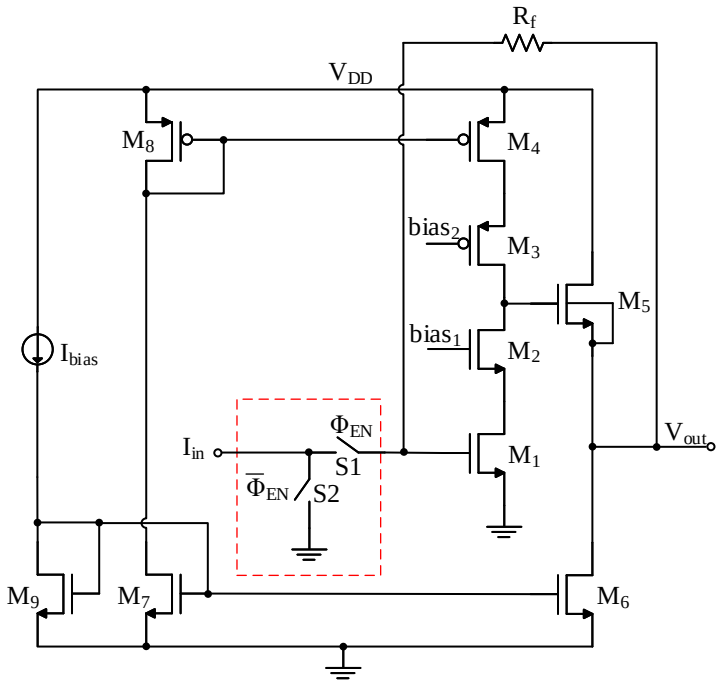



Fig. 3.37 Schematic diagram of the designed resistive feedback transimpedance amplifier.

The switches at the input to change the transceiver from transmit to receive mode are also shown in the red dotted box in Fig.3.37.

### Measurement results

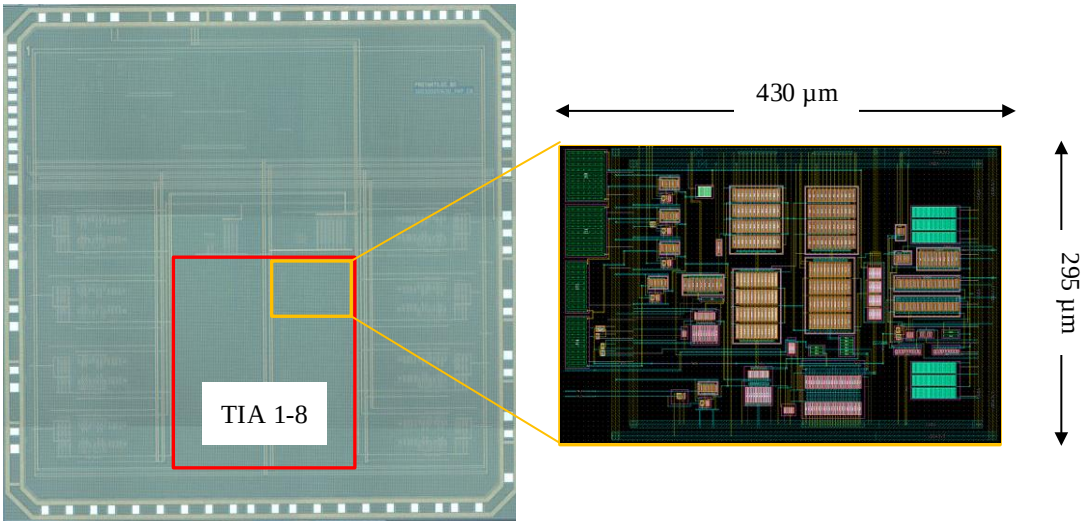



Fig. 3.38 Die photo and the layout of the receiver circuit is highlighted.

The layout of the TIA is highlighted in the die micro-photograph in Fig. 3.38. The frequency response of the TIA is estimated by applying a current input and measuring the output voltage. The frequency response for the four different gain settings is shown in Fig. 3.39. The $f_{-3dB}$ for each case can also be read-out from the figure and can be observed that with increasing gain setting, the bandwidth is reduced as expected. For the highest gain setting of 300 kΩ, an $f_{-3dB}$ of 4 MHz is observed which meets the target specification of the design. The input-referred current noise of the TIA is measured using the noise function of the spectrum analyzer. The current noise spectrum for all the gain settings are shown in Fig. 3.40. At the highest gain setting, an input-referred noise current of 2.6 pA/$\sqrt{\text{Hz}}$ is measured. For smaller gain settings, the noise values can be seen to be increasing.

Since the chip has both HV pulsers and low voltage TIA integrated on the same die, it is important that the TIA circuit is well isolated from the HV pulsers. This crosstalk is measured by pulsing with HV channel 1 and measuring at the output of the channel 1 TIA. The HV pulser is switching at 2 MHz with a peak to peak output of 49 V. The input to the TIA is left open. From the frequency spectrum in Fig. 3.41b it can be seen that there is an isolation of −70 dB between the HV pulser and the TIA. This is negligible and shows that the TIA is well isolated from the HV pulser. This can be attributed to the DTI provided by the technology.

The isolation between adjacent receive channels are also very important in a multi-channel CMUT transceiver ASIC. To evaluate this, a current input is applied to channel 1 TIA and the channel 2 TIA input is left open. The output of both the TIAs are measured. The measured

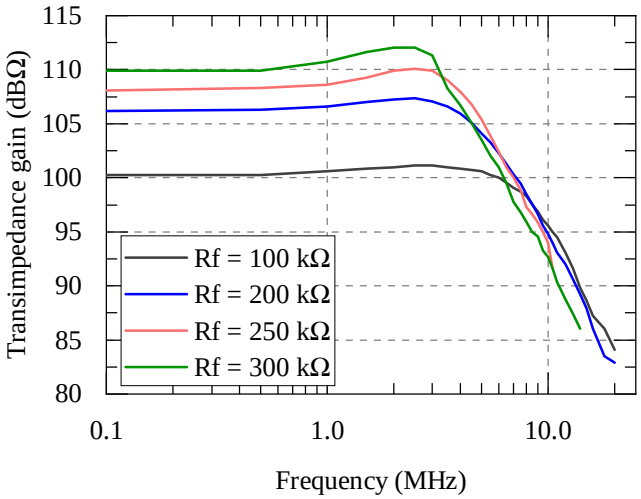



Fig. 3.39 Measured frequency response of the TIA.

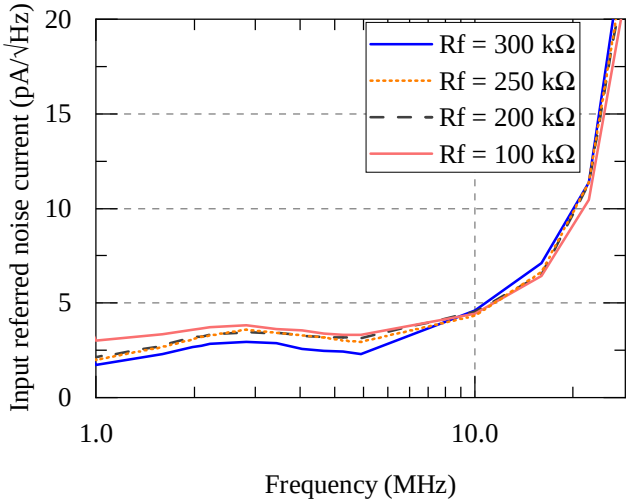
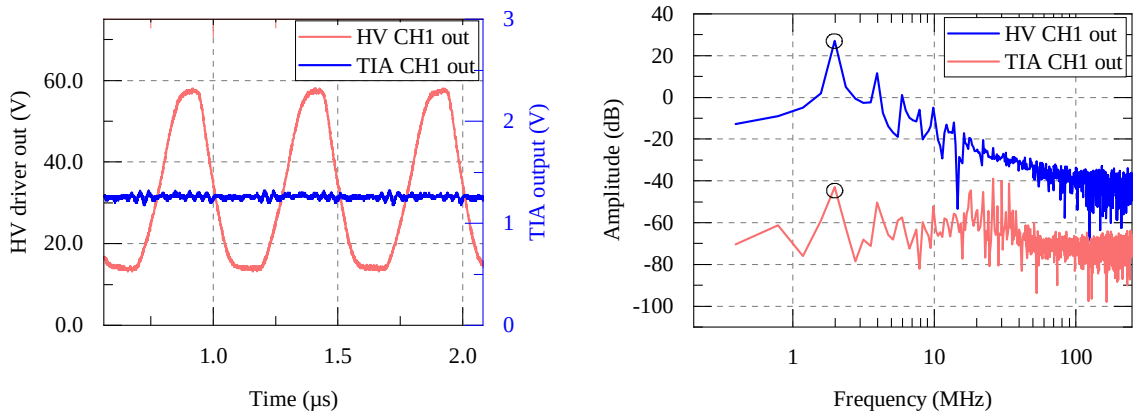



Fig. 3.40 Measured input-referred noise current.

transient and spectrum are shown in Fig. 3.42. It can be noted that the isolation between the two channels is only around −29 dB. This could be due to that fact that the TIAs have poor CMRR due to its single ended topology.

The dynamic range of the TIA is another important parameter. The dynamic range for the TIA is measured for each of the gain setting of the TIA. The measurement data is illustrated in Fig. 3.43. It shows the output voltage of the TIA for different values of input currents. For the highest gain setting of 300 kΩ, we can observe a dynamic range of 34 dB. The bottom left side of the plot shows the noise floor of the TIA. The dynamic range values for each gain setting is listed in table 3.4. As expected it can be seen that the dynamic range decreases drastically with increasing gain. For the lowest gain setting of 100 kΩ, the TIA has a dynamic



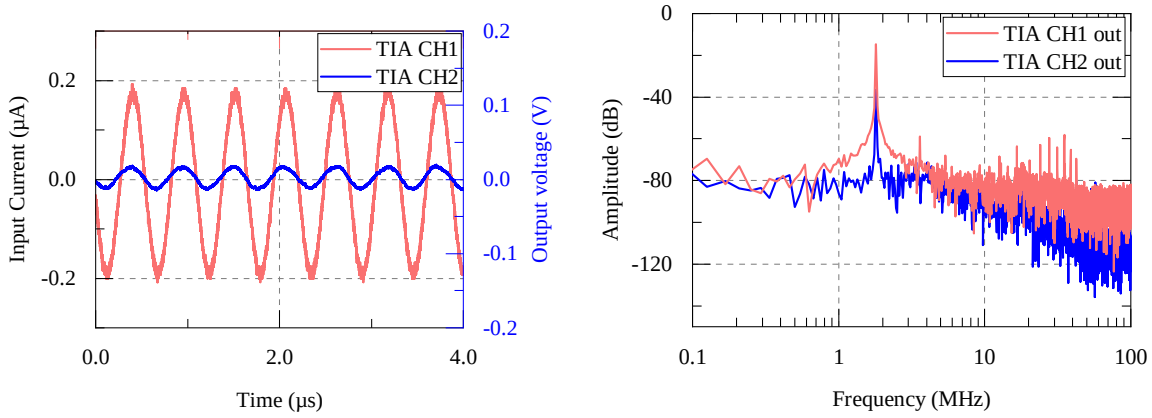

(a) (b)

Fig. 3.41 (a) Measured crosstalk between one HV pulser channel and the TIA of the same channel; (b) Frequency spectrum of the two circuits.

range of 47 dB. A TIA that is optimized for power consumption and area is designed in the final chip version ProTaktilUS_C0, which is presented in the next section.

Table 3.4 Dynamic range of the TIA for different gain setting.

| Feedback resistor | Dynamic range |
|---|---|
| Rf = 100 kΩ | 47 dB |
| Rf = 200 kΩ | 42 dB |
| Rf = 250 kΩ | 37.5 dB |
| Rf = 300 kΩ | 34 dB |




(a) (b)

Fig. 3.42 (a) Measured crosstalk between two adjacent receive channels; (b) Frequency spectrum of the two channels.

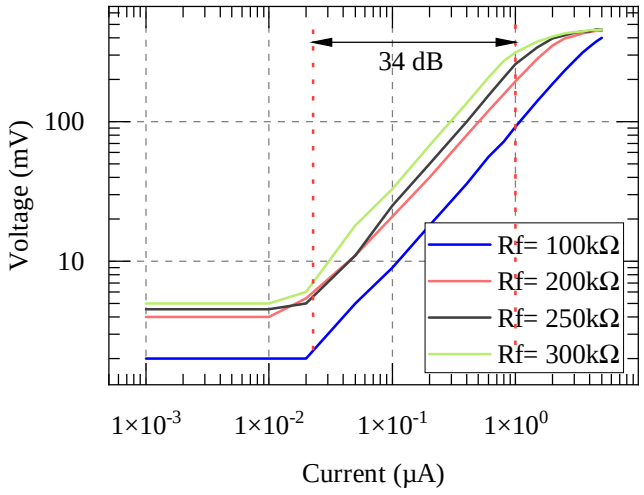
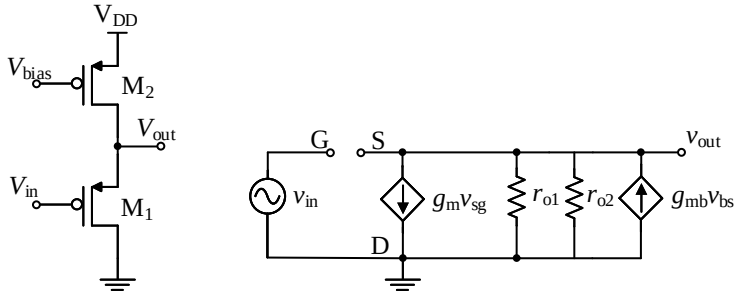



Fig. 3.43 Measurement data showing the TIA dynamic range.

## Super source follower

Source follower circuits are a widely used building blocks. They allow voltage source at high impedance to be transferred to a low-impedance voltage source. The output voltage follows the input with a level shift up or down depending on if it is NMOS or PMOS based.




(a) (b)

Fig. 3.44 (a) A PMOS source follower; (b) small-signal equivalent circuit.

Small-signal analysis can be performed to find the voltage gain and the output resistance of the circuit. By applying KCL at the source node, we have

$$g_{\mathrm{mb}}V_{\mathrm{bs}} = g_{\mathrm{m}}V_{\mathrm{sg}} + \frac{V_{\mathrm{out}}}{r_{\mathrm{o1}}} + \frac{V_{\mathrm{out}}}{r_{\mathrm{o2}}} \tag{3.51}$$

From the circuit inspection, we have $V_{\mathrm{bs}} = V_{\mathrm{b}} - V_{\mathrm{s}} = -V_{\mathrm{out}}$ and $V_{\mathrm{sg}} = V_{\mathrm{out}} - V_{\mathrm{in}}$. Also assuming $r_{\mathrm{o1}} = r_{\mathrm{o2}} = r_{\mathrm{o}}$ and substituting this into (3.51), we get the voltage gain as:

$$A_{\mathrm{v}} = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{g_{\mathrm{m}}}{g_{\mathrm{m}} + g_{\mathrm{mb}} + \frac{2}{r_{\mathrm{o}}}} \tag{3.52}$$

Since the value of $r_o$ is very high we can write the gain equation as:

$$A_{\mathrm{v}} = \frac{g_{\mathrm{m}}}{g_{\mathrm{m}} + g_{\mathrm{mb}}} = \frac{1}{1+\eta} \tag{3.53}$$

If we ignore the body effect, we can see the the voltage gain of the source follower $A_{\mathrm{v}} \approx 1$.

The output resistance of the source follower can be estimated from the small-signal model in Fig. 3.44 by nulling the input voltage source and applying a test voltage $V_t$ at the output. Again assuming the output resistance of the MOSFET's $r_o$ is a large value, we get:

$$R_{\mathrm{out}} = \frac{1}{g_{\mathrm{m}} + g_{\mathrm{mb}}} \tag{3.54}$$

This value will be a few kΩ. This is not really that low. When driving low resistance loads, this value of output resistance is not small enough and will lead to loading effect on the buffer. Another requirement for voltage buffers is that they should have fast settling

performance which is not limited by slew rate. The conventional source follower shown in Fig. 3.44 is of type class A. The slew rate is limited by the bias current. There is a trade-off between slew rate and power consumption. Class AB voltage followers are desired to have an improved slew rate performance without large power consumption. The class AB circuits provide a dynamic load current which is much higher than the biasing current during a large input voltage transient. This can be expressed as the current boosting factor (CBF) [41] which can be written as:

$$\text{CBF} = \frac{I_{\text{out(max)}}}{I_{\text{bias}}}$$

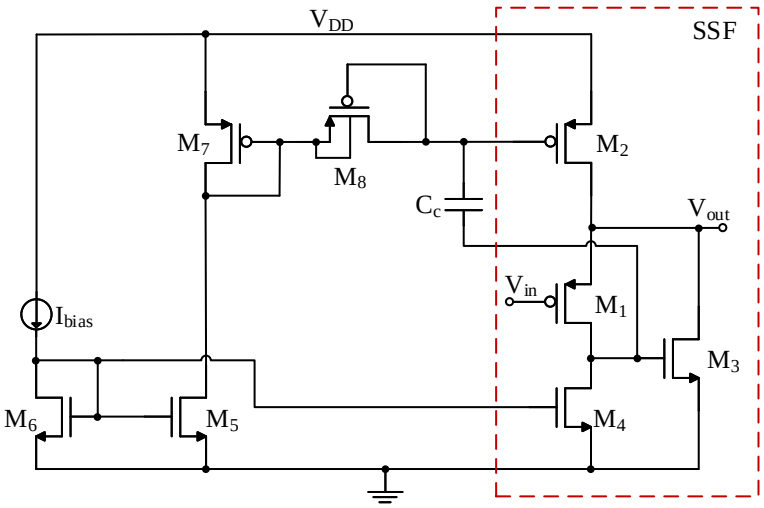



Fig. 3.45 Schematic diagram of a super source voltage follower.

A super source follower (SSF) architecture is used to achieve high CBF and low output resistance. A PMOS class AB super source follower is illustrated in Fig. 3.45. The SSF part is highlighted with the dotted red box. The transistor $M_3$ provides a negative feedback. When there is an increase in current through $M_1$, this causes the gate of $M_3$ also to go up which results in the source of $M_1$ getting pulled down. This eventually results in a reduced overdrive voltage for $M_1$ which lowers the current. This confirms negative feedback. As a result of this applied negative feedback, the output resistance is further lowered. This can be proven using the small-signal model from Fig. 3.46. The voltage gain of the SSF is first derived. The body transconductance $g_{\text{mb}}$ is ignored. Applying KCL at the $v_{\text{out}}$ node we can write:

$$g_{\text{m3}} v_{\text{gs3}} + \frac{v_{\text{out}}}{r_{\text{o2}}} + \frac{v_{\text{out}}}{r_{\text{o3}}} + \frac{v_{\text{gs3}}}{r_{\text{o4}}} = 0 \tag{3.55}$$

$$v_{\text{out}} \left( \frac{1}{r_{\text{o2}}} + \frac{1}{r_{\text{o3}}} \right) + v_{\text{gs3}} \left( g_{\text{m3}} + \frac{1}{r_{\text{o4}}} \right) = 0 \tag{3.56}$$

Applying KCL at the gate of $M_3$, we get:

$$g_{m1}v_{sg1} + \frac{v_{out} - v_{gs3}}{r_{o1}} - \frac{v_{gs3}}{r_{o4}} = 0 \tag{3.57}$$

$$v_{gs3} = \frac{v_{out}\left(g_{m1} + \frac{1}{r_{o1}}\right) - g_{m1}v_{in}}{\frac{1}{r_{o1}} + \frac{1}{r_{o4}}} \tag{3.58}$$

Since $\frac{1}{r_{o1}} \ll g_{m1}$, we can write (3.58) as

$$v_{gs3} = (v_{out}g_{m1} - g_{m1}v_{in})(r_{o1} \parallel r_{o4}) \tag{3.59}$$

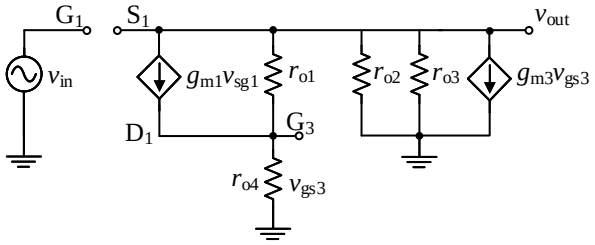



Fig. 3.46 Small-signal equivalent circuit of the super source voltage follower.

Substituting (3.59) into (3.56),

$$v_{out}\left(\frac{1}{r_{o2}} + \frac{1}{r_{o3}}\right) + g_{m1}(v_{out} - v_{in})(r_{o1} \parallel r_{o4})g_{m3} = 0 \tag{3.60}$$

If we assume the small-signal output resitances of all the transistors to be $r_o$, we can write (3.60) as,

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}g_{m3}r_o/2}{\frac{2}{r_o} + g_{m1}g_{m3}r_o/2} \approx 1 \tag{3.61}$$

The output resistance of the SSF can be calculated by nulling the input voltage source and applying a test voltage $v_t$ at the output node and measuring the test current $i_t$. Applying KCL at node $v_t$, we get:

$$g_{m3}v_{gs3} + \frac{v_t}{r_{o3}} + \frac{v_t}{r_{o2}} + \frac{v_{gs3}}{r_{o4}} = i_t \tag{3.62}$$

$$v_t\left(\frac{1}{r_{o3}} + \frac{1}{r_{o2}}\right) + v_{gs3}\left(g_{m3} + \frac{1}{r_{o4}}\right) = i_t \tag{3.63}$$

Writing the KCL at the node $G_3$ we get:

$$\frac{v_{gs3}}{r_{o4}} = g_{m1}v_t + \frac{v_t - v_{gs3}}{r_{o1}} \tag{3.64}$$

$$v_{gs3} = \frac{\left(g_{m1} + \frac{1}{r_{o1}}\right) v_t}{\frac{1}{r_{o1} \| r_{o4}}} \tag{3.65}$$

As $\frac{1}{r_{o1}} \ll g_{m1}$,

$$v_{gs3} = g_{m1} v_t \left(r_{o1} \parallel r_{o4}\right) \tag{3.66}$$

Substituting (3.66) into (3.63),

$$\frac{v_t}{i_t} = \frac{1}{\frac{1}{r_{o3} \| r_{02}} + g_{m1} g_{m3} \left(r_{o1} \parallel r_{o4}\right)} \tag{3.67}$$

Since the values of output resistances are quite high, we can approximate this as:

$$R_{out} = \frac{v_t}{i_t} = \frac{1}{g_{m1} g_{m3} \left(r_{o1} \parallel r_{o4}\right)} \tag{3.68}$$

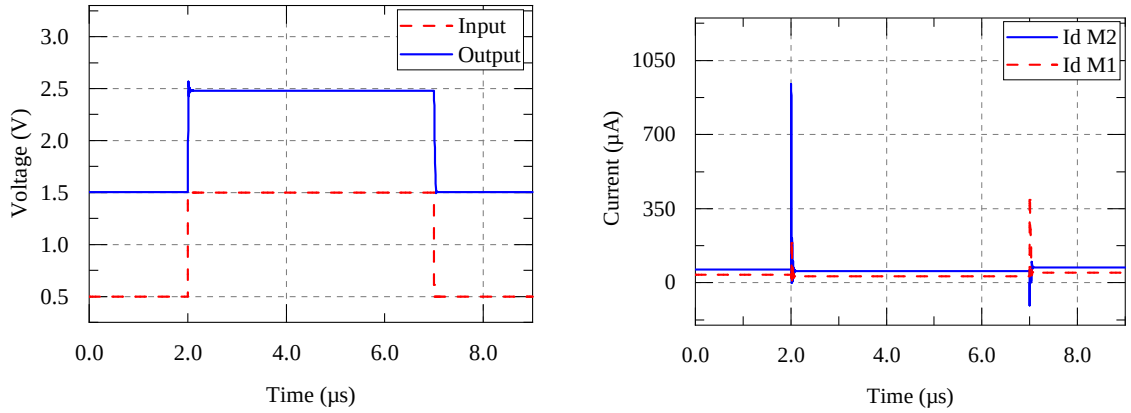
Comparing (3.68) with (3.54), it can be seen that the output resistance for the super source follower is a lot smaller than the conventional source follower by roughly a factor of $g_{m3} \left(r_{o1} \parallel r_{o4}\right)$ . The circuit has an input common mode range given by;

$$V_{in(min)} \geq V_{GS3} - V_{THP} \tag{3.69}$$

$$V_{in(max)} \leq V_{DD} - V_{SD,sat} - V_{SG,M1} \tag{3.70}$$

The class AB operation of the SSF is achieved by using a quasi floating gate transistor (QFG) [41]. It is a MOSFET with a weak gate connection to the DC bias voltage. This can be achieved using a large resistor. Referring to Fig. 3.45, the transistor $M_2$ is the QFG device. The transistor $M_8$ is in cut-off and provides the large resistance needed to weakly connect the gate of $M_2$ to the biasing voltage. This sets the quiescent current in the output branch accurately. A large transient voltage at $V_{in}$ causes the gate of $M_3$ to move in the opposite direction. The variation at this node is transferred to the gate of $M_2$ with the high pass filter formed by $C_c$ and $M_8$. The current in $M_2$ is not limited by the bias current. Hence the follower operates as class AB. As $M_8$ operates in cut-off region, it offers are very large resistance in the GΩ region. As a result, the cut-off frequency will be under 1 Hz and blocks the DC effectively.

A SSF with a quiescent current of 25 µA is designed. The simulation result showing the step response can be seen in Fig. 3.47a. A 1 V input voltage step is applied and the output is plotted. The drain currents through the transistors $M_1$ and $M_2$ are also shown. The push pull




(a) (b)

Fig. 3.47 (a) Simulated response of the SSF to a step input voltage; (b) Drain currents of the transistors $M_2$ and $M_1$.

Table 3.5 Performance parameters of the super source follower

| Parameter | Value |
|---|---|
| SR+ | 87 V /µs |
| SR- | 27 V /µs |
| Load cap | 10 pF |
| CBF | 15 A/A |
| Input noise | 68 nV /$\sqrt{Hz}$ @ 2 MHz |
| Quiescent power | 376 µW |

action can be seen by the large dynamic currents during the pulse edges. As illustrated, this current is much higher than the quiescent current. An output load capacitance of 10 pF is used for the simulations.

The complete receiver front-end combining the low power TIA and the super source follower is designed. The circuit performance has been verified using post-layout simulations. The laboratory measurement results of this circuit block is not available at the time of writing this thesis as the chip is still under fabrication. The layout of the complete receiver circuit with the TIA followed by the SSF is shown in Fig. 3.48. The circuit occupies a total area of 0.04 $mm^2$.

In table 3.6 the performance parameters of the two versions of the TIA are listed and compared with prior art. The TIA on the chip version A0 is mentioned as TIA_A0 (measurement values) and the TIA on the final chip version is mentioned as TIA_C0 (simulation results) in the table. It can be seen that this work compares favorably with the listed works in terms of large transimpedance gain and low noise performance. This design also occupies the smallest

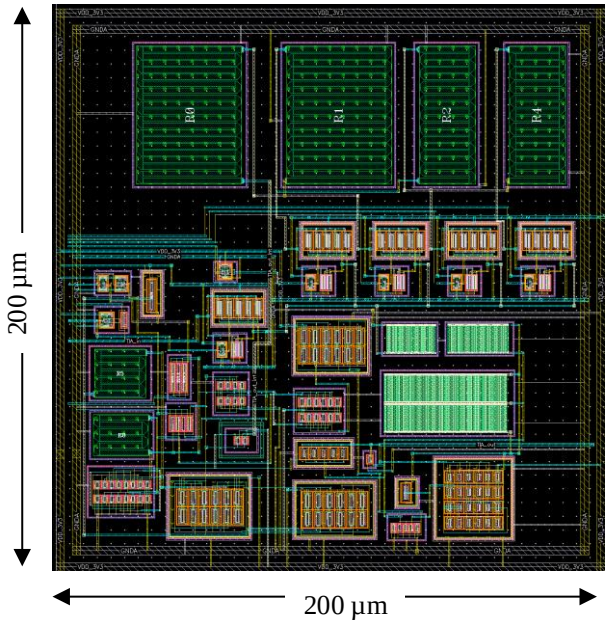



Fig. 3.48 Layout of the TIA with super source follower.

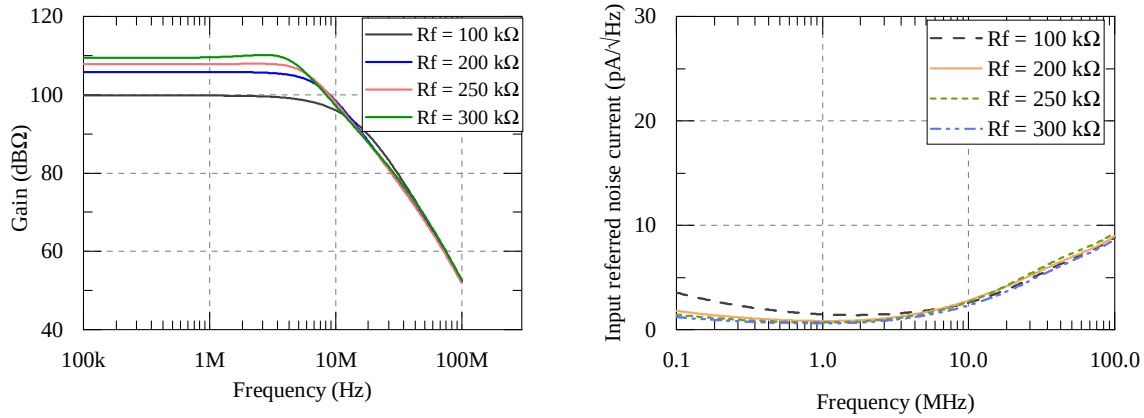
area. The bandwidth is on the lower side as compared to the state of the art. This can be attributed to the high value of the feedback resistor used. The power consumption is also comparable. However the listed work in [29] reports extremely low power consumption with similar performance parameters. The new TIA version improves on the power consumption a lot. An FOM can be used to compare the different works. This is a slightly modified FOM as reported in [39] and [42] by removing the input capacitance as all the works do not report the input capacitance values.

$$FOM = \frac{\sqrt{BW\,[\mathrm{GHz}]}R_{\mathrm{T}}\,[\Omega]}{\mathrm{Noise}\left[\mathrm{pA}/\sqrt{\mathrm{Hz}}\right]P\,[\mathrm{mW}]} \tag{3.71}$$

From the FOM numbers, it can be seen that the A0 version of the TIA shows poor performance when compared with the state of the art. The power consumption and area occupied are on the higher side for this design. The C0 version with the new TIA design can be seen to improve massively on these numbers and achieve the best FOM compared to the state of the art.

Table 3.6 Measured performance parameter of the TIA circuit compared with prior art

| Parameter | TIA_A0 | TIA_C0 | [43] | [12] | [29] | [44] |
|---|---|---|---|---|---|---|
| Gain (dBΩ) | 109 | 105.8 | 87-99 | 15-32 dB(LNA) | 95.1 | 108-119 |
| Bandwidth (MHz) | 4.7 | 6.6 | 20 | 11 | 12 | 16 |
| Input Noise ($pA/\sqrt{Hz}$) | 2.6 | 0.95 | 4nA (rms) | 4.1 $nV/\sqrt{Hz}$ | 3.5 | 1.96 |
| Dynamic range (dB) | 34 | 46 | 71 | NA | NA | 53 |
| Area ($mm^2$) | 0.1 | 0.04 | 0.3 | N.A | 0.15 | 18 |
| Power (mW) | 6.6 | 1 | 6 | 6.26 | 0.38 | 3.3 |
| FOM | 1198 | 9030 | 2330 | - | 4678 | 4889 |




(a) (b)

Fig. 3.49 (a) Gain of the receiver; (b) Input referred noise of the receiver.

## 3.5 Start-up clamp circuit

The CMUT transceiver chip has multiple power supplies on the chip. For this work, we have a 3.3 V used as the low voltage supply, 60 V and 15 V as high voltage power supplies which are applied externally. Two on-chip HV linear regulators produce 56 V and 11 V internally. The HV SOI process which is used for design can support up to 200 V for $V_{DS}$ and $V_{BS}$, however the maximum $V_{GS}$ that can be supported is 5.5 V. Hence, care must be taken to make sure that this limit is not exceeded at any point in time. In these kind of multi-voltage systems, the power up is really crucial. As explained in the section 3.2.3, the MOSFETs $M_3$ and $M_4$ are biased by the HV linear regulators. These linear regulators take a finite amount of time to power up to their designed voltages. However, the HV supplies $V_{DDH,HS}$ and $V_{DDH,LS}$ which are supplied externally are ramped up with a faster slew-rate. So this puts the gate of the transistors $M_3$ and $M_4$ under the risk of breakdown. Hence, a start-up clamp circuit is designed which pulls the gate of $M_3$ and $M_4$ to $V_{DDH,HS}$ and $V_{DDH,LS}$ until the HV linear regulators reach their designed voltage levels. A block diagram of this start-up clamping circuit is shown in Fig. 3.50.

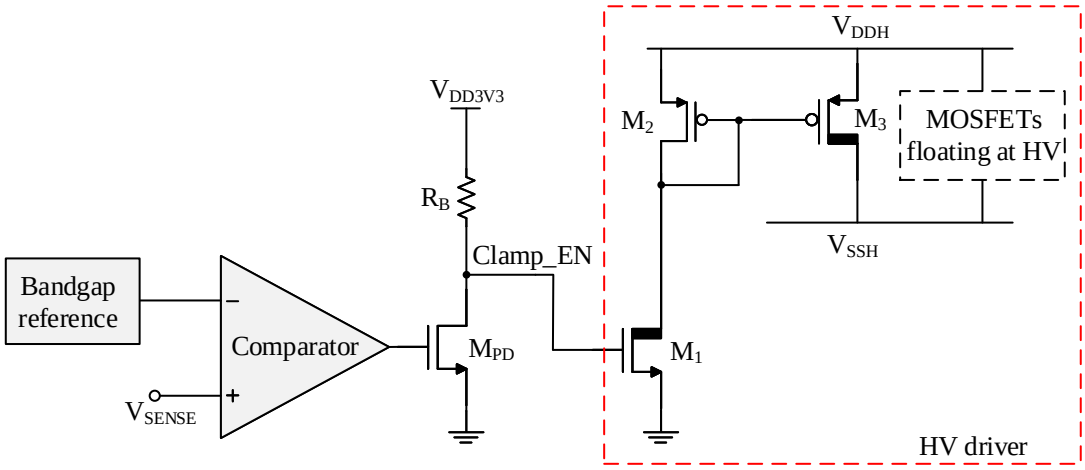



Fig. 3.50 Block diagram of the start-up monitor circuit.

It is assumed that the low voltage power supply comes up before all the HV supplies. This can be easily done externally using a supervisor IC. A comparator is used to compare the fedback voltage of the HV regulator ( we can call it $V_{sense}$) to the output of a bandgap voltage reference. The bandgap is designed to produce a voltage of 1 V. Initially, when only the 3.3 V is available, the $V_{sense}$ is at 0 V and the comparator output is low. This makes Clamp_EN to go to high. $M_1$ is turned on and pulls the gate of $M_2$ low. $M_2$ can be sized to make sure that the $V_{SG}$ is within the limits. This turns on $M_3$ and the nodes of the floating transistors are pulled to $V_{DDH}$.

The $V_{sense}$ voltage will be at 1.2 Vwhen the HV regulator reaches its designed value. When the $V_{sense}$ goes above the bandgap voltage, the comparator output goes high and turns on the MOSFET $M_{PD}$. This pulls down the node Clamp_EN turning off $M_1$. This turns off $M_2$ and $M_3$ resulting in the release of the clamp.

### 3.5.1 Bandgap reference circuit

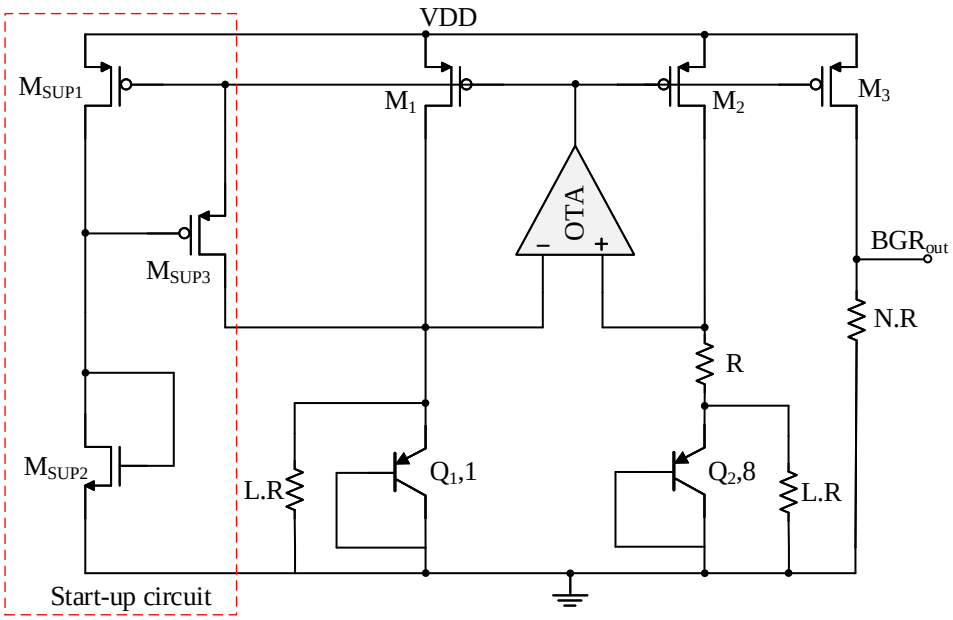



Fig. 3.51 Schematic of the 1 V bandgap voltage reference circuit.

The schematic diagram of the 1 V bandgap voltage reference circuit is shown in Fig. 3.51. The circuit follows the same design principle as in [45]. This circuit topology allows the design of bandgap reference circuit with voltages different from the standard 1.2 V output. The main idea here is to split the total current into a CTAT and PTAT values and then the sum of these two values are driven through an output resistance to produce a voltage which is constant with respect to temperature. It can be shown that the output voltage of the BGR circuit can be written as:

$$V_{\mathrm{REF}} = n.V_{\mathrm{T}}.N.ln(K) + \frac{N}{L}.V_{\mathrm{Q1}} \tag{3.72}$$

To get the variation of the BGR voltage with temperature, a derevative of (3.72) can be taken. This gives:

$$\frac{\partial V_{\mathrm{REF}}}{\partial T} = n.N.ln(K).\frac{\partial V_{\mathrm{T}}}{\partial T} + \frac{N}{L}.\frac{\partial V_{\mathrm{Q1}}}{\partial T} \tag{3.73}$$

In order to achieve a zero temperature coefficient for the BGR, we need the reference voltage to stay constant with temperature. Equating (3.73) to zero gives:

$$L = \frac{-\frac{\partial V_{Q1}}{\partial T}}{n.ln(K).\frac{\partial V_T}{\partial T}} \tag{3.74}$$

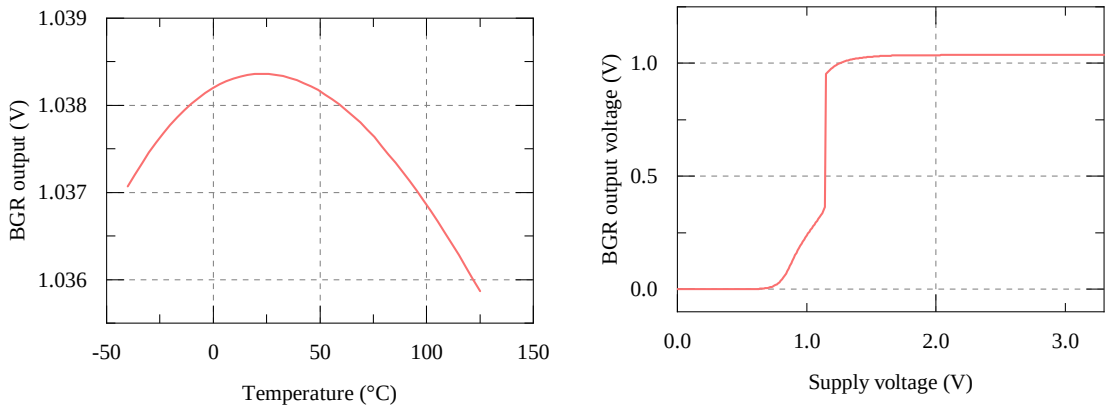
For this design we use K=8. Also the terms $\frac{\partial V_{Q1}}{\partial T}$ and $\frac{\partial V_T}{\partial T}$ can be accurately determined by simulations. To design for a particular reference voltage, (3.72) can be re-written as:

$$N = \frac{V_{REF}}{n.V_T.ln(K) + \frac{V_{Q1}}{L}} \tag{3.75}$$

The design values for the BGR circuit is listed in table 3.7.

Table 3.7 Design values for the BGR circuit

| Parameter | Value (in $\mu m$) |
|---|---|
| L | 9.6 |
| N | 8.3 |
| R | 9 kΩ |
| Ibias | 2 µA |




(a) (b)

Fig. 3.52 (a)Post-layout simulation showing the BGR output voltage against temperature sweep; (b) BGR output variation with a dc sweep of the supply voltage.

The post-layout simulation results of the BGR circuit is shown in Fig. 3.52. In Fig. 3.52a, the output voltage is plotted against the temperature variation from -40°C to +125°C. The temperature coefficient can be calculated as:

$$\mathrm{TC}_{V_{ref}} = \frac{V_{\max} - V_{\min}}{V\,(@T_{\mathrm{ref}})\,.\,(T_{\max} - T_{\min})} \cdot 10^6 ppm/^{\circ}C \tag{3.76}$$

This is calculated to be 28 ppm/°C. In Fig. 3.52b, the BGR output voltage is plotted against the variation of the input supply voltage. It can be seen the BGR can start up with a minimum supply voltage of 1.3 V. This is limited by the output voltage of the circuit.

### 3.5.2 Symmetric OTA

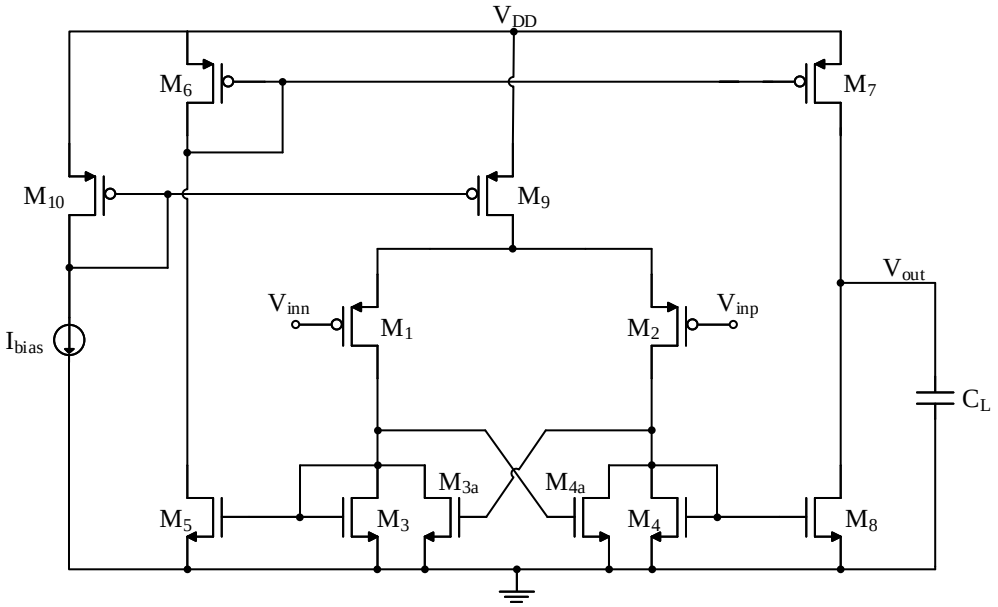



Fig. 3.53 Schematic of the OTA used as comparator.

A symmetric OTA with a partial positive feedback gain boost is used as the comparator for the clamp release circuit. This is the same topology used in the section 3.3. To demonstrate the performance of the complete start-up protection circuit, post-layout simulations are performed on the complete system combining the HV pulser, HV linear regulator and the start-up clamp circuit. This is illustrated in Fig. 3.54. It can be seen in 3.54(a) that at circuit power-up, when the HV supplies are not turned ON, the Clamp_EN signal is high. Later when the HV supplies are powered up, the pull-up transistor $M_3$ in Fig. 3.50 pulls up the node $V_{SSH}$ and it tracks the $V_{DDH}$. Once, the voltage at node $V_{SENSE}$ goes above the reference voltage, the Clamp_EN signal goes low and the $V_{SSH}$ settles to the regulator output voltage. This way it can be ensured that the floating devices can be protected during chip start-up. The only condition that needs to be maintained is that the low voltage supply needs to be powered before the HV supplies. This can be easily ensured at the PCB level using an off the shelf supervisor IC.

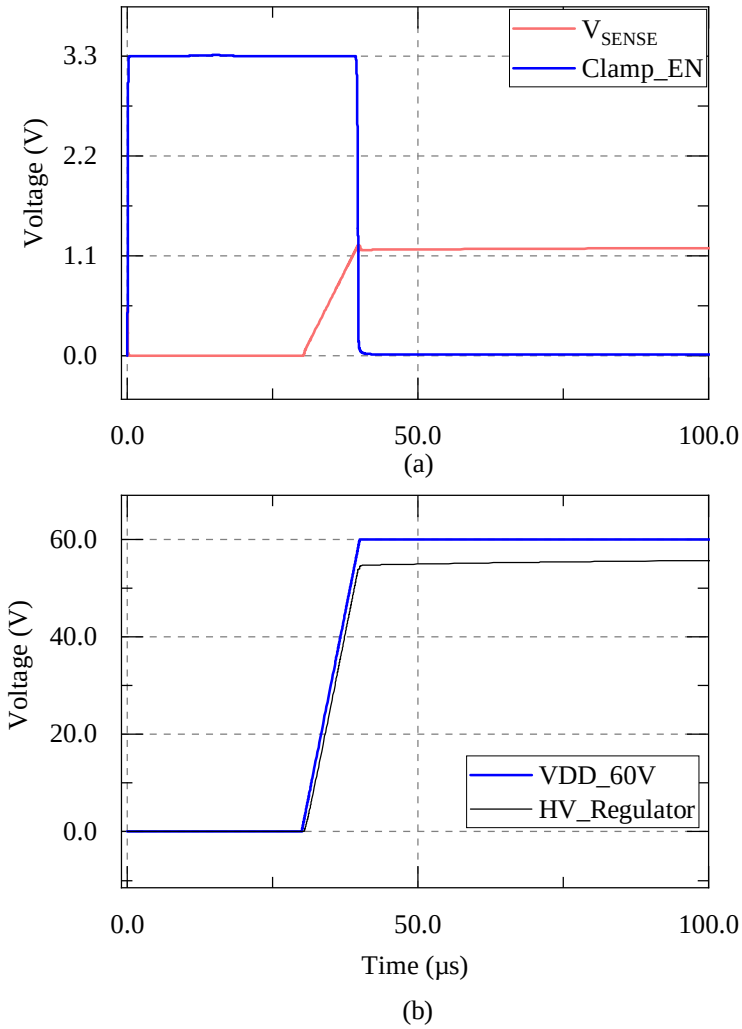



Fig. 3.54 (a) Plot showing the operation of the clamp circuit; (b) the 60 V power supply ramp-up and the ramp-up of the 56 V linear regulator is also shown here.

## 3.6 Transceiver Chip Performance and Comparison to State of the Art

Three versions of the transceiver chip have been designed each with incremental performance improvements and feature addition. Two versions of chips have been fully characterized in the lab. In the table 3.8, the performance summary of the designed transceiver ASIC is presented and a comparison with state of the art is made (CMUTs and piezoelectric based transducers are both included). Even though, an accurate comparison of certain parameters is difficult due to the fact that the targeted application and specifications are different, it can be seen that this work compares positively in terms of power consumption from the HV supply. Our work integrates the HV driver including level shifters and can achieve power

levels better than the state of the art listed in the table except [44] which has lower power consumption from the HV supply. However this work does not include on chip HV pulsers. The noise performance also compares favorably which shows that the removal of the HV switch from the receive path indeed improves the noise performance. The peak to peak pulse amplitude and frequency of operation is also one of the highest. It can also be seen that only in our work, the HV biasing of CMUTs is moved on-chip. For this reason, the chip active area is slightly on the higher side for our work compared to the state of the art.

To summarize, it can be concluded that this research work advances the state of the art designs of the ultrasonic transceiver ASIC by removing the external bias tee circuit and obtaining performance parameters that are comparable with the other works. A multi-channel interface ASIC is developed that can be successfully used for a pulse-echo operation with a CMUT array.

Table 3.8 System level comparison with state of the art

| Parameter | This Work | [46] | [11] | [12] | [29] | [30] | [44] |
|---|---|---|---|---|---|---|---|
| Technology | 0.18$\mu$m HV SOI | 0.18$\mu$m HV BCD | 0.18$\mu$m HV CMOS | 0.18$\mu$m HV BCD | 0.18$\mu$m CMOS | 0.35$\mu$m HV CMOS | 0.18$\mu$m HV CMOS |
| Transducer type | CMUT | CMUT | CMUT | CMUT | CMUT | CMUT | PZT |
| Transmit circuit | HV pulser | HV pulser | HV pulser | HV pulser | HV pulser | HV pulser | Switch |
| HV biasing | Internal | External | External | External | External | External | N.A |
| Channels | 8 | 16TX/1RX | 16 | 64 | 1 | 4 | 16TX/64RX |
| Pulse voltage ($V_{pp}$) | 49 | 58 | 30 | 60 | 15 | 30/60 | 28 |
| Pulse frequency (MHz) | 8 | 5 | 32-42 | 7 | 2.6 | 1.38 | 13 |
| Output load (pF) | 15 | 25 | 18 | 15 | 12 | 18 | 0.7 |
| Power(mW)@supply (V) | 12@60 | 3.6mW@1.8 | 44@44 | 300mW/ch (static) | N.A | 98@30 | 9.1 |
| Active area($mm^2$) | 6 | 2.6 | 1.5 | 28.6 | 0.15 | 3.9 | 1.8 |
| TIA Gain (dB$\Omega$) | 100-109 | 74-90 | 99 | 32 dB(LNA) | 95.1 | 110 | 108-119 |
| Input Noise (pA/$\sqrt{\text{Hz}}$) | 2.6 | 2-3 | 1.93 | 4.1 nV/$\sqrt{\text{Hz}}$ | 3.5 | 0.5 | 1.96 |
| TIA BW (MHz) | 4.7-8 | 2-4 | 25 | 11 | 12 | 9 | 16 |

### Pulse-echo operation

To test the system level operation of the transceiver ASIC, pulse-echo operations are performed using a single element CMUT sample. As the CMUT samples available for testing have a voltage requirement lower than the default operational values of the ASIC, the internal HV linear regulators are turned off and the appropriate voltages are applied externally from a power supply. For the first system measurement, a CMUT designed for airborne application is used. The CMUT parameters are listed in the table 3.9. 25 V pulses at 1.95 MHz frequency are applied with a 10 µs transmit time. The pulse burst is applied at every 1 ms.

Table 3.9 Parameters of the CMUT used for testing

| Parameter | Value |
|---|---|
| Capacitance | 17.09 pF |
| Impedance | 0.93 MΩ |
| Resonance frequency (at 25V DC bias) | 1.95 MHz |

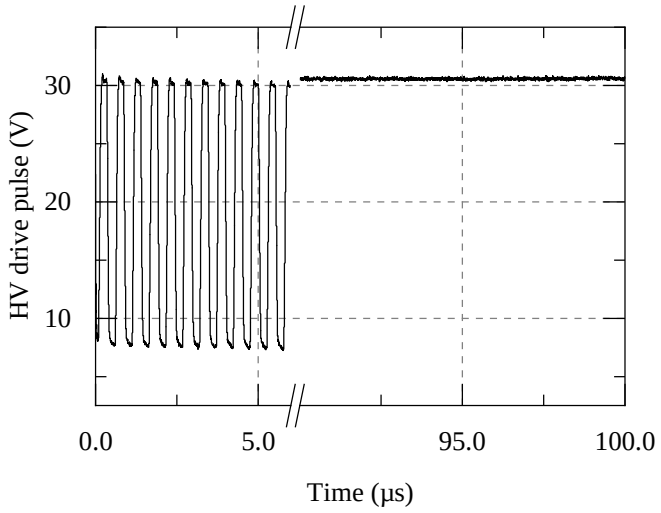



Fig. 3.55 High voltage pulses applied to the airborne CMUT under test.

The result of the pulse-echo operation is shown in Fig. 3.55 and 3.56. The measurement is performed in air. It can be noted that the distance measured is quite low which shows the high attenuation of the ultrasound waves in air. Also the CMUTs operated in air has a very low fractional bandwidth. This requires the HV pulses to be very close to the CMUT resonant frequency to actuate it and produce and high amplitude acoustic signal.

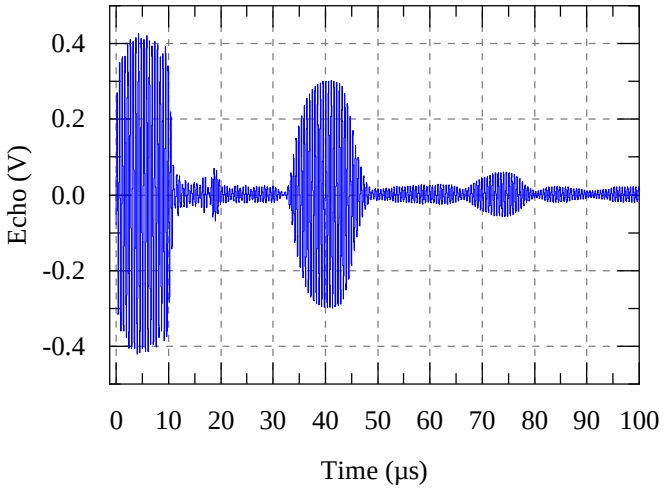



Fig. 3.56 Echo received at the output of the transimpedance amplifier measured by oscilloscope with the target at approximately 1 cm from the CMUT.

A second pulse-echo operation is performed with another CMUT optimized for fluid operation. A test set up is built using a glass beaker and silicone oil. As silicone oil is non-conducting, the immersion measurement can be performed safely. The CMUT chip is wire bonded on a interface PCB and connected to the transciever chip board using flexible cables. The CMUT parameters are listed in the table 3.10

Table 3.10 Parameters of the CMUT used for fluid testing

| Parameter | Value |
|---|---|
| Capacitance | 18 pF |
| Resonance frequency | 4 MHz |
| Pull-in voltage | 19 V |

The measurement result is shown in Fig. 3.57. The test is performed with the CMUT PCB placed 3 cm away from the beaker wall. In the transmit mode, 7 V peak to peak pulses switching between 18 V and 11 V are applied. The number of pulses are set to 10 and the pulse frequency is set to 4.4 MHz. In the receive mode, the CMUT is biased at 18 V. As it can be seen, strong echo signals are measured at the output of the TIA. The wide bandwidth operation of the CMUT in liquid is verified by performing pulse-echo operation for pulse frequencies in the range from 2 MHz to 6 MHz

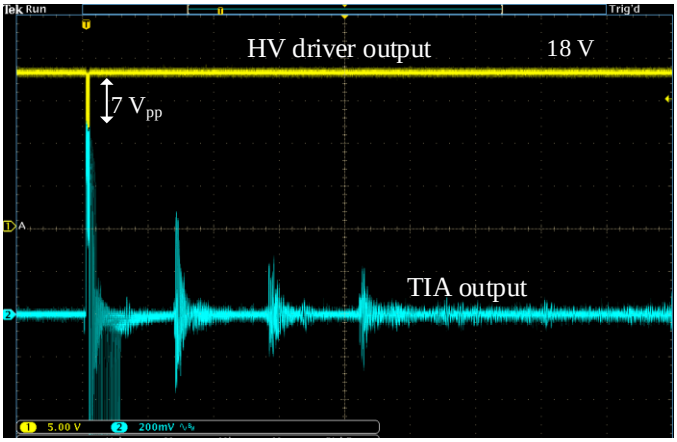



Fig. 3.57 Pulse-echo measurement result of the low voltage CMUT immersed in silicone oil.

# Chapter 4

# Transmit Beamforming Circuit Design

## 4.1 Introduction

To create an image using an ultrasonic transducer, it is necessary to focus the ultrasound beam to a point of interest and then to move it to the next point. So basically, the beam needs to be focused and steered. The beamforming can be achieved in several ways. The simplest construction is a single element transducer. In such devices, the size of the transducer determines the point where the beam is focused. This point is known as the natural focal point and can be expressed as mentioned in [47] as:

$$Z_t = 0.339\frac{L_y^2}{\lambda} \tag{4.1}$$

where $L_y$ is the width of the transducer and $\lambda$ is the wavelength of acoustic wave. $Z_t$ is the natural focal point. Using an acoustic lens or by having a curved transducer surface also enables acoustic beam focusing [8]. However, to steer the beam, the transducer will have to be moved mechanically. This introduces imaging artifacts and the imaging quality will be highly dependent on the skill of the technician. This issue can be solved by using transducer arrays to steer the beam. A linear array can be used to perform beamforming in a 2D space. Three methods can be used for beam steering using an array: sequential linear array, mechanical sector scanner and phased linear arrays [48]. In the sequential linear scanning, a pulse-echo operation is performed with each element of the array one after the other. Each of this operation produces a B-mode line in the display. The field of view is restricted by the length of the array. In mechanical sector scanner, the transducers are rotated around an axis using an electric motor. Phased array scanners produce image by electronic steering of the beam. By appropriate delay applied to the elements in the array, beams can be focused at different depths and automatic steering can be also done. In comparison to

the sequential scanning, each element of the array is used to produce every B-mode lines in the image. Phased array approach has higher resolution and has higher data rates which improves image quality [48].

## 4.2 Beamforming architectures

The possibility to use electronic scanning similar to radar application was first demonstrated in [49]. A linear transducer array was used for beam steering by using an electronics circuitry to actuate each array element with a pre-defined delay. An imaging system prototype using phased array principle was demonstrated in [50] and [51]. Beam steering was performed both during transmit and receive operation to produce high resolution images. In Fig. 4.1 a transmit beamforming is illustrated. Low voltage control signals at the desired frequency is applied to delay elements whose delay can be precisely controlled. These delay elements then drive the HV drivers which produce the required HV pulses to actuate the transducers in the transmit mode.

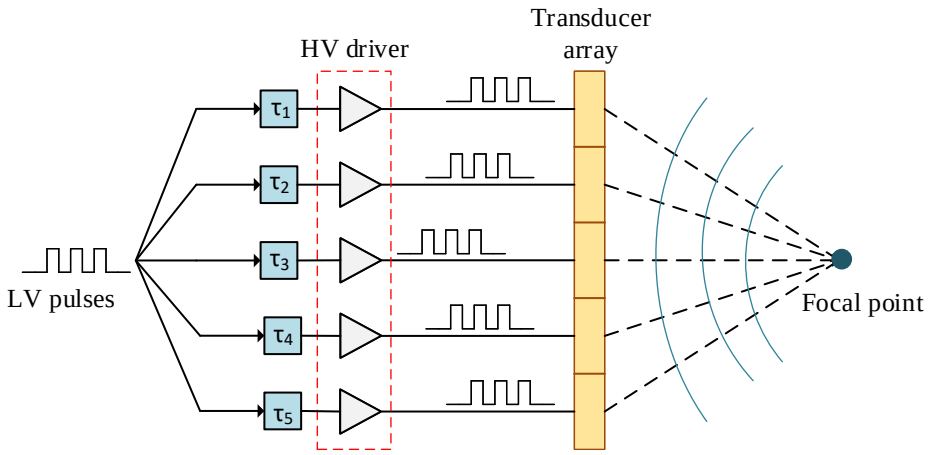



Fig. 4.1 Illustration of the transmit beamforming using a CMUT array.

Use of 2D ultrasound transducer arrays enable the development of volumetric 3D images [52]. This requires a large number of transducers on the imaging probe. CMUT technology enables the development of 2D arrays with large number of elements which leads to improved image resolution, contrast and signal to noise ratio [53]. To perform beamforming operation, each element in the fully populated arrays needs to be individually actuated and received from. In the conventional designs each element of the transducer requires one cable. This results in an imaging system with long coaxial cables running to the back-end where bulky electronics are used to interface those. In order to realize a portable ultrasound imaging system, the driving electronics that produce the precisely delayed HV pulses can

be moved close to the transducer. Integrating the beamforming circuity on-chip and using a monolithic or hybrid integration technique helps with cable count reduction [54] [27]. To generate accurate delayed driving signal, multiple approaches have been adopted. A simple digital beamforming architecture was presented in [55] and [56]. This approach is illustrated in Fig. 4.2. In this approach, the required delay values are loaded into the memory which is then input to a 10 bit comparator which would produce a high at the output when this delay value matches to a counter. This enables a one-shot circuitry which triggers the HV driver circuit. This is a very simple approach. However, to get a very high resolution for the delay values, a fast counter clocked at very high frequencies is required. Also, the output of the one-shot circuitry is not well controlled, so the HV output pulse width is not accurately set. A similar approach was also implemented in [53]. An all digital transmit beamforming was presented in [57]. Here, the resolution was limited to 25 ns and maximum time delay to 750 ns.

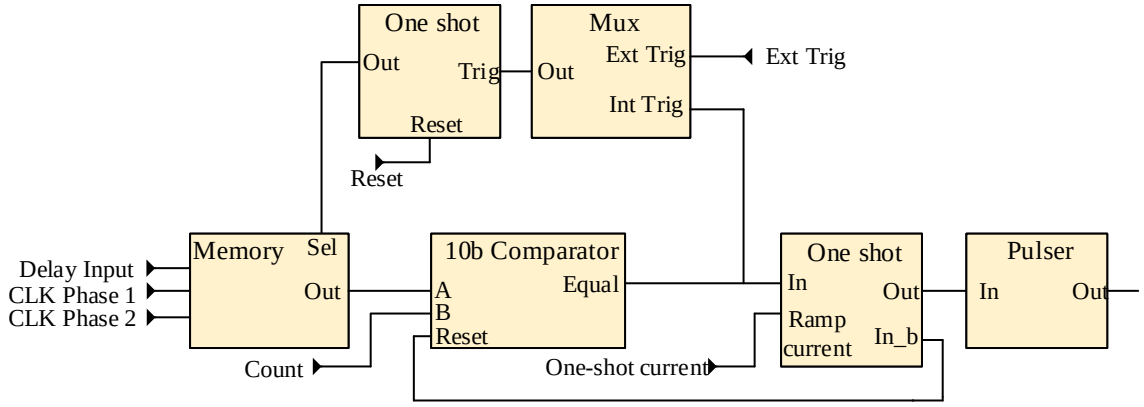



Fig. 4.2 Block diagram of the digital beamforming architecture presented in [55] [56].

To achieve high resolution and accurate time delay between the array elements, several techniques are presented in literature. In [58] and [59], an integrated phase locked loop was used on chip to generate precisely controlled clock phases with high resolution. This approach enables highly accurate clock phase generation. However, a PLL design is complicated and it is a second order system which makes it harder to stabilize. Also, the frequency of interest for diagnostic ultrasound application is generally a few MHz range. For this frequency range the phase noise of the PLL can be higher when compared to a delay locked loop (DLL). A transmit beamforming chip based on a DLL was presented in [60] and [61]. A main concern of the design in [60] is that the DLL used is not flexible to accept a wide input reference clock frequency. Also external receive circuits are used. In [61] only the transmit beamforming capability is provided. The HV pulsers and pre-amplifiers are external to the

chip. Further, the fine timer resolution is fixed which results in lack of flexibility in terms of delay generation. In this work, an 8 channel CMUT transceiver chip with a wide range analog DLL is presented. The chip can accept reference clock ranging from 10 MHz to 40 MHz. Further, approaches to reduce the static phase error of the DLL is also implemented to reduce the delay quantization error. Fig. 4.3 illustrates the proposed transmit beamformer circuit. The core of the circuit is a wide range analog DLL operating at 20 MHz. The DLL is designed to provide 10 clock phases each separated by 5 ns. A digital block selects these 10 phases based on the programmed fine delay values stored in the registers. A 10:1 MUX selects the DLL clocks for fine timer operation and a phase shifter is clocked with this selected clock. The fine timer block also includes a clock divider which divides the input clock by a 6-bit divider value. A pulse counter circuit takes the output of the clock divider and provides the programmed number of pulses to the phase shifter. This divided and counted clock is then shifted out to each of the HV driver. The coarse timer block consist of a global 10 bit counter and a comparator. The comparator of each fine timer block provides an enable (ENA) signal to the pulse counter once the count value reaches the stored coarse timer value. A trigger detector blocks waits for an external trigger signal. If the external trigger signal stays high for atleast 3 clock cycles, the trigger detector enables the coarse timer block. This is reset at the end of the counting and waits for the next trigger.

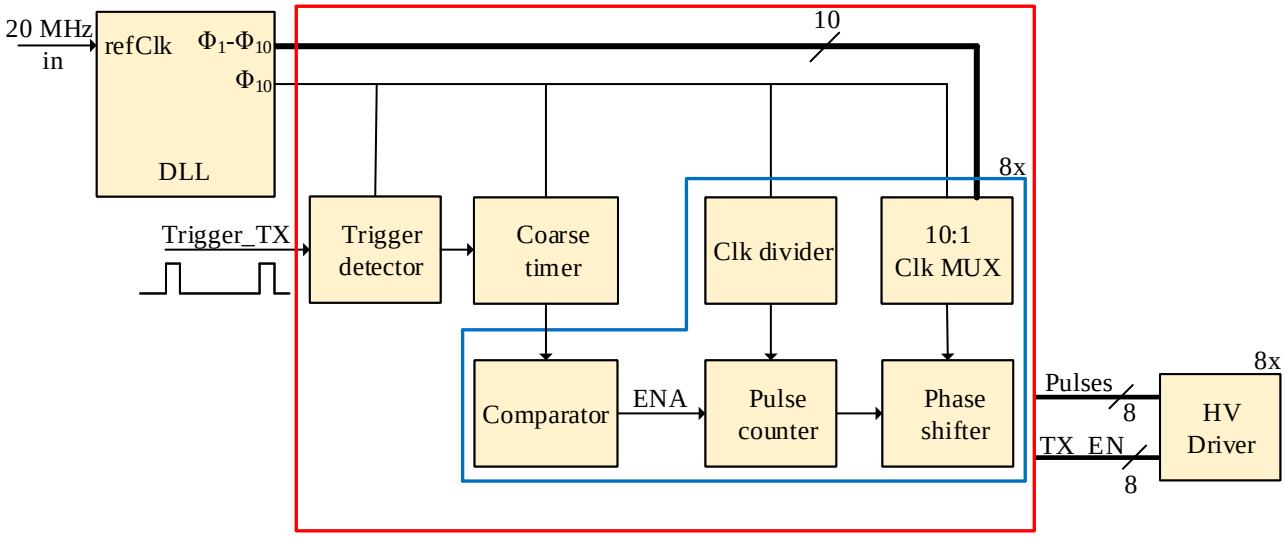



Fig. 4.3 Block diagram of the proposed DLL based transmit beamformer circuit.

## 4.3 Delay Locked Loop

Delay-locked loops (DLL's) are used widely in memory, microprocessors, IO interfaces of digital circuits for clock synchronization, minimize clock skew and clock and data recovery circuits (CDR) [62][63]. Certain applications require multi-phase clocks with precisely shifted phases. Simply delaying the clocks using a delay line could achieve this, however this is not robust to temperature, voltage or process variations. A precise control over this can be achieved by putting the delayed clock signal around a loop and locking the delayed output clock to a reference clock [64]. Since, the principle is similar to that of a phase-locked loop (PLL), the circuit is sometimes also referred to as the delay line PLL. The key design objectives of the DLL are wide locking range, fast locking time, low static phase error and low jitter. In [65] a DLL based CDR circuit is analyzed. DLLs offer higher jitter tolerance as compared to PLL in such circuits because the power supply and substrate noise induced phase errors do not accumulate over clock cycles [66]. DLLs also fare better in terms of loop stability as compared to PLLs. This is due to the fact that DLL is a first order system as opposed to a PLL where the VCO makes it a second order system. A multi-phase DLL based built in self test (BIST) circuit was presented in [67].

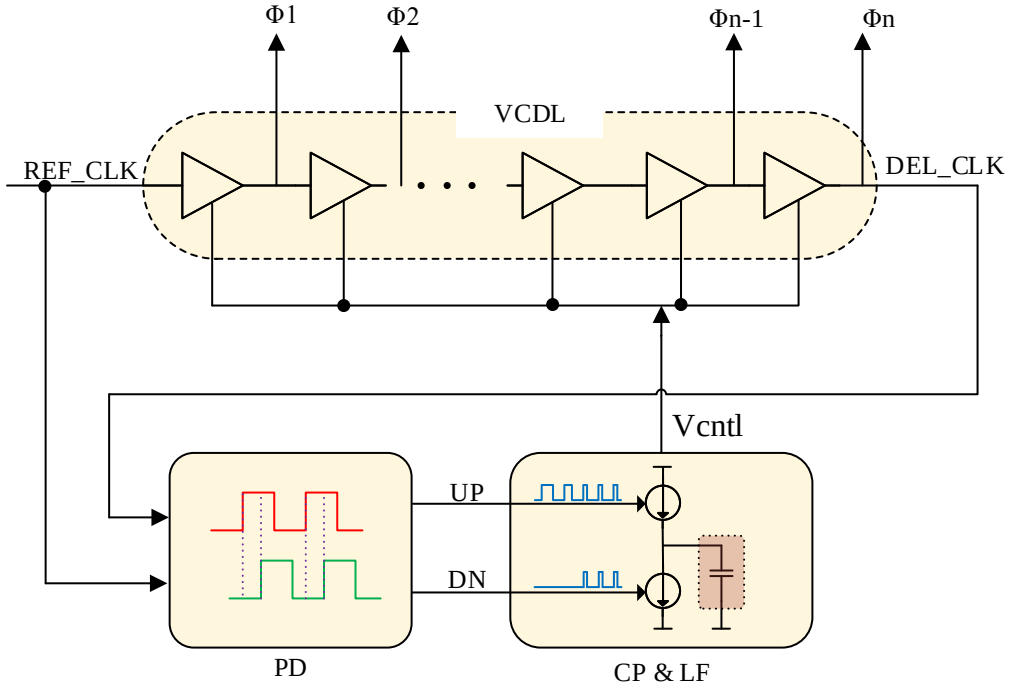



Fig. 4.4 Block diagram of a conventional delay locked loop.

A block diagram representation of a conventional analog DLL is shown in Fig. 4.4. The key building blocks of the DLL include: a voltage controlled delay line (VCDL), a phase detector (PD), a charge spump (CP) and loop filter (LF). The negative feedback loop adjusts

the delay of the VCDL by a control voltage which is proportional to the phase error. In the locked condition, the reference clock (REF_CLK) and the delayed clock (DCLK) have the same phase. As the only state variable of the DLL is the phase, a first order control loop is used to adjust the phase error. Hence the loop filter of the DLL consist of only a single capacitor. The reference clock is input to the VCDL. The phases of the delayed clock and the reference clock are then compared by the PD which produces UP and DN signals. These UP and DN signals are used to control a charge pump which pumps or removes charge from the loop filter capacitance. The output of the loop filter generates the control voltage ($V_{cntl}$) which is used to adjust the delay of the VCDL. Ideally, in the locked state, the VCDL delays the reference clock by exactly one clock cycle.

### 4.3.1 Frequency response

The closed loop frequency response of the DLL is analyzed in this section to understand the loop dynamics of the DLL. A continuous time approximation is used here. The sampling nature of the phase detector operation is ignored. This approximation is valid for loop bandwidths which are atleast a decade below the frequency of operation [62] [68]. This allows us to treat the output of the phase detector as the average value.

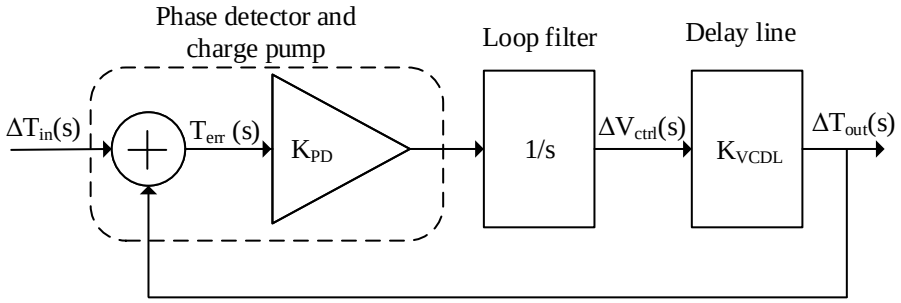



Fig. 4.5 S-domain linear model of the DLL.

In Fig. 4.5 a block diagram of the s-domain linear model of the DLL in terms of input and output delay is shown [69]. The state variable used is time which is more meaningful in the case of a DLL. In the ideal condition, in the locked state of the DLL, the output clock is delayed exactly by one clock period $T_{ref}$. The model describes the effect on the output clock delay when there is a small delay of $\Delta T$ in the input reference clock when the DLL is close to the locked state. The transfer function of the VCDL can be represented by the incremental change in the delay to an incremental change in the control voltage. This can be written as:

$$K_{VCDL} = \frac{\Delta T_{out}(s)}{\Delta V_{ctrl}(s)} \tag{4.2}$$

The phase detector followed by the charge pump generates an output current in response to the error in the time delay. This can be written as:

$$K_{PD} = \frac{I_{pd}(s)}{T_{err}(s)} = \frac{I_{ch}}{T_{ref}} \tag{4.3}$$

The loop filter consist of a capacitor whose integral control adjusts the VCDL delay until the phase error reaches zero. The loop filter can be modelled as:

$$\frac{\Delta V_{ctrl}(s)}{I_{pd}(s)} = \frac{1}{sC} \tag{4.4}$$

The closed loop gain of the DLL can be written as a first order transfer function given by:

$$H(s) = \frac{1}{1 + s.\tau} \tag{4.5}$$

Where the time constant $\tau$ can be written as:

$$\tau = \frac{1}{K_{PD} \cdot (1/C) \cdot K_{VCDL}} \tag{4.6}$$

$$\tau = \frac{T_{ref} \cdot C}{K_{VCDL} \cdot I_{ch}} \tag{4.7}$$

The time constant shows how fast the DLL can react to quick change in input clock frequencies. As stated earlier, for the continuous approximation operation of the phase detector $\tau \geq 10 \cdot T_{ref}$. The closed loop transfer function can be written as:

$$H(s) = \frac{1}{1 + \frac{s \cdot T_{ref} \cdot C}{K_{VCDL} \cdot I_{ch}}} \tag{4.8}$$

We can write the closed loop bandwidth (-3 dB frequency) as:

$$\omega_{3dB} = \frac{I_{ch} \cdot K_{VCDL}}{C \cdot T_{ref}} \tag{4.9}$$

$$f_{3dB} = \frac{I_{ch} \cdot K_{VCDL}}{2\pi C} \cdot f_{ref} \tag{4.10}$$

### 4.3.2 DLL operation

The locking operation of a conventional DLL is illustrated in Fig. 4.6. When the VCDL delay is initially smaller than the clock period, the control loop increases the delay of the VCDL until the DCLK is phase locked to the CLK. This is shown in 4.6 (a). The phase detector

compares the DCLK and CLK and produces a DN signal which discharges the loop capacitor through the charge pump. This results in reducing the control voltage which increases the delay of the VCDL. The case where the initial delay of the VCDL greater than the clock period is also shown in Fig. 4.6 (b).

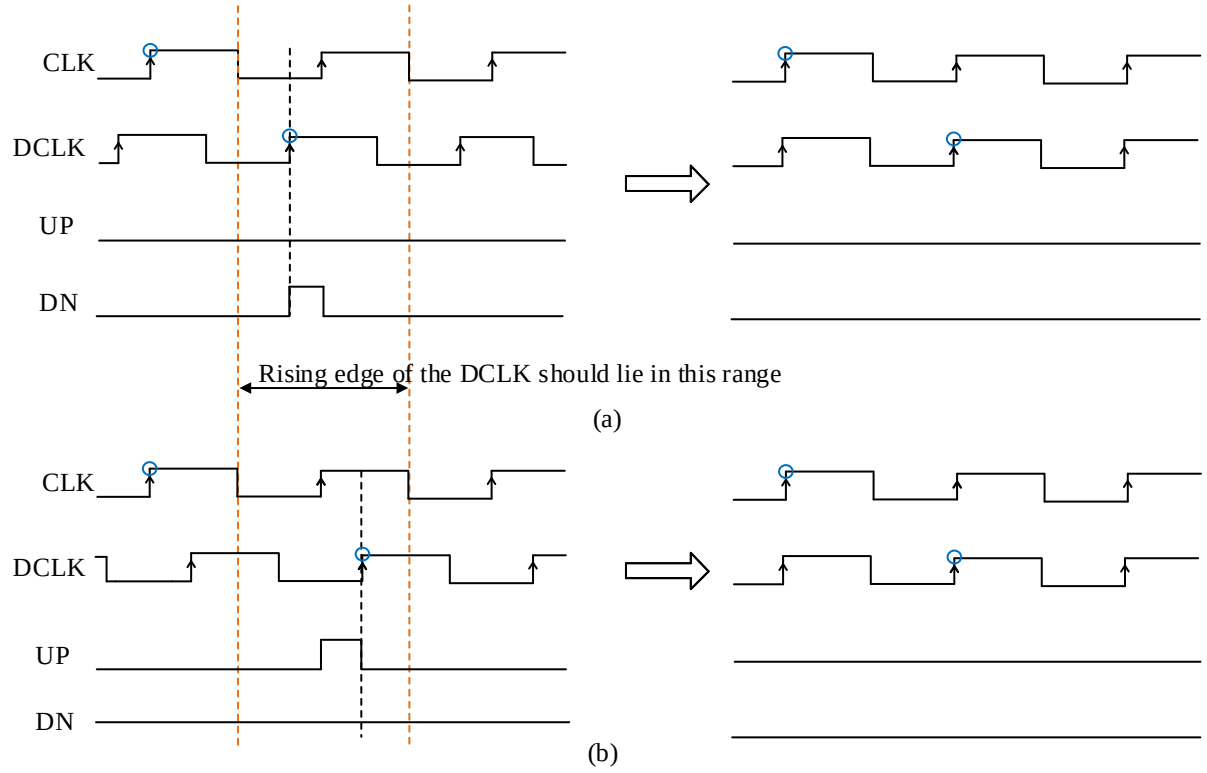



Fig. 4.6 Illustration of DLL locking operation and frequency locking range.

Conventional analog DLL can lock to only clock frequencies in a very narrow range. The initial delay of the VCDL needs to be within the range shown in Fig. 4.6 to ensure that the DLL does not go into a stuck at minimum delay or harmonic lock problem. The minimum and maximum delay of the VCDL must be within the below mentioned range to avoid either of this problem [67]:

$$0.5 \times T_{\mathrm{CLK}} < T_{\mathrm{VCDL,min}} < T_{\mathrm{CLK}} \tag{4.11}$$

$$T_{\mathrm{CLK}} < T_{\mathrm{VCDL,max}} < 1.5 \times T_{\mathrm{CLK}} \tag{4.12}$$

This can be expressed in terms of $T_{\mathrm{CLK}}$ as:

$$Max\left\{T_{\mathrm{VCDL,min}}, 2/3 \times T_{\mathrm{VCDL,max}}\right\} < T_{\mathrm{CLK}} < Min\left\{2 \times T_{\mathrm{VCDL,min}}, T_{\mathrm{VCDL,max}}\right\} \quad (4.13)$$

The inequality above manifests that there is only a very narrow range of frequencies for which the DLL will operate without entering into a harmonic locking or stuck at minimum delay problem. If $T_{\mathrm{VCDL,max}} \geq 3 \times T_{\mathrm{VCDL,min}}$, the inequality in (4.13) can not be satisfied for any value of $T_{\mathrm{CLK}}$ [70]. Further, with PVT variations, the VCDL delay can vary over a wide range which makes a reliable DLL design even cumbersome task. Dual-loop DLL architectures were developed to get rid of the harmonic lock and provide wide locking range [71],[72], [63]. It was possible to achieve a wide frequency locking range with these architectures as compared to the conventional. However, the chip area and power consumption was much higher. Further, the digital dual loop architecture reported in [71] is not suitable for our application as multi-phase clock output is desired. Digital DLLs can also achieve a wide operating range, however they have poor jitter performance due to the frequent phase selection and switching. Also, as mentioned before, they can not be used for applications where multi-phase clocks are needed. The works presented in [73] and [74] establishes an initial condition for the VCDL delay using an external reset signal. Although the work in [75] uses an efficient false lock detector circuit to prevent the DLL from going into harmonic lock and stuck problems, the reported jitter performance was not very promising. For our work, a fully analog replica delay line based approach as reported in [76] and [77] has been designed.

The block diagram of the designed wide range DLL is illustrated in Fig. 4.7. The bottom part shows the core DLL and the replica delay line (RDL) is placed on the top. The RDL generates a control voltage $V_{\mathrm{cr}}$ which is used to coarsely adjust the time delay of the VCDL in the core DLL. A fine control voltage $V_{\mathrm{cf}}$ generated from the loop filter fine tunes the VCDL. The RDL has the following circuit blocks: a delay cell (DC) with the same design as used in the main delay line, a current steering phase detector (CSPD) which compares the phase of the reference clock with the delayed signal, and a low-pass filter (LPF) at the output of the CSPD to generate the coarse control voltage. The $V_{\mathrm{cr}}$ is used to adjust the delay of the delay cell in the RDL as well.

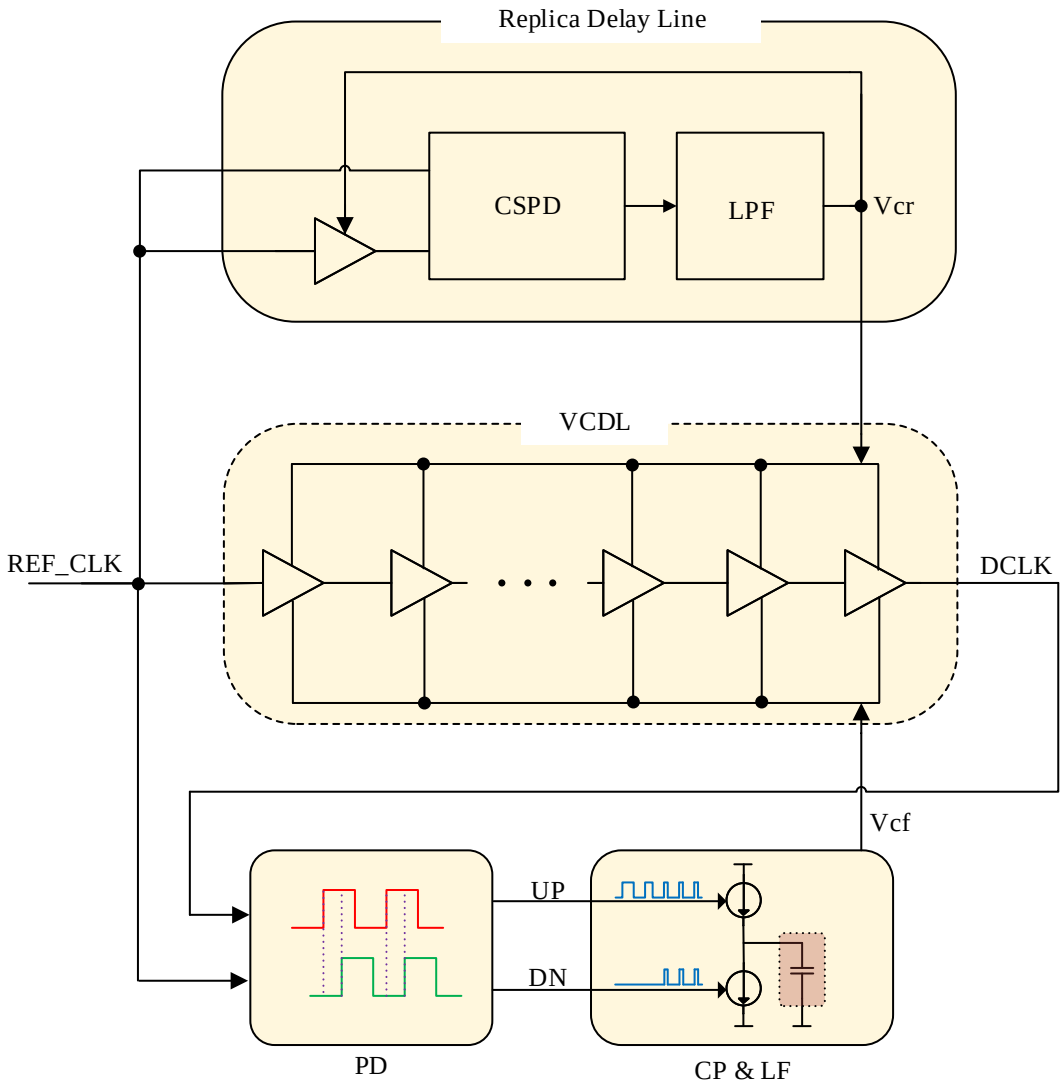



Fig. 4.7 A wide range DLL with a replica delay line (RDL).

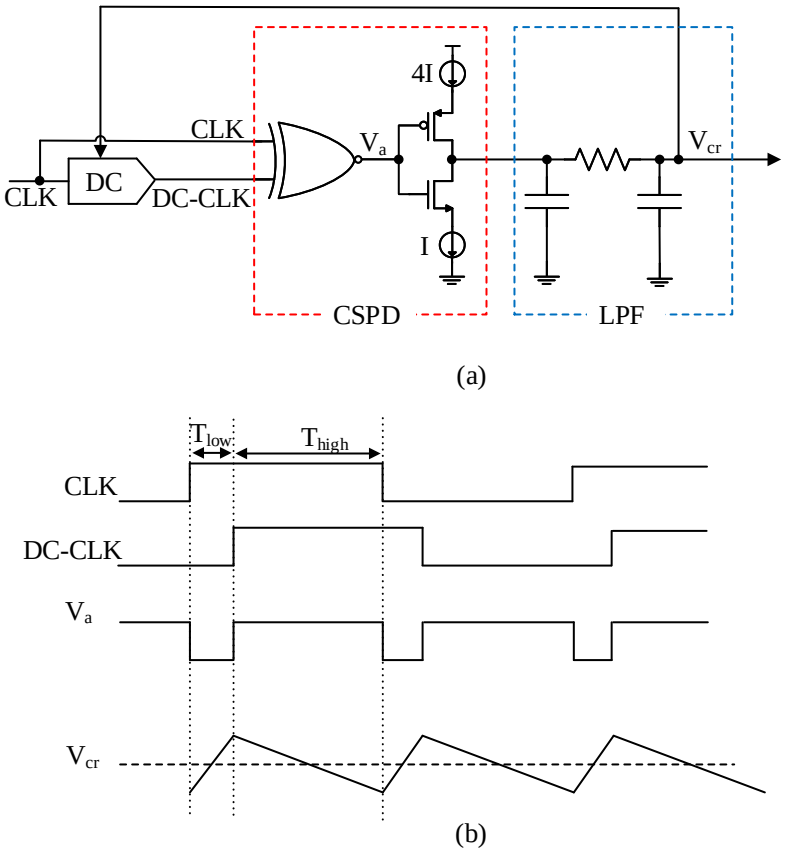



Fig. 4.8 Replica delay line with current steering phase detector (CSPD) and representation of waveforms showing operation.

The replica delay line and its operation is illustrated in Fig. 4.8. For the CSPD, the charging current to discharging current has a ratio of 4:1. The negative feedback in the RDL loop generates the coarse control voltage $V_{\text{cr}}$ such that it adjusts the DC to have a delay of $T_{\text{CLK}}/10$. With ten delay cells in the VCDL, we get a total delay close to $T_{\text{CLK}}$. The input to the CSPD are the *CLK* and a clock signal delayed by the DC ($DC-CLK$). Since this is a negative feedback loop, in the steady state, the charge added must be equal to the charge removed from the capacitor. If the charging and discharging currents were equal, this would be possible with an equal charging and discharging times. Since here we have four times more charging current than discharge current, we need 4 times discharge time than the charging time. The loop will adjust the DC until this state is achieved. This ensures a charging time of $\pi/5$ and discharging time of $4\pi/5$. The node $V_a$ will be adjusted according to the DC delay value to achieve this.

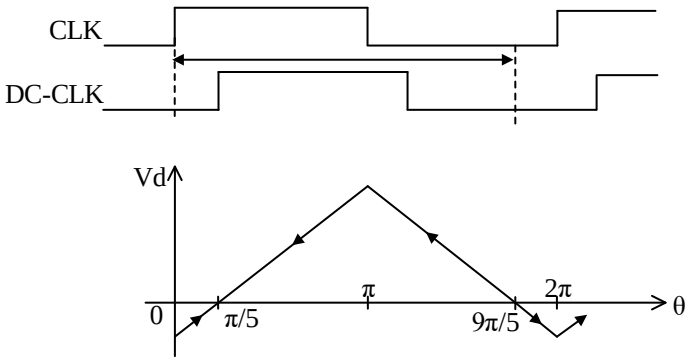



Fig. 4.9 Gain curve of the CSPD and locking range.

The frequency lock range of the replica delay line can be determined using the gain curve of the CSPD as described in [70] and [77]. The gain curve of the CSPD is shown in Fig. 4.9. Here, $V_{\mathrm{d}}$ represents the change in the steady state $V_{\mathrm{cr}}$ value. The x-axis represents the delay. The arrow in the gain curve shows the direction in which delay will change. If the delay of the DC in the RDL is less than $\pi/5$ ($T_{\mathrm{CLK}}/10$), the $V_{\mathrm{d}}$ will have a negative value and the delay is adjusted until the loop settles with a $T_{\mathrm{DC}}$ of $T_{\mathrm{CLK}}/10$. With a $T_{\mathrm{DC}}$ between $\pi/5$ and $9\pi/5$, a positive $V_{\mathrm{d}}$ will adjust the $T_{\mathrm{DC}}$ to lock at $\pi/5$. If the delay is greater than $9\pi/5$, the $V_{\mathrm{d}}$ becomes negative, i.e, $V_{\mathrm{cr}}$ will be reduced. This will increase the delay and the RDL will try to lock at $2\pi+\pi/5$ which is a harmonic lock condition. The following inequality can be used to express the maximum and minimum delay values needed to achieve locking:

$$0 < T_{\mathrm{DC,min}} < \frac{1}{10}T_{\mathrm{CLK}} \tag{4.14}$$

$$\frac{1}{10}T_{\mathrm{CLK}} < T_{\mathrm{DC,max}} < \frac{9}{10}T_{\mathrm{CLK}} \tag{4.15}$$

We can write these equations in terms of $T_{\mathrm{CLK}}$. From (4.14) we can write:

$$T_{\mathrm{CLK}} > 10T_{\mathrm{DC,min}} \tag{4.16}$$

From (4.15)

$$T_{\mathrm{CLK}} < 10T_{\mathrm{DC,max}} \tag{4.17}$$

$$T_{\mathrm{CLK}} > \frac{10}{9}T_{\mathrm{DC,max}} \tag{4.18}$$

Combining (4.16)-(4.18),

$$Max\{10T_{\mathrm{DC,min}}, \frac{10}{9}T_{\mathrm{DC,max}}\} < T_{\mathrm{CLK}} < 10T_{\mathrm{DC,max}} \tag{4.19}$$

If we make $T_{\mathrm{DC,max}} > 9 \cdot T_{\mathrm{DC.min}}$, (4.19) can be written as:

$$\frac{10}{9}T_{\mathrm{DC,max}} < T_{\mathrm{CLK}} < 10T_{\mathrm{DC,max}} \tag{4.20}$$

This gives us the best possible theoretical lock range for this DLL architecture at frequency lock range of 1:9.

### 4.3.3 Voltage controlled delay line design

The voltage controlled delay line (VCDL) consists of ten variable delay element (VDE). Each VDE is formed by four delay cells (DC). The total number of VDE connected in the VCDL chain sets the delay range of the delay line. The three different kind of delay cells are: shunt capacitor based delay cell [78], variable resistor delay cell [79] and current starved delay cell [80],[81]. In the shunt capacitor based delay cell, a MOSFET is used to control the amount of capacitance load connected to the output of a NOR gate. In the variable resistor based approach, a digitally controlled array of transistors are used as variable resistor to control the delay. For this work, a current starved delay cell is used as it is area efficient when compared with the other two approaches. Also, the implementation is much simpler.

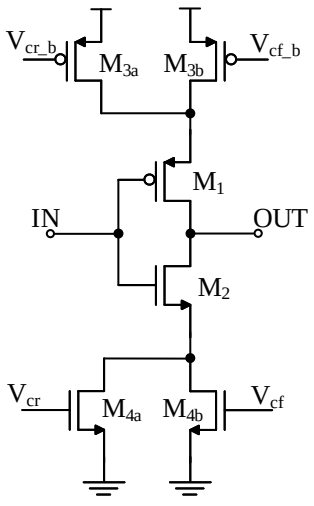
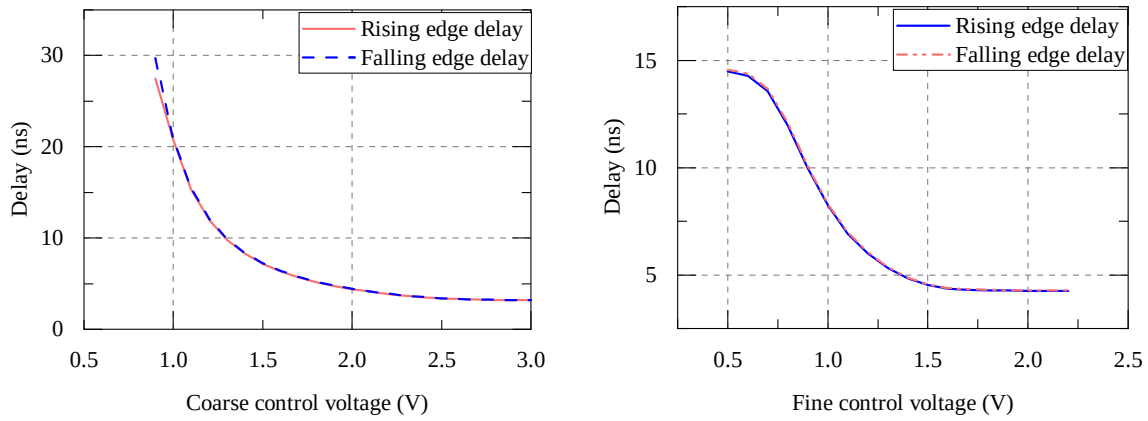



Fig. 4.10 Schematic diagram of a current starved delay cell with dual control.

The circuit shown in Fig. 4.10 is the implemented dual control delay cell. Transistors $M_1$ and $M_2$ form an inverter. The MOSFETs $M_{3a}$, $M_{3b}$, $M_{4a}$ and $M_{4b}$ act as current source

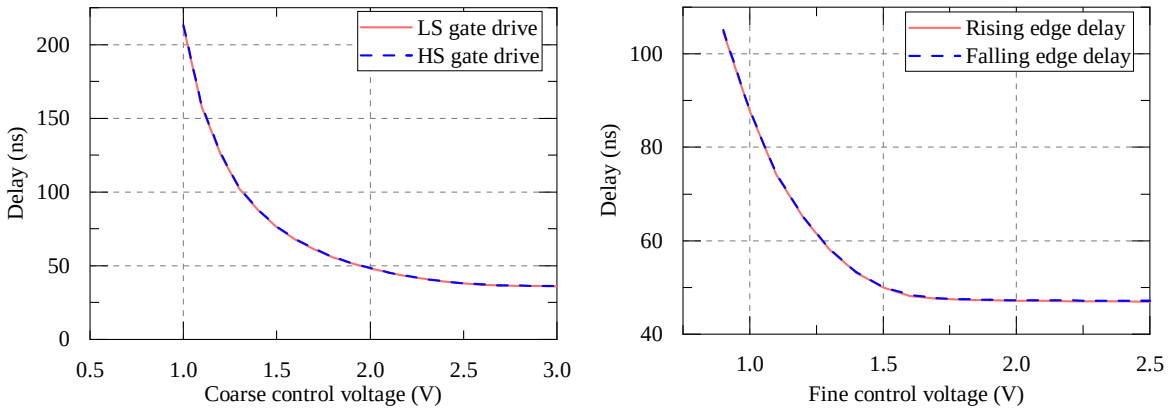
and sink devices. The coarse and fine control voltages are applied to the source and sink MOSFETs to control the current of the inverter. This allows to control the delay of the inverter by controlling the charging current of the capacitance at the output node OUT. As can be seen from the Fig. 4.10, the source and sink transistors are split in order to be able to control them with both the coarse and fine control signals. These control voltages will define the charging and discharging current of the inverter. $M_{3b}$ is made weaker than $M_{3a}$ to ensure that delay changes slowly with the application of the fine control voltage. The same is done with $M_{4b}$ and $M_{4a}$.




(a) (b)

Fig. 4.11 (a) Post-layout simulation result showing the delay variation against a sweep of coarse control voltage. The fine control voltage set at 800 mV; (b) delay variation against sweep of fine control voltage. Coarse control voltage set at 1.2 V.

In Fig. 4.11, the delay variation of the delay cell against the control voltage sweep is shown. Fig. 4.11a, the fine control voltage is set at 800 mV and the coarse control voltage is swept. It can be seen that the delay varies from roughly about 30 ns to 4 ns. The delay variation has a non-linear response. This is due to the fact that in the current starved inverter, we are adjusting the delay by controlling the currents in the MOSFET which has a non-linear relationship to the gate voltage. Beyond 2 V, the delay remains nearly constant. In Fig. 4.11b, the coarse control is fixed at 1.2 V and the fine control voltage is varied. The delay varies only in a small range as desired.




(a) (b)

Fig. 4.12 (a) Post-layout simulation result showing the delay variation of the complete delay line against a sweep of coarse control voltage. The fine control voltage set at 800 mV; (b) delay variation of delay line against sweep of fine control voltage. Coarse control voltage set at 1.2 V.

Fig. 4.12 shows the delay variation of the complete VCDL in terms of the coarse and fine control voltage variations. It can be observed that the VCDL follows a similar trend and shows a non-linear variation in the delay. In Fig. 4.13, a post-layout transient simulation result of the VCDL is shown. A 20 MHz clock is used as the input. It can be observed that each subsequent output tap has a delay of 5 ns for a control voltage setting of 2 V coarse control and 800 mV fine control.

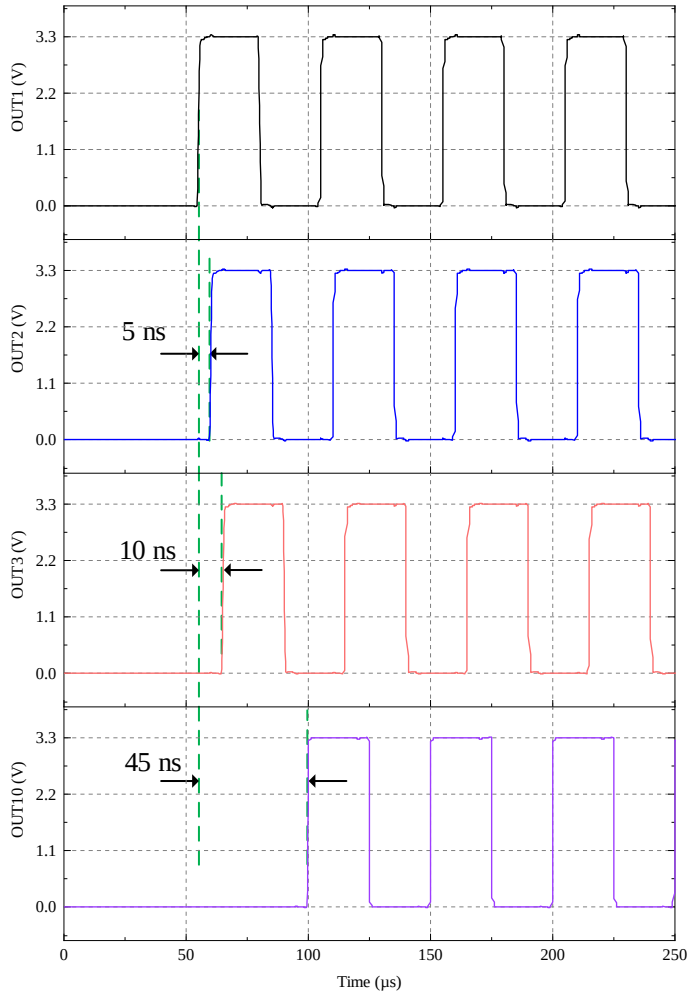



Fig. 4.13 Transient simulation of the delay line with a 20 MHz clock input. The coarse control voltage is set at 2 V and fine control voltage at 800 mV

### 4.3.4 Dynamic phase detector

A phase detector (PD) is a crucial block of the DLL. The PD measures the phase difference between two input clock signals and produces an output which is proportional to the phase error. For an analog DLL, the two inputs of the PD are the reference clock (REF_CLK) and the output from the last tap of the VCDL (DCLK). Fig. 4.14 illustrates two widely used PD circuits. In 4.14(a), an XOR based PD is shown. For this PD, the output duty cycle is directly proportional to the phase difference between input signals [69]. A main drawback of this kind of PD is that it can not really detect which of the clocks is leading or lagging. The average value of the output repeats after a phase difference of 180°. Additionally, the XOR PD produces only one output which is not suitable for a charge pump based circuit where we need two signals (UP and DN).

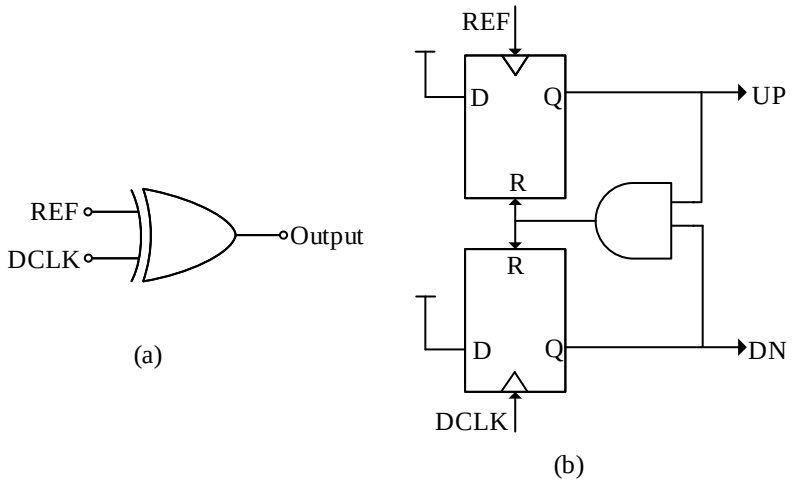



Fig. 4.14 (a) An XOR phase detector, (b) a phase-frequency detector.

A sequential circuit using flip-flops is shown in Fig. 4.14(b). This circuit is called the phase-frequency detector (PFD). This circuit generates the UP and DN outputs which are required to drive the charge pump. Also, since the circuit's output depends also on the past history, the PFD can detect the polarity of the phase difference between the two input clocks ( i.e, it can detect which input is leading or lagging). Another advantage of the PFD over the XOR PD is that, the PFD is not dependent on the duty cycle of the input clocks as the flip-flops are edge sensitive. A main disadvantage of the PFD circuit is that the speed of operation is limited due to the reset time [67].

In Fig. 4.15, a dynamic PD circuit is shown. These circuits are widely used in high speed PLL and DLL designs [82]. The required UP and DN signals are generated by the same circuit structure except that the inputs are switched. As opposed to the PFD circuit, the dynamic PD uses no flip-flops and has a simpler structure.The PD has fast operation due to the use of dynamic logic circuit.

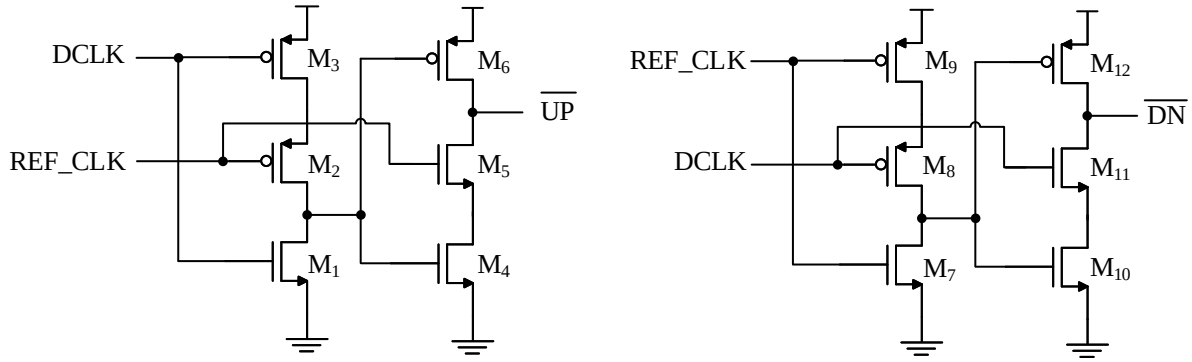



Fig. 4.15 Schematic diagram of the dynamic phase detector circuit to generate the UP and DN control signals for the charge pump.

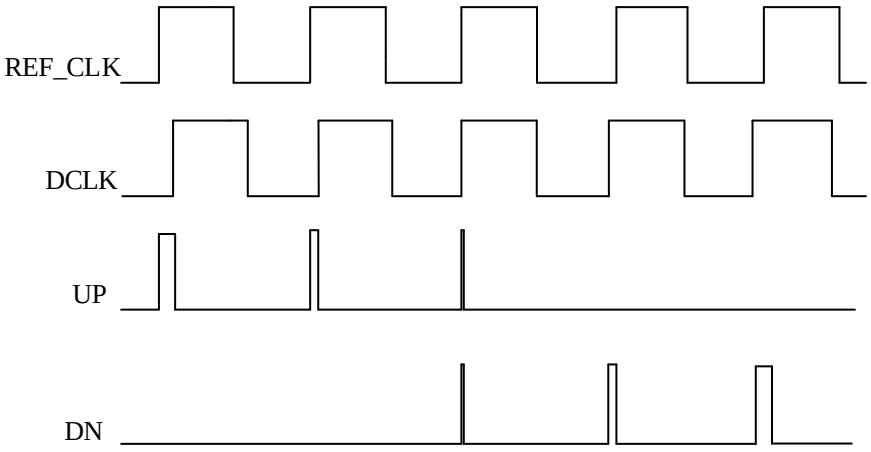



Fig. 4.16 Waveforms showing the operation of the PD.

To explain the working of the dynamic phase detector, let us initially assume that both DCLK and REF_CLK are at logic 0. This turns off $M_1$; $M_2$ and $M_3$ are turned on which pulls the drain of $M_1$ to logic 1. Now $M_4$ is on, $M_6$ and $M_5$ are off. If we make sure $M_6$ is stronger than $M_5$, the node $\overline{UP}$ is pulled to logic 1 and UP to logic 0. Now when REF_CLK goes to 1, $M_5$ turns on. $M_6$ remains off since the drain of $M_1$ retains its precharged logic 1 value. This pulls down $\overline{UP}$ to logic 0 and UP to logic 1. Now when DCLK goes high, $M_1$ is turned on to pull the precharged gate to logic 0. This turns off $M_4$ and turns on $M_6$ driving UP to logic 0. The same analysis can be performed on the circuit on the right to understand the generation of the DN signal.

A post-layout transient simulation result of the dynamic PD working in the closed loop DLL is shown in Fig. 4.17. It can be seen that when the DCLK lags the REF_CLK, the UP

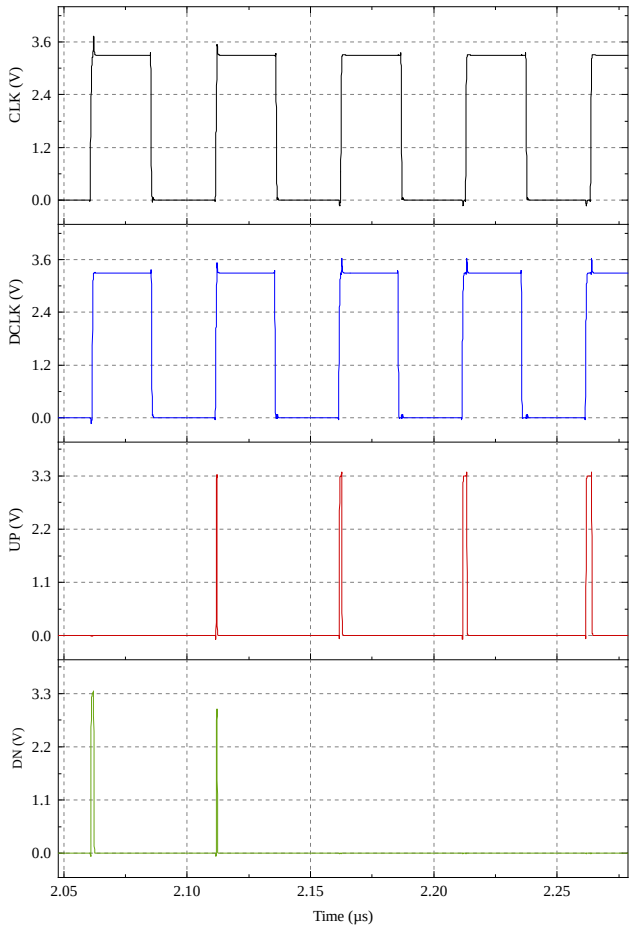



Fig. 4.17 Simulation result showing the operation of the dynamic phase detector.

signal is high and vice-versa. When both the clock signals are nearly aligned close to locked state, both the UP and DN signals are high simultaneously for a very brief moment. This is important to eliminate the dead-zone in the locked state.

### 4.3.5 Charge pump

The phase detector compares the CLK_REF and DCLK and produces the corresponding UP and DN signals depending on the phase error and polarity information. These UP and DN signals are used to generate the control voltage by charging and discharging the loop filter capacitor. The charge pump architectures are broadly classified as three: drain-switched, source-switched and gate-switched charge pumps [83]. Each of these circuit topologies is illustrated in Fig. 4.18.

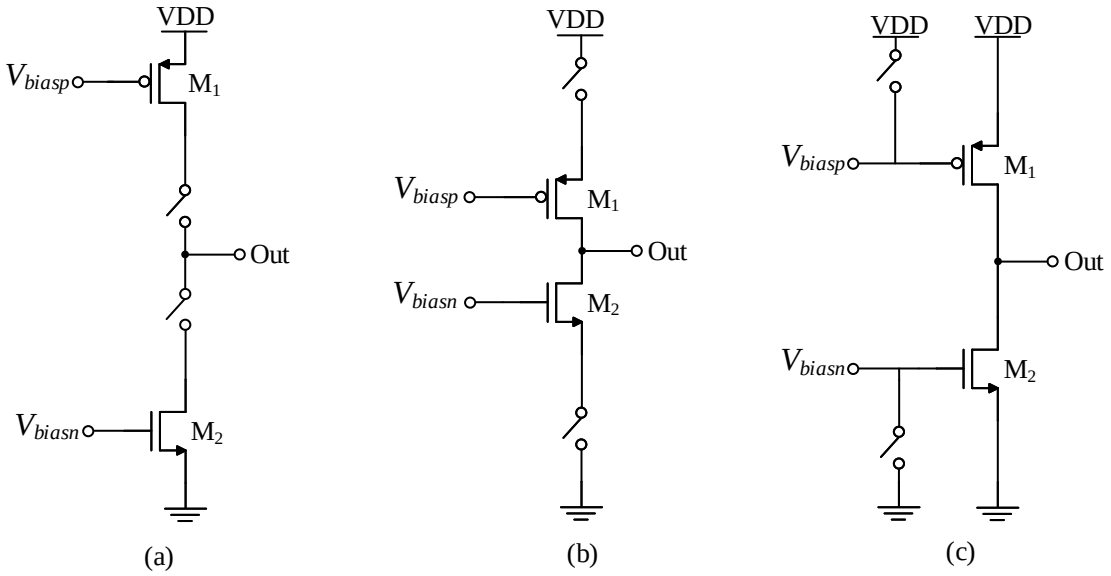



Fig. 4.18 (a) Drain-switched charge pump, (b) source-switched charge pump, (c) gate-switched charge pump.

In the charge pump architectures shown, transistors $M_1$ and $M_2$ are current source and sink respectively. In the drain-switched charge pump, the switches are connected at the drains of the current source transistors. Switching these with the UP and DN pulses from the PD allows to charge and discharge the loop filter capacitor. Two main issues with the drain-switched topology are charge injection and clock feedthrough to the output node. This affects the jitter performance of the DLL. This topology has the advantage of fast switching as the DC bias conditions of the current source transistors are not affected and they are never turned off. They always operate in linear region when the switches are turned off.

In the source-switched charge pump, the switches are connected to the source of the current source transistors. The clock feed-through and charge injection problem is thus eliminated. The gate-switched topology in Fig. 4.18(c) also eliminates this issue. In this case the switches are used to turn on and off the gates of the current sources $M_1$ and $M_2$. This significantly affects the transient behavior since the current source will be completely turned

off and the DC conditions need to be restored to operate them in saturation again. Hence a source-switched charge pump architecture is used for the circuit design.

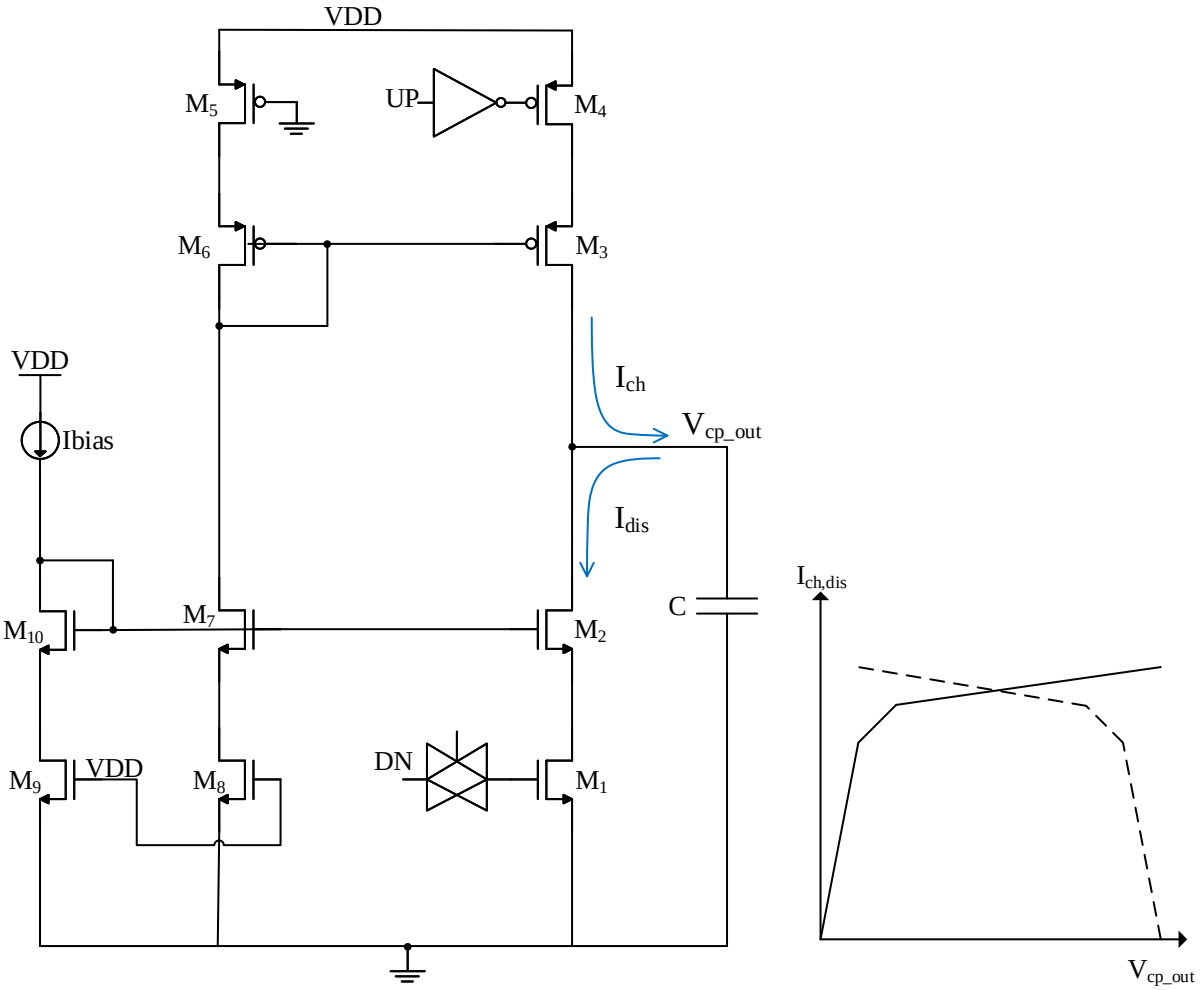



Fig. 4.19 A conventional source-switched charge pump and its charge and discharge operation.

Assuming ideal behavior for the PD and the charge pump, the DLL can achieve zero static phase error in the locked state. However, the non idealities in the charge pump design introduces phase error and time jitter which has to be considered during the circuit design [84], [85]. One main issue in the design of the charge pump is the current mismatch between the charging and discharging phase. A conventional source-switched charge pump circuit implementation and its current behavior is shown in Fig. 4.19. As the control voltage at the output of the loop filter changes, drain-source voltages of the NMOS and PMOS $M_2$ and $M_3$ changes. This affects the current matching between the current mirrors $M_6$/$M_3$ and

$M_7/M_2$. This current mismatch in the charge pump introduces a phase error in the DLL which is given by [86]:

$$\phi_{error} = 2\pi \frac{\Delta t_{on}}{T_{ref}} \frac{\Delta i}{I_{cp}} \tag{4.21}$$

where $\phi_{error}$, $\Delta t_{on}$, $T_{ref}$, $\Delta i$ and $I_{cp}$ are the phase error, on time (pulse width of the UP and DN pulses), period of the reference clock, the current mismatch and the charge pump current respectively. It can be seen from (4.21) that the phase error can be minimized by reducing the $\Delta t_{on}$ and $\Delta i$. The $\Delta t_{on}$ can not be completely eliminated as it is important to eliminate the dead-zone. So it is imperative to reduce the current mismatch in the charge pump. Several approaches are presented in literature to improve the current matching. In [87] a PFD and charge pump chopping approach was presented, [85] presented an auto-zeroing technique to reduce the static offset, [88] reported a highly matched VCDL to improve the phase offset. Using an opamp in the feedback loop also improves the current matching which can be looked as an area and power efficient approach. Similar approaches were also reported in [89] and [90]. With a high loop gain, the error amplifier ensures that the drain of $M_7/M_6$ precisely follows the node voltage at the output $V_{\text{cp\_out}}$. This helps to keep the drain-source voltages of the respective current mirrors to be equal and hence the charging current and discharging currents are kept equal. The implemented circuit topology is shown in Fig. 4.20.

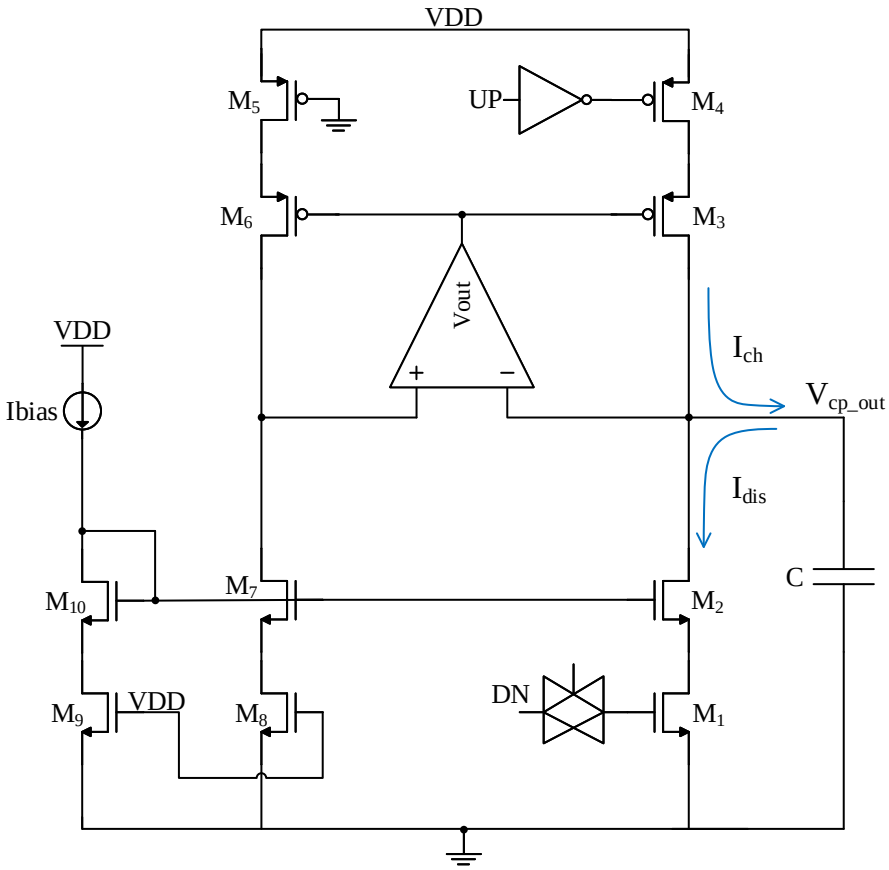



Fig. 4.20 Designed charge pump and loop filter.

The charge pump output node voltage varies over a wide range during the DLL operation. Thus, it requires that the opamp should have a wide input common mode voltage range. A rail to rail input OTA is required for this application. To estimate the specifications for the rail to rail OTA and the loop, simulations have been carried out using a voltage controlled voltage source (VCVS) as an ideal amplifier model. The estimated specifications are listed in the table 4.1.

Table 4.1 Design specifications for the rail to rail amplifier and the charge pump loop

| Parameter | Value |
|---|---|
| ICMR | 900 mV to 3 V |
| DC gain | $\geq$ 40 dB |
| Loop bandwidth | $\leq$ 2.1 MHz |

### Design of rail to rail input OTA

The input common mode voltage range (ICMR) of a differential input amplifier depends on the type of input transistor used. When using NMOS transistors as the input pair, the ICMR is calculated to be closer to the positive supply rail. The ICMR minimum value will be usually much higher than the negative supply rail. When the ICMR range is closer to the negative supply level, PMOS input pair is used. For applications which needs a wide input range, we need a rail to rail input amplifier. A simple approach to achieve this is by using a CMOS complementary input stage [91], [92]. This is shown in Fig. 4.21. A high performance rail to rail input technique using on chip charge pump was reported in [93]. However such an approach is not required in this case.

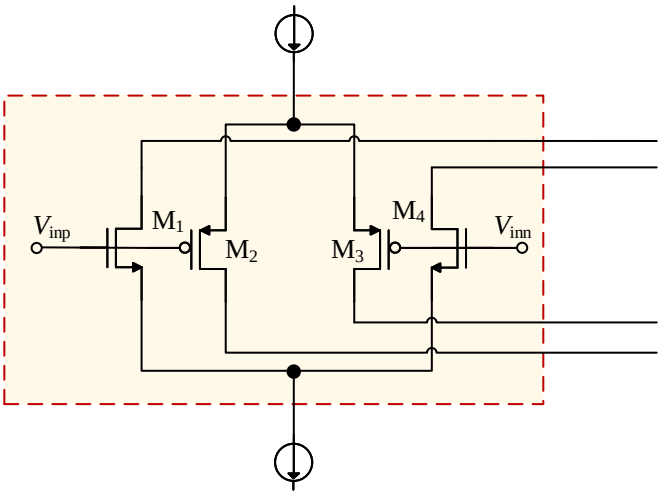



Fig. 4.21 Complementary input stage for rail to rail input operation.

Using a complementary input state, the total transconductance of the the input pair can be written as $g_{mtot}$. This can be written as:

$$g_{mtot} = g_{mN} + g_{mP} \tag{4.22}$$

During the low input voltages, the PMOS transistors will act and during the higher input voltages, the NMOS differential pair will dominate. There is a intermediate voltage range where both the NMOS and PMOS transistors will be on. In this range, the total transconductance will be the sum of both the NMOS and PMOS transconductances. This is graphically represented in the Fig. 4.22. It can be seen that the total transconductance varies nealy by factor of two over the ICMR. It is desirable for good distortion performance and proper frequency compensation that the overall transconductance of the diff-amp remains constant throughout the ICMR [40]. Another drawback of the complementary input stage is that the input offset voltage changes between that of the NMOS and PMOS. Changing the

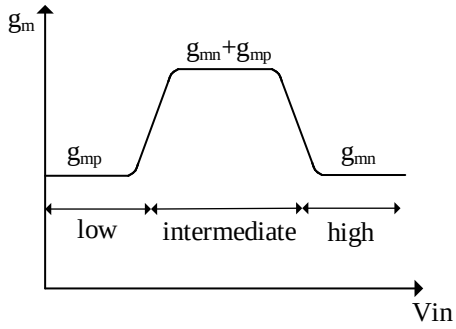



Fig. 4.22 Transconductance $g_{\mathrm{mtot}}$ of the complementary input stage versus the common-mode input voltage.

bias conditions result in an offset that is a function of the input common mode voltage. In the weak-inversion region of MOSFETs, the drain current $I_{\mathrm{D}}$ can be written as:

$$I_{\mathrm{D}} = I_{\mathrm{D0}} \cdot e^{(V_{\mathrm{GS}} - V_{\mathrm{TH}})/nV_{\mathrm{T}}} \tag{4.23}$$

From this the $g_{\mathrm{m}}$ can be written as:

$$g_{\mathrm{m}} = \frac{I_{\mathrm{D}}}{nV_{\mathrm{T}}} \tag{4.24}$$

For constant $g_{\mathrm{m}}$ in the complementary input pair, we need to make

$$g_{\mathrm{mn}} + g_{\mathrm{mp}} = constant \tag{4.25}$$

Since, in the weak inversion region of operation, the $g_{\mathrm{m}}$ is proportional to the drain current $I_{\mathrm{D}}$, we can achieve overall transconductance constant if we keep the sum of the currents constant.

$$I_{\mathrm{n}} + I_{\mathrm{p}} = constant \tag{4.26}$$

If we keep $I_{\mathrm{n}} = I_{\mathrm{p}} = I_0$, the total current when both the pairs are on is given by $I_{\mathrm{n}} + I_{\mathrm{p}} = 2I_0$. So all we need to do is to add an extra $I_0$ to each NMOS and PMOS input pairs when the other pair is off. The designed rail to rail input OTA with constant $g_{\mathrm{m}}$ is illustrated in Fig. 4.23. A folded cascode summing stage is used. The input pair transistors $\mathrm{M_1}$-$\mathrm{M_4}$ are biased in weak-inversion with a bias current of 1 $\mu$A. $\mathrm{MP_1}$ and $\mathrm{MN_2}$ source constant current $I_0$ when both the N and P diff pairs are on. $\mathrm{MS_1}$ and $\mathrm{MS_2}$ are like P channel switches that cut off the DC bias current path. $\mathrm{MS_3}$ and $\mathrm{MS_4}$ have the same function. The N- and P-channel current differential amplifiers which helps to drive the extra $I_0$ when only one of the complementary input pairs are on.

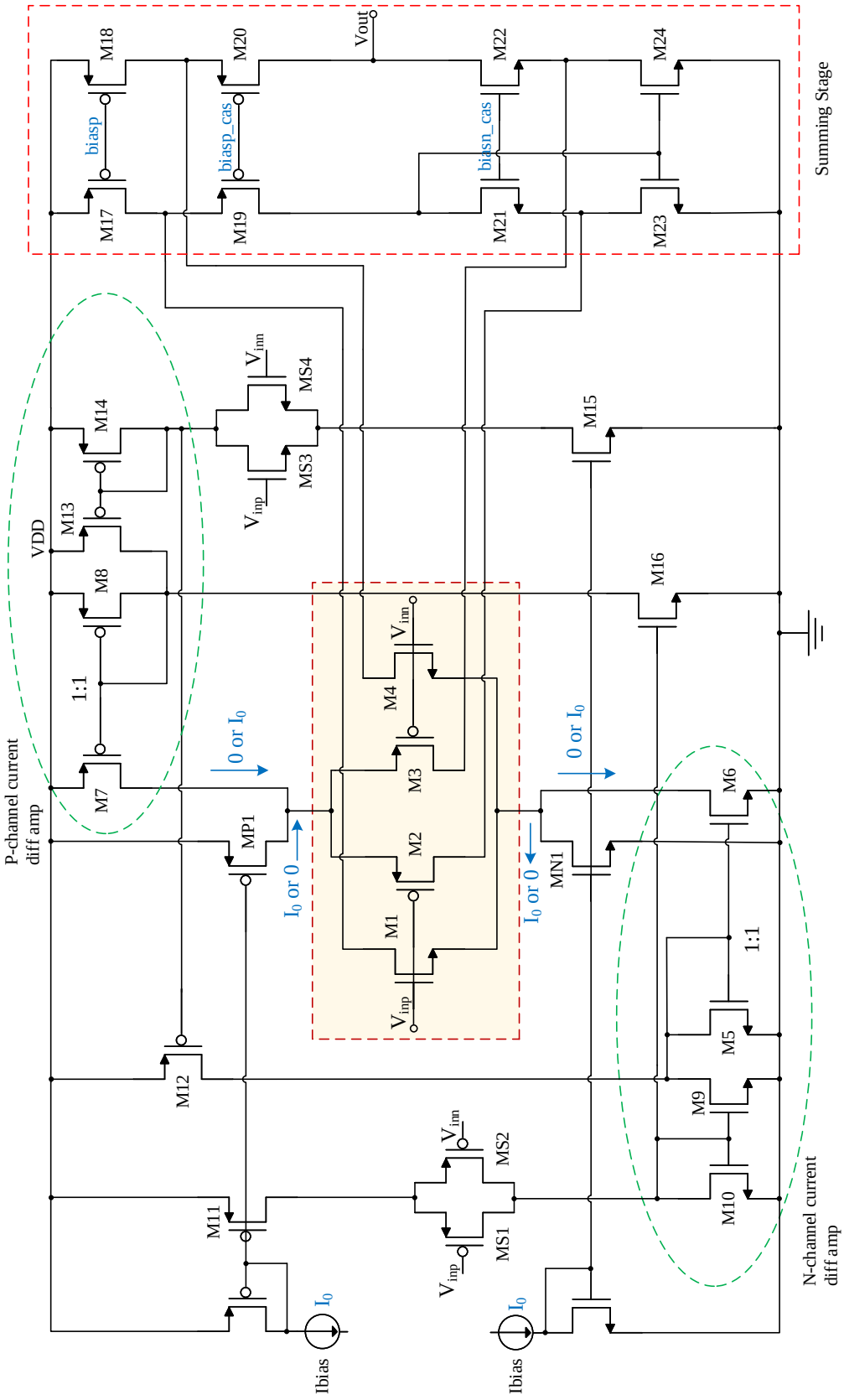



Fig. 4.23 Schematic diagram of the complete rail to rail input OTA.

Post-layout simulations are done to verify the performance of the rail to rail input OTA. The frequency response of the amplifier is shown in Fig. 4.24. It is noted that the amplifier exhibit a dc gain of 56.4 dB and a gain bandwidth (GBW) of 2.59 MHz. The phase margin is estimated to be 85.9 °.

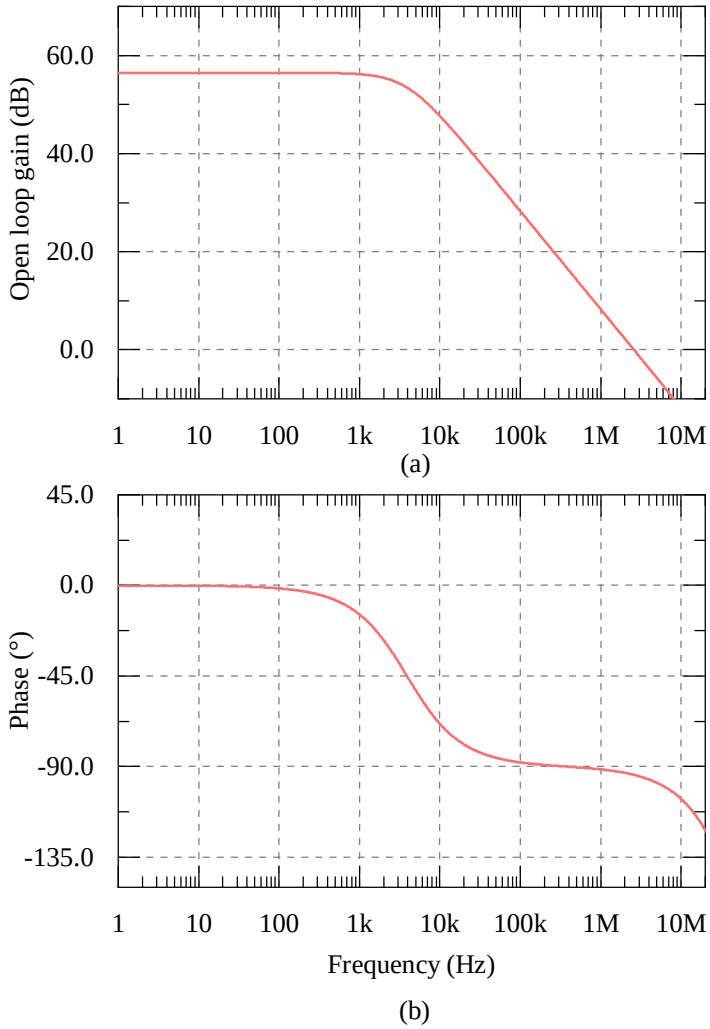



Fig. 4.24 Post-layout simulation showing the frequency response of the rail to rail input OTA.

The amplifier performance is verified across process, temperature and common mode range voltage corners as well and the worst corners are identified. This is shown in Fig. 4.25. It can be seen that across all the corners, the gain is always higher than the desired minimum value of 40 dB and the amplifier phase margin is always above 80 °. The GBW varies between 2 MHz and 3.56 MHz. The bandwidth variation is due to the slight variation of the $g_{mtot}$, which in our case is acceptable. The variation of the $g_{mtot}$ ($g_{mn}$+$g_{mp}$) against the input common mode voltage variation is illustrated in Fig. 4.26. It can be observed that the

$g_{mtot}$ is not a flat line as it would be in an ideal case. The maximum variation of the $g_{mtot}$ is calculated to be 6%.

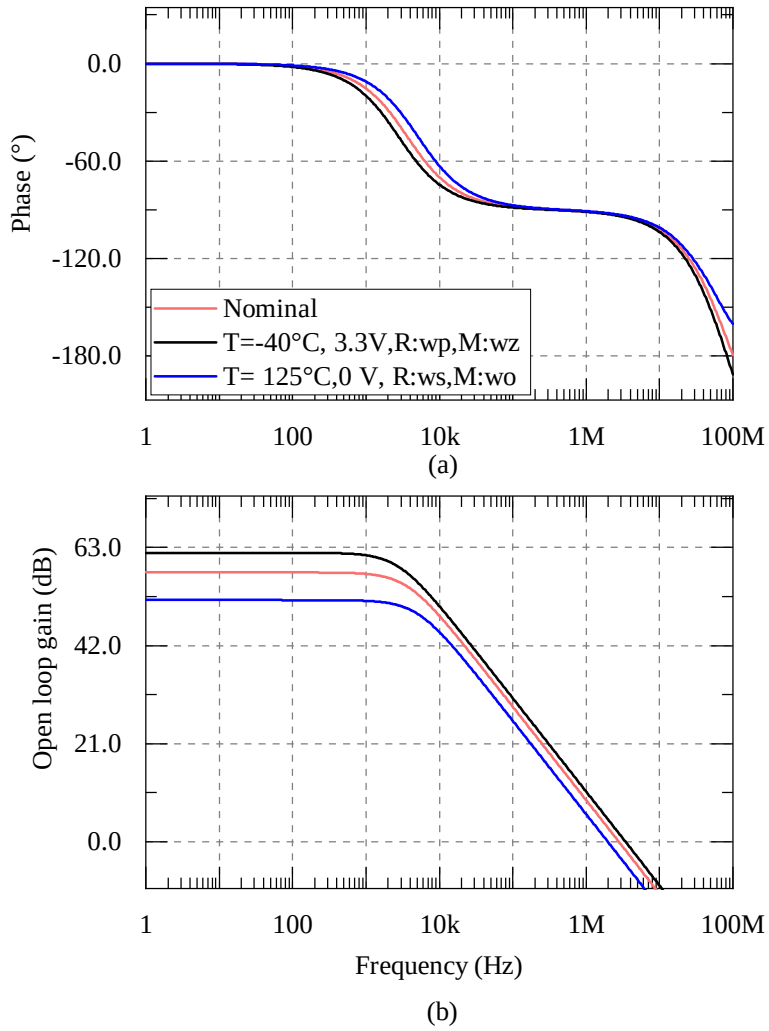



Fig. 4.25 Frequency response of the rail to rail amplifier showing the results at the nominal corner and the worst identified corner.

To estimate the variation of the dc open loop gain with the change in input common mode voltage, a parametric analysis has been done. The result is shown in Fig. 4.27. It can be seen that across the common mode voltage variation, the dc gain changes from 53 dB to 58.5 dB. It is observed that the gain variation is mainly happening due to the variation in the output impedance of the OTA. This is due to the fact that the simulation is done in open-loop where the common mode voltage of the output is set by the diode-connected MOSFET (see Fig. 4.23). It is expected that we won't see such variation, when the OTA is used in the real feedback loop in the charge pump.

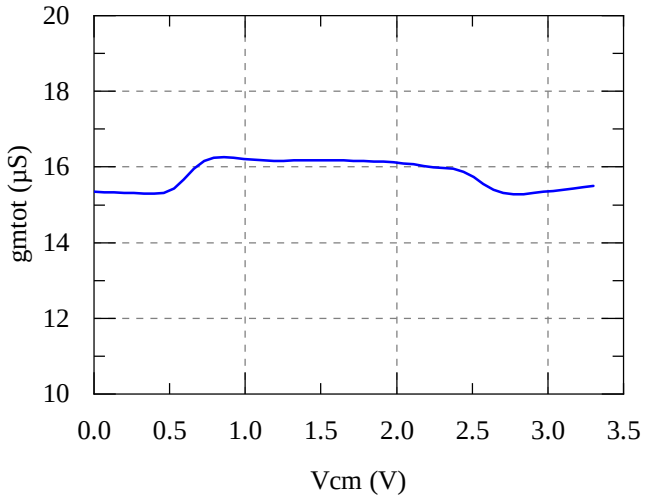



Fig. 4.26 Post-layout simulation showing the variation of $g_{\text{mtot}}$ versus the input common mode voltage.

To verify the performance of the charge pump, a dc sweep is done where the output dc voltage of the loop filter is varied from 0 to 3.3 V and the charging and discharging current are plotted. The result is shown in Fig. 4.29. It can be observed that there is a perfect matching of the charge pump currents. The circuit layout occupies an area of 275 µm$\times$210 µm and is shown in Fig. 4.28.

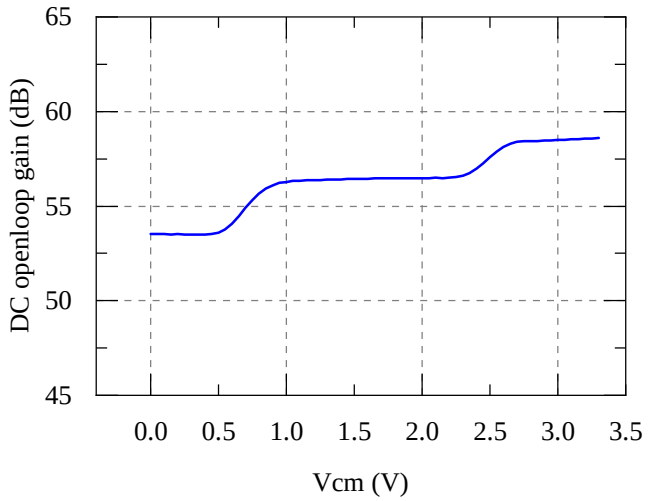



Fig. 4.27 Post-layout simulation showing the variation of DC open-loop gain versus the input common mode voltage.

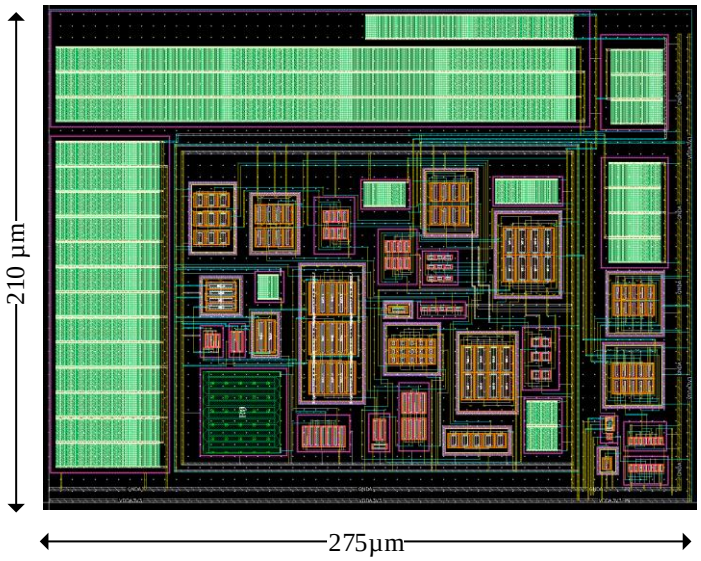



Fig. 4.28 Layout of the charge pump and loop filter with rail to rail OTA and biasing circuits.

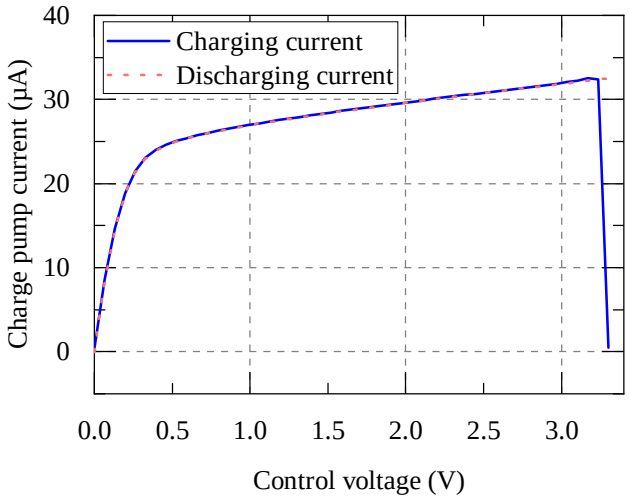



Fig. 4.29 Post-layout dc simulation showing the variation of the charging and discharging currents of the charge pump versus the control voltage variation at the loop filter output.

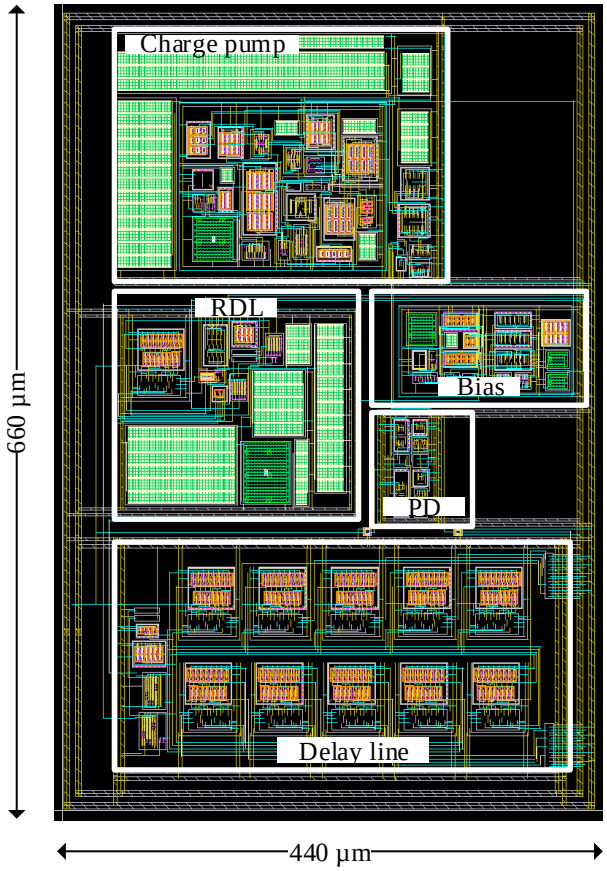
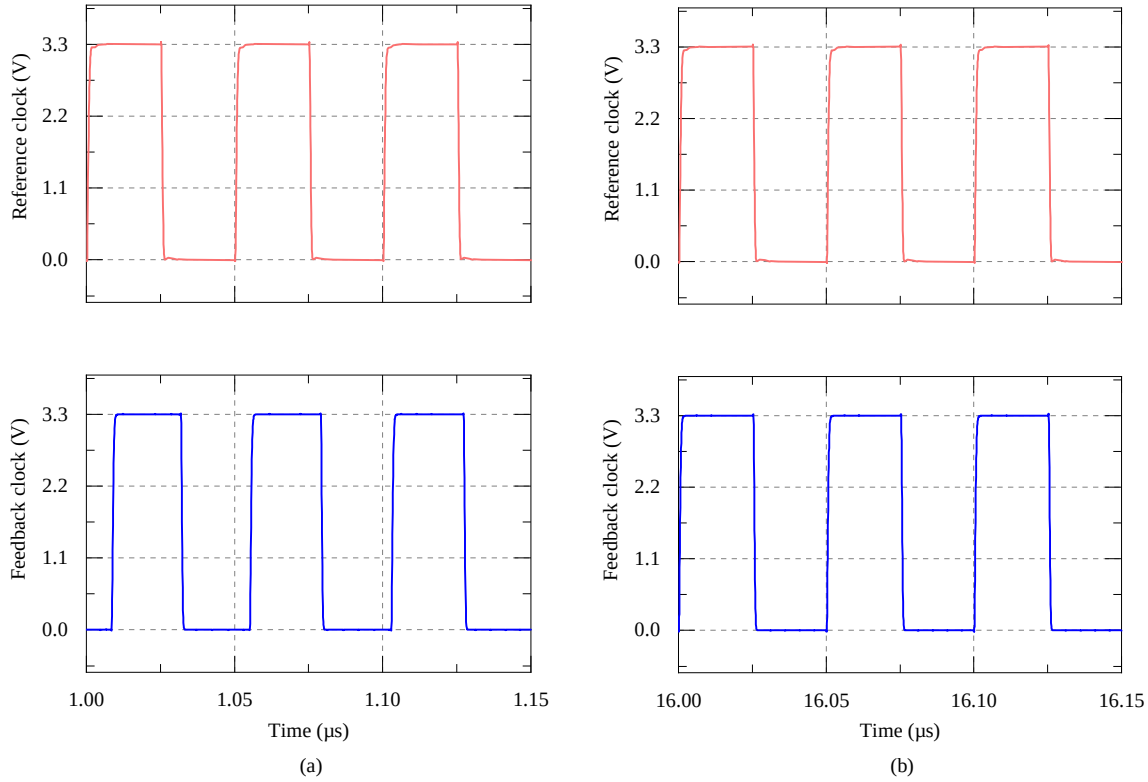



Fig. 4.30 Layout of the complete multi-phase clock generator DLL.

### DLL simulation results

The simulation results of the DLL for an input reference clock frequency of 20 MHz are presented below. Fig. 4.31 shows the transient response of the reference clock and the feedback clock (clock out 10 from the VCDL tap). It can be seen in Fig. 4.31a that the two clock signals are misaligned by certain phase difference after the DLL start up. In Fig. 4.31b, the same clocks can be seen to be fully aligned once the DLL achieves the locked state. The DLL achieves locking after 10.5 µs.




(a) (b)

Fig. 4.31 Post-layout simulation results showing the transient response of the reference clock and delayed clock; (a) transient simulation showing the misaligned reference clock and the feedback clock (output from tap 10) after start up; (b) fully aligned clocks after DLL achieved locked state.

Fig. 4.32 shows the coarse and fine control voltages of the DLL. We can observe that the coarse control voltage achieves a very fast settling as it is generated by the replica delay line which only has a single delay cell. Once the DLL achieves coarse control, the fine control loop takes over and adjusts the delay of the VCDL until the DLL reaches a fully locked state. The simulated DLL locking time is roughly 10.5 µs which is about 210 clock cycles. The

performance parameter of the DLL is listed in the table 4.2. The rms value of the edge to edge jitter is estimated using a periodic steady state (PSS) and pnoise simulation in Cadence. The accuracy of the result is verified using a transient simulation.

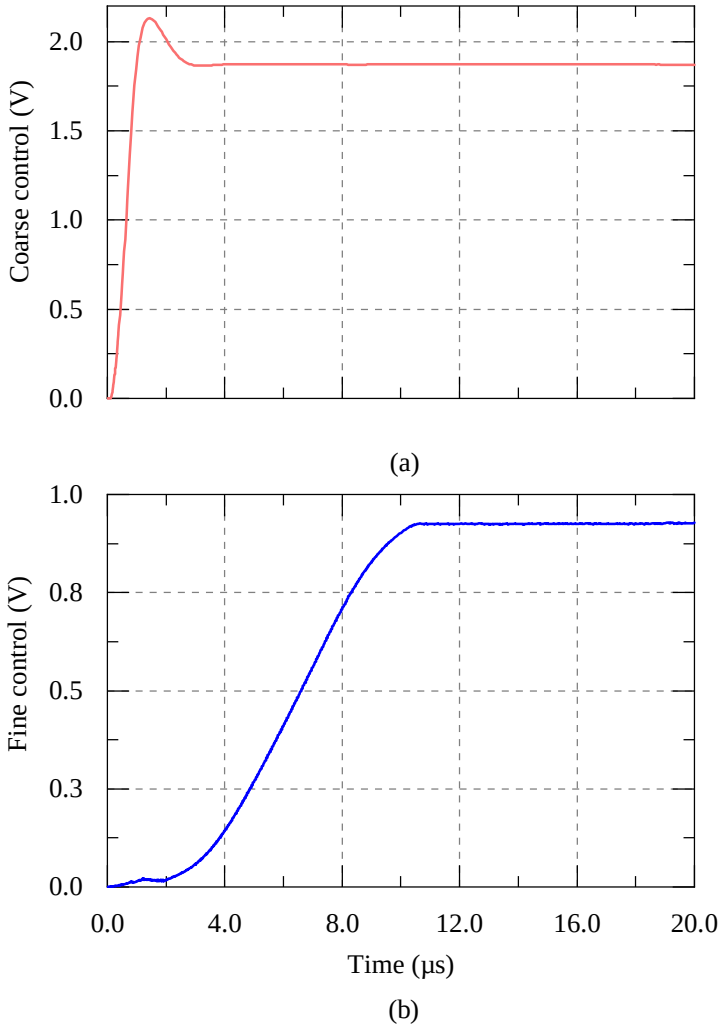



Fig. 4.32 Transient simulation showing the coarse and fine control voltages of the DLL.

To check the transient stability of the DLL, a small frequency step is applied on the reference clock after the initial settling and the DLL response is noted. It is observed that the DLL goes out of lock for a few clock cylces and then gets back to locked operation successfully. Both the control voltages show a slight jump and then settle down. This can be observed from the simulation results shown in Fig. 4.33. A 100 kHz frequency change is applied at 18 µs and at 21 µs it is changed back to the initial value of 20 MHz.

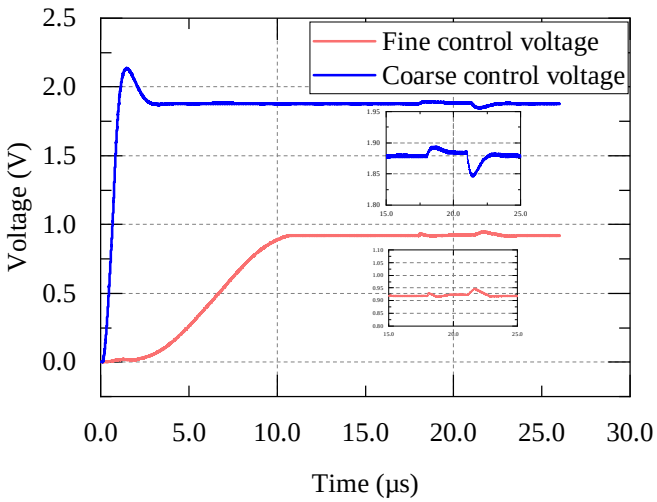



Fig. 4.33 Post-layout transient simulation showing the control voltage response for a frequency jump in the reference clock.

Table 4.2 Performance parameters of the DLL

| Parameter | Value |
|---|---|
| Reference frequency | 20 MHz |
| Locking time | 10.5 µs (210 cycles) |
| Loop bandwidth | 300 kHz |
| Static phase error | 80 ps |
| Lock range | 20 MHz to 48 MHz |
| Jitter (rms) | 10 ps |
| Area | 0.29 $mm^2$ |

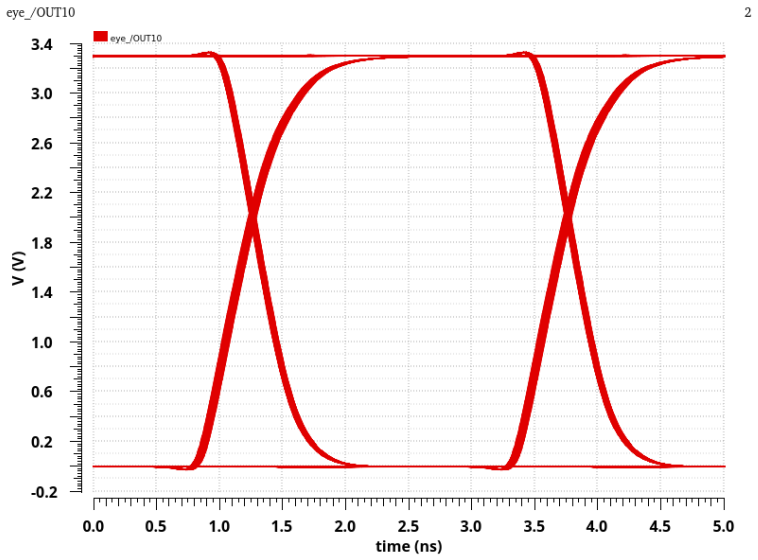



Fig. 4.34 Eye diagram of the DLL.

### 4.3.6 Transmit beamforming output simulation results

Mixed signal simulations are carried out to verify the performance of the transmit beamforming circuit. In Fig. 4.35, a transient simulation result showing the output of the HV driver channels are shown. As previously discussed, the beamforming circuit produces HV output pulses with a pre-programmed delay. The total delay is achieved by combining the coarse timing output from the 10 bit counter and the fine timing clock output generated by the DLL.

$$\text{Total delay} = \text{Coarse delay} + \text{Fine delay} \tag{4.27}$$

From the block diagram of the complete beamformer presented in Fig. 4.3, the 10 bit counter operates at the reference clock. In our case the reference clock used is 20 MHz. This gives us a delay range upto 51.1 µs. With the same clock frequency, the DLL produces a fine delay of 5 ns. Hence the smallest achievable time resolution is 5 ns. The coarse and fine delay values can be programmed on the transceiver chip using the SPI interface.

From Fig. 4.35, the fine delay programmability of the circuit is demonstrated. Each channel is set up with the same coarse delay of 200 ns and each channel has a fine delay separation of 5 ns added from the previous channel. The beamforming circuit has been implemented on a new vesion of the transceiver chip where a new HV driver circuit which switches from 0 V to 34 V. An input reference clock of 20 MHz is applied to the DLL. The internal clock divider block, divides down this clock to the desired 2 MHz output which demonstrates the frequency division capability of the design. The pulse count can also be programmed upto 127 pulses. For this simulation, the number of pulses have been set to 7. A zoomed in version of the waveforms are shown in the Fig. 4.35 to show the fine delay separation. It can be seen that each channel has its edges precisely separated from the previous channel by 5 ns.

In Fig. 4.36, the HV output pulses are shown with a coarse timing delays applied. The external trigger is applied to the chip at 28.5 µs. Each of the HV channels are programmed for a coarse delay of 2 µs between each other. This value is chosen for ease of representation graphically. A larger delay can also be programmed. To demonstrate the triggering operation of the beamforming block, the transient simulation shown in Fig. 4.37 can be used. An external trigger signal is applied at 28.5 µs. The trigger detector block will output a high when the external trigger signal is high for at least 3 clock cycles. This enables the pulse counter block and active low receive enable (RX_EN_N) is pulled high. Once the pulse counting is done, the EN_Pulse_Count signal is pulled low. The trigger detect signal stays high until the 10 bit counter is full and then it resets and awaits for the next external trigger signal. The trigger detect blocks works with the reference clock which in this case is 20 MHz.

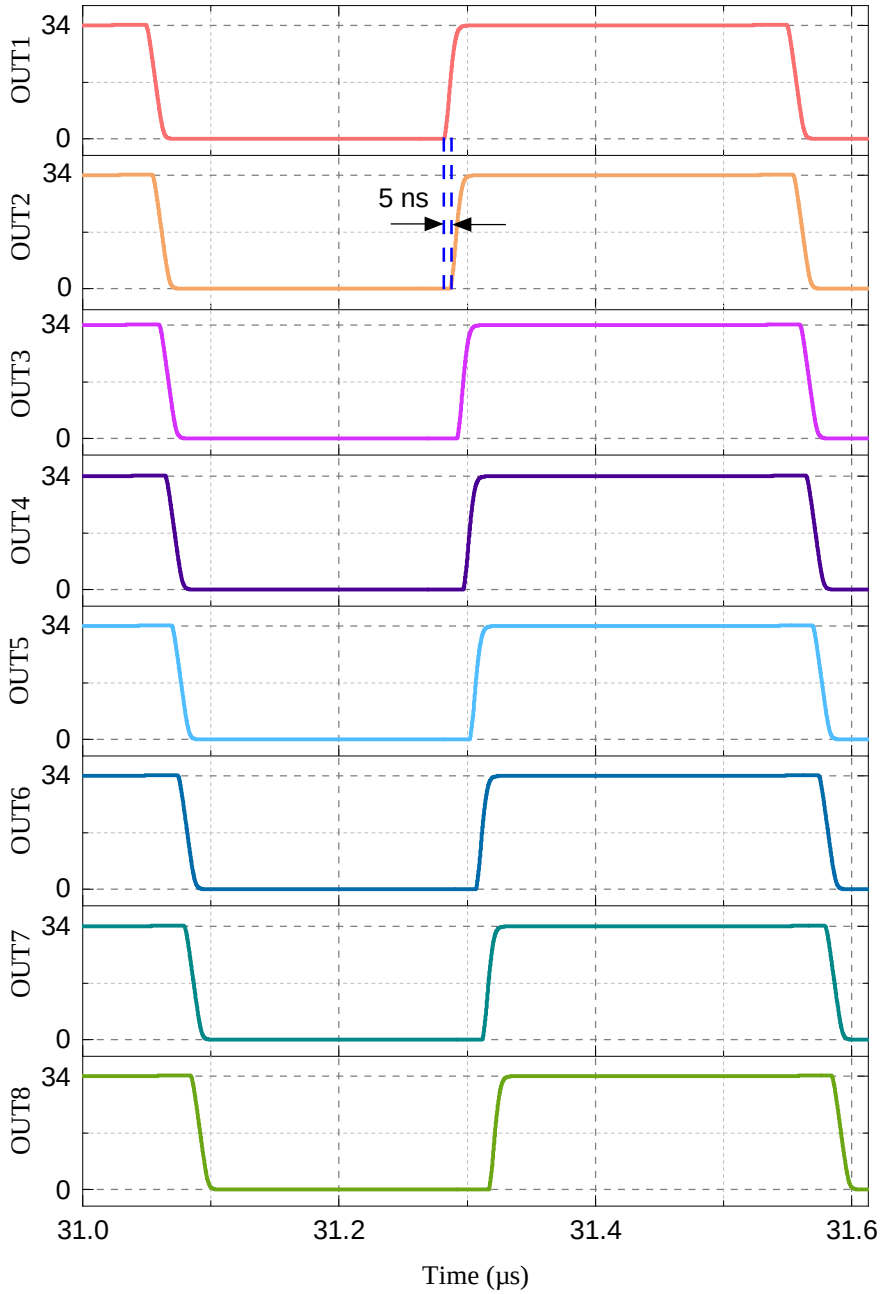



Fig. 4.35 Transient simulation showing the output of the HV driver after applying the delays. Each HV driver channel is separated by the DLL delay of 5 ns.

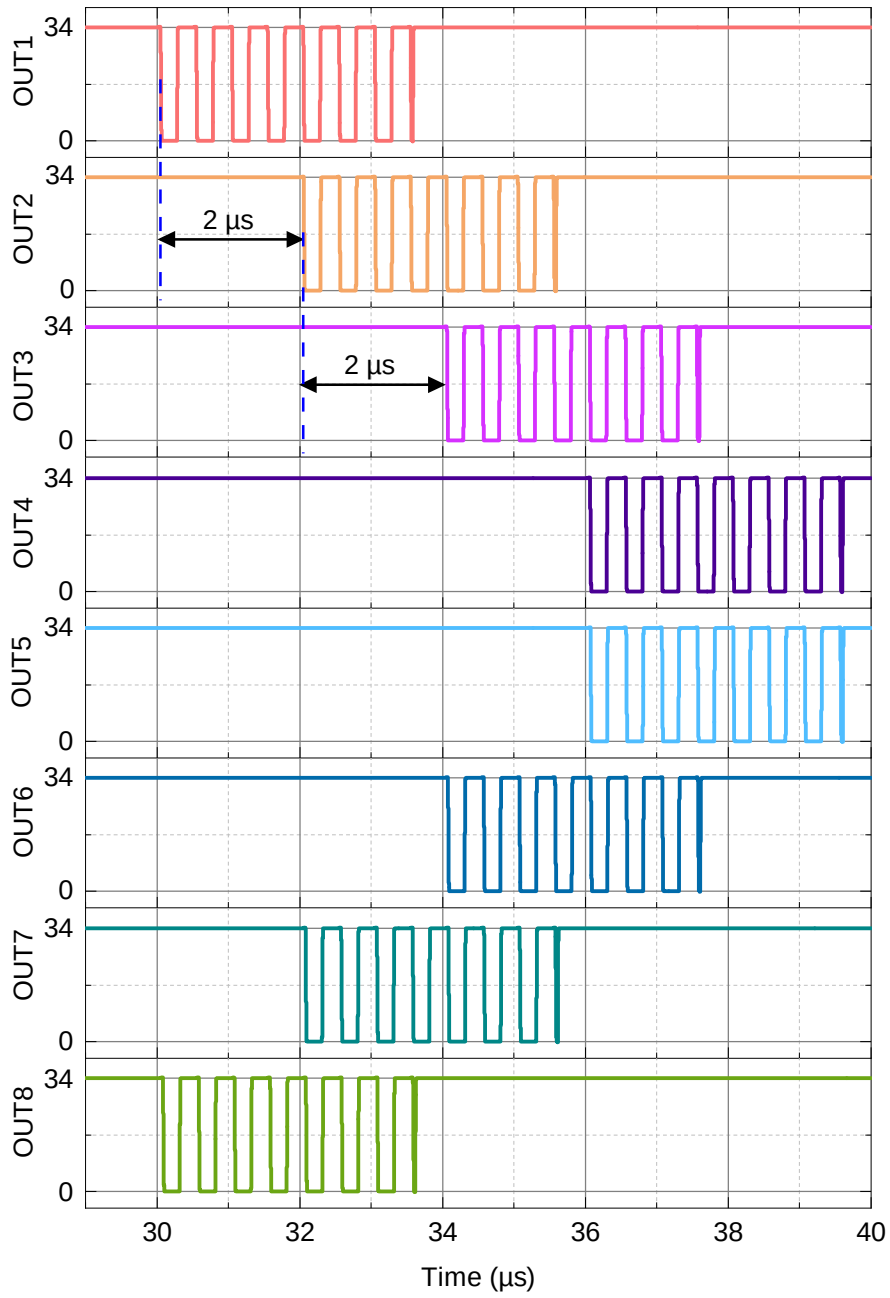



Fig. 4.36 Transient simulation showing the output of the HV driver after applying the coarse timing delays.

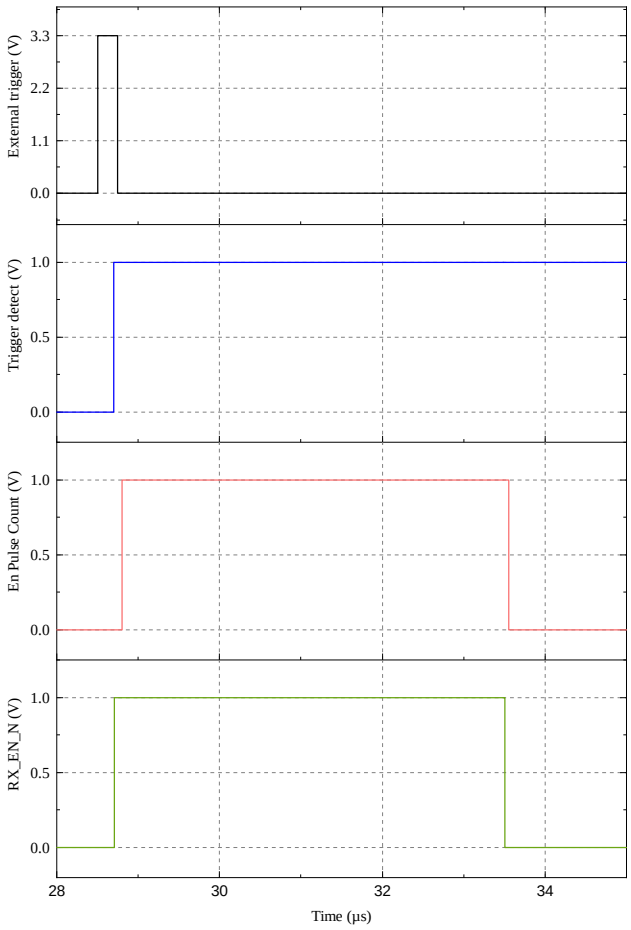



Fig. 4.37 Simulation showing the triggering operation of the beamforming block.

# Chapter 5

# Conclusion

## 5.1 Summary

Micromachined ultrasonic transducers, especially capacitive micromachined ultrasonic transducers present a promising solution for highly integrated, low-power and portable ultrasonic sensor solutions. The opportunities presented by CMUTs towards the miniaturization goal were discussed in the first two chapters. Design of a low power, area efficient interface ASIC with HV driving and low power signal conditioning capability presents a unique challenge. Monolithic or hybrid integration of the CMUT-ASIC systems opens up a number of opportunities such as short-range high-resolution proximity sensing in robotics, miniaturized hand held imaging probes, ultra-thin catheters for intra-vascular imaging and intra-cardiac echography.

This work was aimed at the development of a highly integrated ASIC for a CMUT array with the initial goal of high resolution proximity sensing in robotic grippers. Hence, an air-based CMUT-ASIC system was envisioned. The ASIC design process addressed a key challenge in the CMUT-ASIC interface system, that is to eliminate the external HV biasing for the CMUTs. The HV biasing is required for the CMUTs to operate the devices close to the pull-in voltage for maximum electro-acoustic transduction efficiency. This is true both in the transmit and receive mode. A novel pulser circuit architecture was developed in this work which addresses this issue. The system level architecture of the novel interfacing structure was presented in Chapter 2 and this was compared with the existing architecture to elucidate the advantages. A two-level pulsing scheme, that switches between two HV levels was designed. This is equivalent to dc biasing and ac HV super-imposing. Both the CMUT terminals were used for operation. The CMUT is driven on one terminal and the echo is received from the second terminal. Switches formed using low voltage MOSFETs connect the top electrode of the CMUT to ground during the transmit phase and during the receive

phase, it is connected to the input of a transimpedance amplifier. Pulse-echo measurement was carried out using a single CMUT sample in air. The ProTaktilUS_A0 chip version was used for the measurement. Using the ProTaktilUS_B0 chip, another pulse-echo measurement with CMUT immersed in fluid was performed. The system level measurement results were also presented. The results demonstrated the capability of the ASIC for successful CMUT integration. The proposed transceiver architecture was also successfully verified in the measurement.

In the receive mode, the CMUT is required to be biased close to their pull-in voltage to maximize the receive sensitivity of the CMUT. This is achieved by pulling the output of the HV pulser to the higher of the two HV levels. Further, using both the CMUT ports enabled the elimination of the HV isolation switch from the receive path. An improved noise performance was measured. Circuit blocks required to enable the ASIC for this kind of operation was investigated and implemented. Three ASIC versions with incremental performance addition were designed. Two versions of the ASIC were evaluated till date and the third ASIC version is expected to be tested soon.

Chapter 3 also presented all the key circuit blocks which were designed. The chip performances were evaluated using measurement setup in the lab and results presented and compared with prior art. The two-level HV pulser circuit was designed using an ultra low power level shifter circuit which consumes power from the HV rails only during switching. The design of a novel HV linear regulator was also presented. Two regulators were integrated on the chip. The receive path of the transceiver chip consists of a resistive feedback transimpedance amplifier. The amplifier performance was verified by measurements. The gain programmability of the TIA circuit was also demonstrated. An improved receiver circuit design with a low power TIA and a super source follower buffer was designed and verified with simulations. The design was placed on the third version of the transceiver chip.

The concept for a transmit beamforming circuitry was presented in Chapter 4. Existing beamforming circuit architectures were discussed and a new concept combining a wide range analog DLL and digital circuits to perform phased array actuation was presented. A key circuit block which is the DLL was presented in detail and performance was verified thoroughly using post-layout simulations. The beamforming circuit was also submitted in the ProTaktilUS_C0 version. The aim is to expand the capabilities of the transceiver ASIC for future applications and projects.

## 5.2 Enhancement to state of the art

Some future works that can be considered to improve the performance and capability of the CMUT transceiver ASIC includes the following:

- The required internal HV biasing was provided on our chips using linear regulators with a fixed output voltage. A design of another architecture could be investigated with an adjustable voltage range that would enable easy integration of CMUTs with a different operating voltage range.
- The current ASIC versions integrated 8 TX and 8 RX channels. The possibility of multiplexing could be looked into to reduce the pin count of the chip. This will be an absolute necessity when the chip is required to scale up for a larger number of channels.
- The existing ASIC needs three external power supplies (2 HV and 1 LV). The feasibility of on chip HV generation could be explored to generate all the required voltages on the ASIC. This could further reduce the external connections to the chip.
- The use of HV power supplies on the chip produces large power losses during operation. A study involving the long term reliability of the chip due to heating effects could provide more insights into the long-term reliability of the ASIC.

# References


[1] Dr. Joseph Woo. A short history of the developments of ultrasound in obstetrics and gynecology, 1998.

[2] Yongqiang Qiu, James V. Gigliotti, Margeaux Wallace, Flavio Griggio, Christine E. M. Demore, Sandy Cochran, and Susan Trolier-McKinstry. Piezoelectric micromachined ultrasound transducer (pmut) arrays for integrated sensing, actuation and imaging. *Sensors*, 15(4):8020–8041, 2015.

[3] J. Brown, S. Sharma, J. Leadbetter, S. Cochran, and R. Adamson. Vacuum deposition of mass-spring matching layers for high-frequency ultrasound transducers. In *2014 IEEE International Ultrasonics Symposium*, pages 101–104, 2014.

[4] I. Ladabaum, Xuecheng Jin, H. T. Soh, A. Atalar, and B. t. Khuri-Yakub. Surface micromachined capacitive ultrasonic transducers. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 45(3):678–690, 1998.

[5] M. I. Haller and B. t. Khuri-Yakub. A surface micromachined electrostatic ultrasonic air transducer. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 43(1):1–6, 1996.

[6] Kevin Brenner, Arif Sanli Ergun, Kamyar Firouzi, Morten Fischer Rasmussen, Quintin Stedman, and Butrus Pierre Khuri-Yakub. Advances in capacitive micromachined ultrasonic transducers. *Micromachines*, 10(2), 2019.

[7] Arif S. Ergun, Goksen G. Yaralioglu, and Butrus T. Khuri-Yakub. Capacitive micromachined ultrasonic transducers: Theory and technology. *Journal of Aerospace Engineering*, 16(2):76–84, 2003.

[8] Lawrence Wong. *Capacitive Micromachined Ultrasonic Transducers for Non-destructive Testing Applications*. Phd thesis, University of Waterloo, Ontario, Canada, 2014.

[9] B. Bayram, E. Haeggstrom, A. S. Ergun, G. G. Yaralioglu, and B. t. Khuri-Yakub. Dynamic analysis of cmuts in different regimes of operation. In *IEEE Symposium on Ultrasonics, 2003*, pages 481–484 Vol.1, 2003.

[10] S. Frew, H. Najar, and E. Cretu. Vhdl-ams behavioural modelling of a cmut element. In *2009 IEEE Behavioral Modeling and Simulation Workshop*, pages 19–24, 2009.

[11] Jaemyung Lim, Coskun Tekes, Evren F. Arkan, Ahmad Rezvanitabar, F. Levent Degertekin, and Maysam Ghovanloo. Highly integrated guidewire ultrasound imaging system-on-a-chip. *IEEE journal of solid-state circuits*, 55(5):1310–1323, 2020.

[12] Gwangrok Jung, Coskun Tekes, M. Wasequr Rashid, Thomas M. Carpenter, David Cowell, Steven Freear, F. Levent Degertekin, and Maysam Ghovanloo. A reduced-wire ice catheter asic with tx beamforming and rx time-division multiplexing. *IEEE Transactions on Biomedical Circuits and Systems*, 12(6):1246–1255, 2018.

[13] P. Behnamfar and S. Mirabbasi. A cmut read-out circuit with improved receive sensitivity using an adaptive biasing technique. In *2011 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, pages 397–400, 2011.

[14] A. Hölke, M. Antoniou, and F. Udrea. Partial soi as a hv platform technology for power integrated circuits. In *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 435–438, 2020.

[15] A. Hölke, D. K. Pal, Y. Hao, K. K. Yaw, E. Kho, G. Kittler, U. Kuniss, and J. Gessner. A 200v partial soi 0.18µm cmos technology. In *2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, pages 257–260, 2020.

[16] X-fab_datasheet_xt018_20210827082411.

[17] M. J. Declerq, M. Schubert, and F. Clement. 5 v-to-75 v cmos output interface circuits. In *1993 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 162–163, 1993.

[18] M. Khorasani, L. van den Berg, P. Marshall, M. Zargham, V. Gaudet, D. Elliott, and S. Martel. Low-power static and dynamic high-voltage cmos level-shifter circuits. In *2008 IEEE International Symposium on Circuits and Systems*, pages 1946–1949, 2008.

[19] Hussein Ballan and Michel Declercq. *High Voltage Devices and Circuits in Standard CMOS Technologies*. Springer US, Boston, MA, 1999.

[20] Hyunggun Ma, Gyeongho Namgoong, Eunho Choi, and Franklin Bien. Instantaneous power consuming level shifter for improving power conversion efficiency of buck converter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 66(7):1207–1211, 2019.

[21] J. Doutreloigne, H. de Smet, and A. van Calster. A versatile micropower high-voltage flat-panel display driver in a 100 v 0.7 $\mu$m cmos intelligent interface technology. *IEEE Journal of Solid-State Circuits*, 36(12):2039–2048, 2001.

[22] J. Doutreloigne, H. de Smet, J. van den Steen, and G. van Doorselaer. Low-power high-voltage cmos level-shifters for liquid crystal display drivers. In *ICM'99. Proceedings. Eleventh International Conference on Microelectronics (IEEE Cat. No.99EX388)*, pages 213–216. IEEE, 2000.

[23] Yashodhan Moghe, Torsten Lehmann, and Tim Piessens. Nanosecond delay floating high voltage level shifters in a 0.35 $\mu$m hv-cmos technology. *IEEE Journal of Solid-State Circuits*, 46(2):485–497, 2011.

[24] P. K. Poongodan, O. Sakolski, F. Vanselow, and L. Maurer. An 8 channel transceiver asic to interface a cmut array. In *2021 19th IEEE International New Circuits and Systems Conference (NEWCAS)*, pages 1–4, 2021.

[25] D. Pan, H. W. Li, and B. M. Wilamowski. A low voltage to high voltage level shifter circuit for mems application. In *Proceedings of the 15th Biennial University/Government/ Industry Microelectronics Symposium (Cat. No.03CH37488)*, pages 128–131, 2003.

[26] Byong-Deok Choi. Enhancement of current driving capability in data driver ics for plasma display panels. *IEEE Transactions on Consumer Electronics*, 55(3):992–997, 2009.

[27] Mingliang Tan, Eunchul Kang, Jae-Sung An, Zu-Yao Chang, Philippe Vince, Tony Mateo, Nicolas Senegond, and Michiel A. P. Pertijs. A 64-channel transmit beamformer with ±30-v bipolar high-voltage pulsers for catheter-based ultrasound probes. *IEEE Journal of Solid-State Circuits*, 55(7):1796–1806, 2020.

[28] Hyouk-Kyu Cha, Dongning Zhao, Jia Hao Cheong, Bin Guo, Hongbin Yu, and Minkyu Je. A cmos high-voltage transmitter ic for ultrasound medical imaging applications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(6):316–320, 2013.

[29] Aditya Banuaji and Hyouk-Kyu Cha. A 15-v bidirectional ultrasound interface analog front-end ic for medical imaging using standard cmos technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(8):604–608, 2014.

[30] Parisa Behnamfar, Reza Molavi, and Shahriar Mirabbasi. Transceiver design for cmut-based super-resolution ultrasound imaging. *IEEE Transactions on Biomedical Circuits and Systems*, 10(2):383–393, 2016.

[31] Oleg Sakolski, Prajith Kumar Poongodan, Frank Vanselow, and Linus Maurer. A feedforward compensated high-voltage linear regulator with fast response, high-current sinking capability. *IEEE Solid-State Circuits Letters*, 3:114–117, 2020.

[32] P. K. Hanumolu. Low dropout regulators. In *2015 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–37, 2015.

[33] Gabriel A. Rincón-Mora. *Analog IC design with low-dropout regulators*. Electronic engineering. McGraw-Hill Professional, New York and London, 2009.

[34] A. Garimella and P. M. Furth. Frequency compensation techniques for op-amps and ldos: A tutorial overview. In *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 1–4, 2012.

[35] C. K. Chava and J. Silva-Martinez. A frequency compensation scheme for ldo voltage regulators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 51(6):1041–1050, 2004.

[36] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J.A.G. Galan, A. Carlosena, and F. M. Chavero. The flipped voltage follower: a useful cell for low-voltage low-power circuit design. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 52(7):1276–1291, 2005.

[37] Xi Qu, Ze-Kun Zhou, Bo Zhang, and Zhao-Ji Li. An ultralow-power fast-transient capacitor-free low-dropout regulator with assistant push–pull output stage. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 60(2):96–100, 2013.

[38] Behzad Razavi. *Design of integrated circuits for optical communications*. Wiley, Hoboken, N.J, second edition edition, 2012.

[39] Ahmed Atef, Mohamed Atef, Elsayed Esam M. Khaled, and Mohamed Abbas. Cmos transimpedance amplifiers for biomedical applications: A comparative study. *IEEE Circuits and Systems Magazine*, 20(1):12–31, 2020.

[40] R. Jacob Baker. *CMOS: Circuit design, layout, and simulation*. IEEE Press series on microelectronic systems. John Wiley & Sons, Inc, Hoboken, NJ, USA, third edition edition, 2010.

[41] A. J. Lopez-Martin, E. Osés, J. Ramírez-Angulo, and R. G. Carvajal. Micropower class ab voltage followers with simple quiescent current control. In *2012 IEEE 55th International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 218–221, 2012.

[42] Agata Romanova and Vaidotas Barzdenas. A review of modern cmos transimpedance amplifiers for otdr applications. *Electronics*, 8(10):1073, 2019.

[43] Douwe M. van Willigen, Eunchul Kang, Jovana Janjic, Emile Noothout, Zu-Yao Chang, Martin D. Verweij, Nico de Jong, and Michiel A. P. Pertijs. A transceiver asic for a single-cable 64-element intra-vascular ultrasound probe. *IEEE Journal of Solid-State Circuits*, 56(10):3157–3166, 2021.

[44] Mingliang Tan, Chao Chen, Zhao Chen, Jovana Janjic, Verya Daeichin, Zu-Yao Chang, Emile Noothout, Gijs van Soest, Martin D. Verweij, Nico de Jong, and Michiel A. P. Pertijs. A front-end asic with high-voltage transmit switching and receive digitization for 3-d forward-looking intravascular ultrasound imaging. *IEEE Journal of Solid-State Circuits*, 53(8):2284–2297, 2018.

[45] H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, and K. Sakui. A cmos bandgap reference circuit with sub-1-v operation. *IEEE Journal of Solid-State Circuits*, 34(5):670–674, 1999.

[46] A. Rezvanitabar, M. S. Kilinc, C. Tekes, E. F. Arkan, M. Ghovanloo, and F. L. Degertekin. An ultrasound imaging front-end system-on-a-chip with element-level impedance matching for acoustic reflectivity reduction. In *2021 IEEE Biomedical Circuits 2021*, pages 01–04.

[47] Thomas L. Szabo, editor. *Diagnostic ultrasound imaging: Inside out*. MATLAB examples. Elsevier/AP Academic Press is an imprint of Elsevier, Amsterdam and Boston, second edition edition, 2014.

[48] O. T. von Ramm and S. W. Smith. Beam steering with linear arrays. *IEEE transactions on bio-medical engineering*, 30(8):438–452, 1983.

[49] J. C. Somer. Electronic sector scanning for ultrasonic diagnosis. *Ultrasonics*, 6(3):153–159, 1968.

[50] F. L. Thurstone and O. T. von Ramm. A new ultrasound imaging technique employing two-dimensional electronic beam steering. In Philip S. Green, editor, *Acoustical Holography: Volume 5*, pages 249–259. Springer US, Boston, MA, 1974.

[51] O. T. von Ramm and F. L. Thurstone. Thaumascan: Design considerations and performance characteristics. In Denis White, editor, *Ultrasound in Medicine: Volume 1 Proceedings of the 19th Annual Meeting of the American Institute of Ultrasound in Medicine*, pages 373–378. Springer US, Boston, MA, 1975.

[52] Thomas R. Nelson and Dolores H. Pretorius. Three-dimensional ultrasound imaging. *Ultrasound in Medicine & Biology*, 24(9):1243–1270, 1998.

[53] Ira O. Wygant, Nafis S. Jamal, Hyunjoo J. Lee, Amin Nikoozadeh, Omer Oralkan, Mustafa Karaman, and Butrus T. Khuri-Yakub. An integrated circuit with transmit beamforming flip-chip bonded to a 2-d cmut array for 3-d ultrasound imaging. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 56(10):2145–2156, 2009.

[54] G. Gurun, C. Tekes, J. Zahorian, T. Xu, S. Satir, M. Karaman, J. Hasler, and F. L. Degertekin. Single-chip cmut-on-cmos front-end system for real-time volumetric ivus and ice imaging. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 61(2):239–250, 2014.

[55] Anshuman Bhuyan, Jung Woo Choe, Byung Chul Lee, Ira O. Wygant, Amin Nikoozadeh, Ömer Oralkan, and Butrus T. Khuri-Yakub. Integrated circuits for volumetric ultrasound imaging with 2-d cmut arrays. *IEEE Transactions on Biomedical Circuits and Systems*, 7(6):796–804, 2013.

[56] A. Bhuyan, Chienliu Chang, J. W. Choe, B. C. Lee, A. Nikoozadeh, Ø. Oralkan, and B. t. Khuri-Yakub. A 32×32 integrated cmut array for volumetric ultrasound imaging. In *2014 IEEE International Ultrasonics Symposium*, pages 545–548, 2014.

[57] Yutaka Igarashi, Shinya Kajiyama, Yusaku Katsube, Takuma Nishimoto, Tatsuo Nakagawa, Yasuyuki Okuma, Yohei Nakamura, Takahide Terada, Taizo Yamawaki, Toru Yazaki, Yoshihiro Hayashi, Kazuhiro Amino, Takuya Kaneko, and Hiroki Tanaka. Single-chip 3072-element-channel transceiver/128-subarray-channel 2-d array ic with analog rx and all-digital tx beamformer for echocardiography. *IEEE Journal of Solid-State Circuits*, 54(9):2555–2567, 2019.

[58] N. R. Scales, P. J. Hicks, A. D. Armitage, P. A. Payne, Q. X. Chen, and J. V. Hatfield. A programmable multi-channel cmos pulser chip to drive ultrasonic array transducers. *IEEE Journal of Solid-State Circuits*, 29(8):992–994, 1994.

[59] Peter R. Smith, David M. J. Cowell, Benjamin Raiton, Chau Vo Ky, and Steven Freear. Ultrasound array transmitter architecture with high timing resolution using embedded phase-locked loops. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 59(1):40–49, 2012.

[60] John V. Hatfield and Kwet Seng Chai. A beam-forming transmit asic for driving ultrasonic arrays. *Sensors and Actuators A: Physical*, 92(1-3):273–279, 2001.

[61] Georgios I. Athanasopoulos, Stephen J. Carey, and John V. Hatfield. Circuit design and simulation of a transmit beamforming asic for high-frequency ultrasonic imaging systems. *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, 58(7):1320–1331, 2011.

[62] J. G. Maneatis. Low-jitter process-independent dll and pll based on self-biased techniques. *IEEE Journal of Solid-State Circuits*, 31(11):1723–1732, 1996.

[63] Eunseok Song, Seung-Wook Lee, Jeong-Woo Lee, Joonbae Park, and Soo-Ik Chae. A reset-free anti-harmonic delay-locked loop using a cycle period detector. *IEEE Journal of Solid-State Circuits*, 39(11):2055–2061, 2004.

[64] Behzad Razavi. Delaylocked loops an overview. In *Phase-Locking in High-Performance Systems: From Devices to Architectures*, pages 13–22. IEEE, 2003.

[65] Kyungho Ryu, Kil-Hoon Lee, Jung-Pil Lim, Jinho Kim, Hansu Pae, Junho Park, Hyun-Wook Lim, and Jae-Youl Lee. An analytical jitter tolerance model for dll-based clock and data recovery circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 28(11):2257–2267, 2020.

[66] Kuo-Hsing Cheng, Shu-Ming Chang, Yu-Lung Lo, and Shu-Yu Jiang. A 2.2 ghz programmable dll-based frequency multiplier for soc applications. In *Proceedings of 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits*, pages 72–75, 2004.

[67] Jia Cheng. *A delay-locked loop for multiple clock phases/delays generation*. Phd, Georgia Institute of Technology, 2005.

[68] Anantha P. Chandrakasan, Frank Fox, and William J. Bowhill. *Design of high-performance microprocessor circuits*. IEEE Press, New York, 2001.

[69] Neil H. E. Weste and David Money Harris. *CMOS VLSI design: A circuits and systems perspective*. Addison Wesley, Boston, 4th ed. edition, 2011.

[70] Yongsam Moon, Jongsang Choi, Kyeongho Lee, Deog-Kyoon Jeong, and Min-Kyu Kim. A 62.5-250 mhz multi-phase delay-locked loop using a replica delay line with triply controlled delay cells. In *Proceedings of the IEEE 1999 Custom Integrated Circuits Conference (Cat. No.99CH36327)*, pages 299–302, 1999.

[71] S. Sidiropoulos and M. A. Horowitz. A semidigital dual delay-locked loop. *IEEE journal of solid-state circuits*, 32(11):1683–1692, 1997.

[72] S. Tanoi, T. Tanabe, K. Takahashi, S. Miyamoto, and M. Uesugi. A 250-622 mhz deskew and jitter-suppressed clock buffer using two-loop architecture. *IEEE journal of solid-state circuits*, 31(4):487–493, 1996.

[73] Chi-Nan Chuang and Shen-Iuan Liu. A 0.5–5-ghz wide-range multiphase dll with a calibrated charge pump. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 54(11):939–943, 2007.

[74] Chi-Nan Chuang and Shen-Iuan Liu. A 20-mhz to 3-ghz wide-range multiphase delay-locked loop. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 56(11):850–854, 2009.

[75] Yong-Hwan Moon, In-Seok Kong, Young-Soo Ryu, and Jin-Ku Kang. A 2.2-mw 20–135-mhz false-lock-free dll for display interface in 0.15- $\mum$ cmos. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 61(8):554–558, 2014.

[76] Yongsam Moon, Deog-Kyoon Jeong, and Gyudong Kim. Clock dithering for electromagnetic compliance using spread spectrum phase modulation. In *1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No.99CH36278)*, pages 186–187, 1999.

[77] Yongsam Moon, Jongsang Choi, Kyeongho Lee, Deog-Kyoon Jeong, and Min-Kyu Kim. An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance. *IEEE Journal of Solid-State Circuits*, 35(3):377–384, 2000.

[78] M. G. Johnson and E. L. Hudson. A variable delay line pll for cpu-coprocessor synchronization. *IEEE journal of solid-state circuits*, 23(5):1218–1223, 1988.

[79] M. Saint-Laurent and M. Swaminathan. A digitally adjustable resistor for path delay characterization in high-frequency microprocessors. In *2001 Southwest Symposium on Mixed-Signal Design (Cat. No.01EX475)*, pages 61–64, 2001.

[80] M. Maymandi-Nejad and M. Sachdev. A digitally programmable delay element: design and analysis. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 11(5):871–878, 2003.

[81] G. S. Jovanović and M. K. Stojčev. Current starved delay element with symmetric load. *International Journal of Electronics*, 93(3):167–175, 2006.

[82] H. Notani, H. Kondoh, and Y. Matsuda. A 622-mhz cmos phase-locked loop with precharge-type phase frequency detector. In *Proceedings of 1994 IEEE Symposium on VLSI Circuits*, pages 129–130, 1994.

[83] W. Rhee. Design of high-performance cmos charge pumps in phase-locked loops. In *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 545–548 vol.2, 1999.

[84] M.-S. Hwang, J. Kim, and D.-K. Jeong. Reduction of pump current mismatch in charge-pump pll. *Electronics Letters*, 45(3):135, 2009.

[85] Chithra, Aditya Narayanan, R. S. Ashwin Kumar, and Nagendra Krishnapura. Auto-zeroing static phase offset in dlls using a digitally programmable sensing circuit. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 68(6):1788–1792, 2021.

[86] Jae-Shin Lee, Min-Sun Keel, Shin-Il Lim, and Suki Kim. Charge pump with perfect current matching characteristics in phase-locked loops. *Electronics Letters*, 36(23):1907, 2000.

[87] Chithra and N. Krishnapura. Static phase offset reduction technique for delay locked loops. In *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, pages 1–5.

[88] Xingyuan Tong, Jinwu Wu, and Dong Chen. Low-phase-error small-area 4-phase dll with a single-ended-differential-single-ended voltage-controlled delay line. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 69(1):25–29, 2022.

[89] Motahhareh Estebsari, Mohammad Gholami, and Mohammad Javad Ghahramanpour. A novel charge pump with low current for low-power delay-locked loops. *Circuits, Systems, and Signal Processing*, 36(9):3514–3526, 2017.

[90] N. Joram, R. Wolf, and F. Ellinger. High swing pll charge pump with current mismatch reduction. *Electronics Letters*, 50(9):661–663, 2014.

[91] J. H. Huijsing and D. Linebarger. Low-voltage operational amplifier with rail-to-rail input and output ranges. *IEEE journal of solid-state circuits*, 20(6):1144–1150, 1985.

[92] Johan Huijsing. *Operational Amplifiers: Theory and Design*. SpringerLink Bücher. Springer Netherlands, Dordrecht, 2011.

[93] T.A.F. Duisters and E. C. Dijkmans. A -90-db thd rail-to-rail input opamp using a new local charge pump in cmos. *IEEE journal of solid-state circuits*, 33(7):947–955, 1998.

# Publications

## Conference and Journal publications

Below listed are the papers published during the project time frame:

- P. K. Poongodan, P. P. Bora, D. Borggreve, F. Vanselow and L. Maurer, "A low power, offset compensated, CMOS only bandgap reference in 22 nm FD-SOI technology," 2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2018, pp. 1-4, doi: 10.1109/MOCAST.2018.8376639
- P. K. Poongodan, F. Vanselow and L. Maurer, "A Two-Level, High Voltage Driver Circuit with Nanosecond Delay for Ultrasonic Transducers," 2020 9th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2020, pp. 1-4, doi: 10.1109/MOCAST49295.2020.9200247
- O. Sakolski, P. K. Poongodan, F. Vanselow and L. Maurer, "A Feedforward Compensated High-Voltage Linear Regulator With Fast Response, High-Current Sinking Capability," in IEEE Solid-State Circuits Letters, vol. 3, pp. 114-117, 2020, doi: 10.1109/LSSC.2020.3005787
- P. K. Poongodan, O. Sakolski, F. Vanselow and L. Maurer, "An 8 Channel Transceiver ASIC to Interface a CMUT Array," 2021 19th IEEE International New Circuits and Systems Conference (NEWCAS), 2021, pp. 1-4, doi: 10.1109/NEWCAS50681.2021.9462791
- F. Vanselow, P. Poongodan, O. Sakolski and L. Maurer, "A New Switching Scheme For High-Voltage Switched Capacitor DC-DC Converter," 2021 10th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2021, pp. 1-4, doi: 10.1109/MOCAST52088.2021.9493344
- S. G. Koch et al., "Empowering Robots for Multimodal Tactile Gripping using Capacitive Micromachined Ultrasonic Transducers," 2021 Smart Systems Integration (SSI), 2021, pp. 1-5, doi: 10.1109/SSI52265.2021.9467023

# Appendix A

# Verilog codes

## Verilog codes

The verilog codes for the various digital blocks used in the transmit beamforming circuitry are listed below:

### Coarse timer module

```
//Verilog HDL for "Digital_blocks_beamforming", "Coarse_Timer_v21" "functional"
 module Coarse_Timer_v21 ( i_clk, i_trigger_ext, i_reset_n, o_coarse_time, o_trigger_ok );

//input ports

input i_clk;
input i_trigger_ext;
input i_reset_n;

//output ports

output [9:0] o_coarse_time;
output o_trigger_ok;

//output ports data types
reg [9:0] o_coarse_time;
reg o_trigger_ok;
```

```
//internal variables
reg [4:0] counter_trigger;
reg count_full;

always@(posedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 1'b0)
begin
o_coarse_time <= 10'd0;
counter_trigger <= 4'd0;
o_trigger_ok <= 1'b0;
count_full <= 1'b0;
end // if (i_reset_n == 0)

else
begin
counter_trigger <= counter_trigger[2:0], i_trigger_ext;
if(counter_trigger[4:0] == 5'b01111) // test for bit 4 == 0, so set o_trigger_ok only at beginning of pulse

begin o_trigger_ok <= 1'b1; // when the external trigger input is high for
//counter_trigger <= 4'd0;// more than 3 clock cycles, give the trigger_ok flag.
end if(o_trigger_ok==1'b1 and o_coarse_time != 10'b1111111111) // check if the trigger_ok flag is high

begin //and the coarse timer value is not 10b'11 1111 1111
o_coarse_time <= o_coarse_time + 10'd1;// run the 10 bit counter
count_full <= 1'b0;
end

else if(o_coarse_time == 10'b1111111111)
begin
o_coarse_time <= 10'd0;// if the 10 bit counter is full, reset the counter,
count_full <= 1'b1; //give a count_full flag
o_trigger_ok <= 1'b0;
end
```

```
else if (count_full == 1'b1)
begin
count_full <= 1'b0;
end

end // else: !if(i_reset_n == 0)
end // always@ (posedge i_clk or negedge i_reset_n)
endmodule
```

**Fine timer module**

```
//Verilog HDL for "Digital_blocks_beamforming", "fine_timer" "functional"

module fine_timer_v2 ( i_count_in, i_reset_n, i_coarse_time_reg, i_frequency_divider,
i_pulse_count_reg, i_dll_clk_ph, i_sel_dll_ph, i_trigger_ok, o_clk_out, o_rx_en_n );
//input ports

input [9:0] i_count_in; //count from the 10 bit coarse counter timer.
input i_reset_n;
input [9:0] i_coarse_time_reg; //register to store 10 bit coarse time values to compare
input [7:0] i_frequency_divider; //6 bit frequency divider reg. Tie [7:6]=2'b11;
input [7:0] i_pulse_count_reg; //8 bit pulse counter reg value. Divided clock is the input.
input [9:0] i_dll_clk_ph; //10 DLL clk phases. clk9 is phase0.
input [3:0] i_sel_dll_ph; //4 bit i/p for mux> DLL phase selector.
input i_trigger_ok; //trigger ok signal from coarse counter.

//output ports output o_clk_out;
output o_rx_en_n; //rx path enable control signal

//output port declaration.
wire o_clk_out;
wire o_rx_en_n;

//port wires
wire flag_pulse_counter; //flag from the pulse counter block when count is reached
wire en_pulse_counter; //connect comparator out to enabling pulse_counter
```

```
wire divided_clk; //connect output of pulse counter to phase shifter
wire mux_clk_out; //connect mux output to phase shifter
wire rx_en_n;

//connect coarse comparator module
Comparator_Coarse_Time_v1 comparator( .i_clk(i_dll_clk_ph[9]), .i_count_in(i_count_in),
.i_reset_n(i_reset_n), .i_coarse_time_reg(i_coarse_time_reg), .i_pulse_counter_flag(flag_pulse_counter),
.o_count_ok(en_pulse_counter) );

//connect clk_divider_pulse counter module
clk_divider_pulse_counter clk_divider_pulse_counter1( .i_reset_n(i_reset_n), .i_clk(i_dll_clk_ph[9]),
.i_frequency_divider(i_frequency_divider), .i_enable(en_pulse_counter), .i_pulse_count_reg(i_pulse_count_reg
.o_clk_out(divided_clk), .o_count_done(flag_pulse_counter) );

//connect_clk_mux module
clk_mux_10to1 clk_mux( .i_clk(i_dll_clk_ph), .i_sel_ph(i_sel_dll_ph), .i_reset_n(i_reset_n),
.o_clk_out(mux_clk_out) );

//connect phase shifter module
phase_shifter phase_shifter1 ( .i_clk(mux_clk_out), .i_in(divided_clk), .i_reset_n(i_reset_n),
.o_out(o_clk_out) );

//connect rx_enable module
rx_enable rx_ena( .i_clk(mux_clk_out), .i_reset_n(i_reset_n), .i_trigger_ok(i_trigger_ok),
.i_count_done(flag_pulse_counter), .o_rx_en_n(rx_en_n) );

//phase shift the rx enable out
phase_shifter phase_shifter2( .i_clk(mux_clk_out), .i_in(rx_en_n), .i_reset_n(i_reset_n),
.o_out(o_rx_en_n) );

endmodule
```

**Clock divider and pulse counter module**

```
//Verilog HDL for "Digital_blocks_beamforming", "clk_divider_pulse_counter"

module clk_divider_pulse_counter ( i_reset_n, i_clk, i_frequency_divider, i_enable, i_pulse_count_reg,
```

```
o_clk_out, o_count_done );

//input port
input i_clk;
input i_reset_n;
input [7:0] i_frequency_divider;
input i_enable;
input [7:0] i_pulse_count_reg;

//output port
output o_clk_out;
output o_count_done;

//output port declaration
reg o_clk_out;
wire o_count_done;

//port wires
wire int_divided_clk_2x;
wire clk_data;
wire int_en_clk_out;

//connect clk divider module
Clock_Divider_v1 clock_divider ( .i_reset_n(i_reset_n), .i_clk(i_clk), .i_divider(i_frequency_divider),
.o_clk_data(clk_data), .o_gclk_out(int_divided_clk_2x) );

//connect pulse counter module
Pulse_Counter_v2 pulse_counter ( .i_clk(int_divided_clk_2x), .i_clk_data(clk_data), .i_reset_n(i_reset_n),
.i_enable(i_enable), .i_pulse_count_reg(i_pulse_count_reg), .o_count_done(o_count_done),
.o_en_clk_out(int_en_clk_out) );

always @(posedge int_divided_clk_2x or negedge i_reset_n) begin
if (i_reset_n == 1'b0)
begin
o_clk_out <= 1'b0;
end
```

```
else
begin
if (int_en_clk_out || clk_data) o_clk_out <= !clk_data;
end
end // always @ (posedge clk_int or negedge i_reset_n)

endmodule
```

**Clock gate module**

```
//Verilog HDL for "Digital_blocks_beamforming", "clk_gate_gtech" "structural"

module clk_gate_gtech ( ck_in, enable, ck_out );

input enable;
output ck_out;
input ck_in;

LGCP_5VX1 iICG ( .E(enable), .CLK(ck_in), .GCLK(ck_out) );

endmodule
```

**Clock divider module**

```
//Verilog HDL for "Digital_blocks_beamforming", "Clock_Divider_v1" "functional"

module Clock_Divider_v1 ( i_reset_n, i_clk, i_divider, o_clk_data, o_gclk_out );

parameter WIDTH = 8; // Number of bits needed to count up to N
parameter N = 64; // Clock divisor / 2(max. 2^WIDTH)

//input ports
input i_reset_n;
input i_clk;
input [WIDTH-1:0] i_divider;

//output ports
```

```
output o_clk_data;
output o_gclk_out;

//output data type declarations
reg o_clk_data;

//internal variables
reg [WIDTH-1:0] last_count;
wire [WIDTH-1:0] count;

reg reg_clkpulse;

always@(posedge i_clk or negedge i_reset_n)
begin
if (i_reset_n == 1'b0)
begin
last_count <= WIDTH1'b0;
o_clk_data <= 1'b0;
reg_clkpulse <= 1'b0;
end

else
begin
if (last_count >=  i_divider) // (count == N - i_divider)
begin
last_count <= WIDTH1'b0;
o_clk_data <= !o_clk_data;
reg_clkpulse <= 1'b1;
end

else
begin
last_count <= count;
reg_clkpulse <= 1'b0;
end
```

```
end // else: !if(i_reset_n == 0)
end // always@ (posedge i_clk or negedge i_reset_n)

assign count = last_count + WIDTH-11'b0, 1'b1;

clk_gate_gtech clk_gate_inst ( .ck_in(i_clk), .enable(reg_clkpulse), .ck_out(o_gclk_out)
);

endmodule
```

**Coarse time comparator module**

```
//Verilog HDL for "Digital_blocks_beamforming", "Comparator_Coarse_Time_v1""functional"

module Comparator_Coarse_Time_v1 ( i_clk, i_count_in, i_reset_n, i_coarse_time_reg,
i_pulse_counter_flag, // this is the output of the pulse counter block which goes high when
the pulse counting is done o_count_ok );

//input ports
input i_clk;
input [9:0] i_count_in; // count input coming from the 10 bit coarse counter
input i_reset_n;
input [9:0] i_coarse_time_reg; // coarse time value stored in the 10 bit register
input i_pulse_counter_flag;

//output ports
 output o_count_ok;

//output port data type declarations
reg o_count_ok;
reg [9:0] coarse_time_reg;

always@(posedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 1'b0)
begin
o_count_ok <= 1'b0;
```

```
coarse_time_reg <= 10'd0;
end

else
begin
if(i_count_in == coarse_time_reg)
begin
o_count_ok <= 1'b1;
end

else if(i_pulse_counter_flag == 1'b1)
begin
o_count_ok <= 1'b0;
end
coarse_time_reg <= i_coarse_time_reg;

end // else: !if(i_reset_n == 0)
end // always@ (posedge i_clk or negedge i_reset_n)

endmodule
```

**3 to 10 decoder module**

```
//Verilog HDL for "Digital_blocks_beamforming", "Decoder_3to10" "functional"

module Decoder_3to10 ( i_clk, i_reset_n, i_decoder_in, o_decoder_out );

//input ports
input i_clk;
input i_reset_n;
input [3:0] i_decoder_in;

//output ports
output [9:0] o_decoder_out;

//output port declaration
wire [9:0] o_decoder_out;
```

```
//internal variables
reg sig_int0_del;
reg [9:0] sig_int;
reg [3:0] decoder_in;

assign o_decoder_out = sig_int[9:1], sig_int0_del;

always@(posedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 1'b0)
begin
sig_int[9:0] <= 10'b0000000000;
decoder_in <= 4'b1111;
end
else
begin
if ($unsigned(decoder_in) < 4'd10)
begin
if (sig_int == 10'h000)
begin
sig_int[$unsigned(decoder_in)] <= 1'b1;
end
else if (|(sig_int &  (10'd1 « $unsigned(decoder_in))) != 1'b0)
begin
sig_int <= 10'h000;
end
end // if ($unsigned(decoder_in) < 4'd10)
else
begin
sig_int <= 10'h000;
end // else: !if($unsigned(decoder_in) < 4'd10)
decoder_in <= i_decoder_in;
end // else: !if(i_reset_n == 1'b0)
end // always@ (posedge i_clk or negedge i_reset_n)
```

```
// delay sig_int[0] by half a clock to ease timing (added EB 2021-06-25)
always@(negedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 1'b0)
begin
sig_int0_del <= 1'b0;
end
else
begin
sig_int0_del <= sig_int[0];
end // else: !if(i_reset_n == 1'b0)
end // always@ (negedge i_clk or negedge i_reset_n)

endmodule
```

**Phase shifter module**

```
//Verilog HDL for "Digital_blocks_beamforming", "phase_shifter" "functional"

module phase_shifter ( i_clk, i_in, i_reset_n, o_out );

//input ports
input i_clk;
input i_in;
input i_reset_n;

//output ports
output o_out;

//output port declaration
reg o_out;

always@(posedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 0)
begin
o_out <= 0;
```

```
end

else
begin
o_out <= i_in;
end
end

endmodule
```

**RX enable module**

```
//Verilog HDL for "Digital_blocks_beamforming", "rx_enable" "functional"

module rx_enable ( i_clk, i_reset_n, i_trigger_ok, i_count_done, o_rx_en_n );

//input port
 input i_clk;
input i_reset_n;
input i_trigger_ok;
input i_count_done;

//output port
output o_rx_en_n;

//output port declaration
 reg o_rx_en_n;

//internal
reg flag1;

always@(posedge i_clk or negedge i_reset_n)
begin
if(i_reset_n == 1'b0)
begin
o_rx_en_n <= 1'b0; //keep the rx path enabled by default
flag1 <= 0;
```

```
end
else
begin
if(i_count_done == 1'b1)
begin
o_rx_en_n <= 1'b0; //enable the rx path when counting is done

end
else if(i_trigger_ok == 1'b1 && flag1 != 1)
begin
o_rx_en_n <= 1'b1; //disable the rx path once the trigger is detected
end
else
begin
o_rx_en_n <= 1'b0; //enable rx path
end

if(i_trigger_ok ==1 && i_count_done ==1)
begin
flag1 <= 1;
end
else if(i_trigger_ok ==0)
begin
flag1 <= 0;
end

end
end

endmodule
```