A Methodology to Generate Transient Behavioral Models of Complete ICs out of Design Data for ESD and Electrical Stress Simulation on System Level

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Abstract

Designing electronic (sub-)systems to be robust against ESD events is still not an easy task and a standard approach is not yet available. Accurate high frequency and high current models of all involved components are necessary to get precise system ESD simulation results, which help to optimize the ESD robustness of (sub-)systems. Often, the most critical devices in this context are ICs. There are typically no adequate IC ESD models available. A lot of requirements exist for such models: on the one hand, these IC models need to precisely replicate the IC behavior in case of ESD events. On the other hand, these models need to be quite compact to enable short computation times and protect the IP of the IC vendor. Additionally, a mechanism inside the model is desired to assess if the applied pulse can damage the IC.

Available modeling methodologies mostly focus on special device types (e.g. bipolar transistors) and hence their usage is limited. The biggest disadvantage of existing IC modeling approaches is the need of measurements with complete ICs. These measurements are very resource intense in terms of equipment and staff. Typically, numerous pin-combinations need to be measured with various pulse lengths to get the necessary data for model generation.

This work introduces a novel methodology to derive the IC ESD model out of the design data. A generic model architecture for different device types is the basis. This generic architecture allows to describe several devices with only one model. Complex circuits can be reduced to only one or a few model devices. Very compact ESD models of complete ICs are the result which demand only little computing resources and successfully protect the IP of the IC vendor. It is shown with the examples of two typical automotive ICs that the desired accuracy of $\pm$ 20 % is reached. The ESD clamping behavior and the transient behavior of the derived models match well with measurement results. Furthermore, the destruction limit of the single IC as well as the IC in small systems is accurately reproduced.

Additionally, a comprehensive methodology to characterize and model the high current behavior of common mode inductors is presented. This methodology enables precise system ESD simulations in terms of transient response and destruction limit in case of ESD events for differential communication systems with common mode inductors.

Kurzfassung

Es ist immer noch keine leichte Aufgabe die ESD Festigkeit von elektronischen Systemen und Sub-Systemen auf das geforderte Maß zu bringen.

Um aussagekräftige Simulationsergebnisse auf Systemebene zu erhalten sind präzise Hochfrequenz und Hochstrom Modelle von allen beteiligten Komponenten nötig.

In der Regel stehen keine passenden IC ESD Modelle zur Verfügung, was das wohl größte Hindernis darstellt. An solche IC ESD Modelle gibt es eine ganze Reihe unterschiedlicher Anforderungen.

Zum Einen müssen die IC Modelle die Reaktion des ICs auf ESD Entladungen, auch im transienten Verlauf, korrekt abbilden, auf der anderen Seite sollen aber die Modelle möglichst kompakt sein. Durch kompakte Modelle will man vor allem die benötigten Rechenzeiten in vernünftigen Grenzen halten. Dies ermöglicht auch einen effektiven Schutz des geistigen Eigentums des IC Herstellers. Wünschenswert wäre zudem, dass innerhalb des Modells auch eine Aussage getroffen werden kann, ob der angelegte Puls den integrierten Schaltkreis zerstört.

Bisherige Modellierungsansätze fokussieren sich stark auf einzelne Bauelement-Typen (z.B. Bipolar-Transistoren) und sind nicht universell einsetzbar. Der größte Nachteil bisheriger Modellierungsmethoden ist aber, dass sie auf Messungen mit dem kompletten IC basieren. Etliche Pin-Konbinationen müssen mit zahlreichen Pulslängen gemessen werden, um die nötigen Daten zu erhalten. In der Regel wünscht man sich aber bereits IC Modelle für die Systemsimulation während der Entwicklungsphase der einzelnen Komponten, um eine möglichst kurze Entwicklungszeit des gesamten Systems zu gewährleisten.

Diese Arbeit präsentiert eine neuartige Methodik, um die IC ESD Modelle aus den Entwurfsdaten des ICs abzuleiten. Basis ist eine generische Modellarchitektur, um diverse ESD Schutzelemente beschreiben zu können. Diese generische Architektur bietet den enormen Vorteil, mehrere Elemente mit einem Modell beschreiben zu können. Dadurch lassen sich komplexe Schaltungen innerhalb eines ICs auf ein einziges Modell-Element komprimieren. Auf diesem Wege entstehen sehr kompakte Modelle von kompletten ICs, welche geringen Rechenaufwand in der Systemsimulation und einen ausgesprochen guten Schutz des geistigen Eigentums des IC Herstellers ermöglichen. Anhand von zwei typischen ICs für den Automobilbereich wird gezeigt, dass diese Modelle die gewünschte Genauigkeit von ± 20 % erreichen. Das quasi-statische ESD Klemmverhalten und das transiente Verhalten in der Simulation stimmen gut mit den Messergebnissen überein. Die Zerstörgrenze des ICs wird gut nachgebildet, sowohl als einzelnes Element als auch in kleinen Systemen.

Ganz im Sinne des SEED-Ansatzes wird eine ganzheitliche Systembetrachtung mit dem Fokus ESD Festigkeit gemacht. Nicht nur die IC Modelle müssen besondere transiente Verhaltensweisen präzise nachbilden, sondern auch die Modelle der externen Bauelemente. Deshalb wird eine Methodik entwickelt, um Gleichtaktdrosseln für den ESD Bereich zu charakterisieren und zu modellieren. Dadurch lässt sich das Verhalten bei ESD Ereignissen von beispielweise Kommunikationssystemen mit Gleichtaktdrosseln präzise vorhersagen.

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List of Abbreviations

I_h .... holding current
I_{t1} .... trigger current
I_{t2} .... destruction current
R_{on} .... dynamic resistance in on-state
V_h .... holding voltage
V_{t1} .... trigger voltage
V_{t2} .... destruction voltage
A .... anode
AC .... alternating current
AEC .... automotive electronics council
AMR .... absolute maximum ratings
AMS .... analog and mixed signal
ANSI .... American National Standards Institute
ASIC .... application specific integrated circuit
B .... base (sometimes also used for bulk)
BCD .... bipolar CMOS DMOS
BOM .... bill of materials
C .... capacitance
C .... cathode
C .... collector
CAN .... controller area network
CDM .... charged device model
CMC .... common mode choke
CMOS ...... complementary MOSFET
CT-1 .... inductive current sensor of Tektronix
D .... drain
DC .... direct current
DMOS ...... double-diffused MOS
DUT .... device under test
E .... emitter
ECU .... electronic control unit
EFT .... electrical fast transient

EMC .... electromagnetic compatibility
EMI .... electromagnetic interference
EPA .... electrostatic protected area
ESD .... electrostatic discharge
ESDA .... ESD Association
EUT .... equipment under test
FEM .... finite element method
FET .... field effect transistor
G .... gate
ggNMOS .... grounded gate NMOS
GND .... ground, reference point for voltages ($V_{GND} = 0V$)
HBM .... human body model
HDL .... hardware description language
HMM .... human metal model
HV .... high voltage
i-v-curve .... plot of current versus voltage, mainly used as quasi-static plot for ESD protection devices
I/O .... input output interface of an IC
IC .... integrated circuit
IEC .... International Electrotechnical Commission
IP .... intellectual property
ISO .... International Organization for Standardization
JEDEC ..... joint electron device engineering council
JS .... joint standard
L .... inductance
LV .... low voltage
MLCC ...... multi layer ceramic capacitor
MOS .... metal oxide semiconductor
MOSFET ... metal oxide semiconductor field effect transistor
N .... number of windings
NMOS ...... n-channel MOSFET
OEM .... original equipment manufacturer
PCB .... printed circuit board
PMOS ...... p-channel MOSFET
PUT .... pin under test
R .... resistor
RC .... resistor capacitor network
RF .... radio frequency

S .... source
SCR .... silicon controlled rectifier
SEED .... system efficient ESD design
SOA .... safe operation area
SOI .... silicon on insulator
SPICE ...... simulation program with integrated circuit emphasis
TBM .... transient behavioral model
TBM-MOS . transient behavioral model for MOSFETs
TDDB ...... time dependent dielectric breakdown
TLP .... transmission line pulse (System)
TS .... technical specification
TVS .... transient voltage suppressor device
VDD .... positive supply voltage
VSS .... negative supply voltage

1 Introduction

Electrostatic discharge (ESD) is not a new threat neither in general nor for the electronics industry. Established test standards are available to verify the robustness of electronic components and systems against ESD events. However, on the system or printed circuit board (PCB) level the design for ESD robustness is still not straightforward. Several components like discrete capacitors, resistors or protection devices are combined with integrated circuits (ICs). Up to now the detailed knowledge of the behavior of these components during ESD injection is not fully available to the system designer. This makes it hard to find the right balance of components and their placements to optimize both the functional behavior as well as the ESD robustness of the system. Furthermore, the (sub-)system vendor is interested in a cost-optimized solution. Avoiding costly re-design steps as a consequence of failed ESD qualification tests as well as an over-engineering of the protection concept are goals for the system developers.
This work will introduce a modeling framework to generate ESD models of complete ICs. A black box modeling approach without physical details is chosen to reach short simulation run times. This enables simulations on PCB level while the Intellectual Property (IP) of the IC vendor is protected effectively. Finally a methodology is described to derive precise ESD behavioral models of complete ICs from their design data, which enables an automated model generation flow. Compared to a measurement-based model generation process this can reduce the effort significantly to provide ESD models of complete ICs for the system designers. In addition, these ESD models can be generated even before the silicon of the IC is available.

1.1 The challenge of designing systems robust against ESD

To design robust electronic systems, the methodologies published are summarized which enable a Co-Design of an IC and external protection elements for ESD robustness on PCB level.

It is still common practice for a large number of systems that ESD robustness design is purely based on experience and more or less done as a "trial and error" approach. Finding out during qualification tests that a (sub-)system has an ESD robustness issue is always a bad situation. First of all, it is usually very costly to improve the systems ESD robustness in such a late design stage and this might significantly delay the product launch. Furthermore, after the system is fixed in terms of bill of materials (BOM), PCB layout and functional performance, it is typically quite hard to find an optimal solution to increase the ESD robustness without

harming other system parameters. Ideally, the ESD robustness of systems is optimized already during an early system design phase when all parameters can be adjusted with comparably low effort. A simulation-based solution can provide results at low cost and early in system development phase. It has to be noted that for such simulations adequate high frequency and high current/power models of all involved components are essential. This task is not easy to fulfill as most of the components are operating outside of their regular operating conditions during ESD events and hence often the nominal models are not accurate or even not valid in this range. Moreover, the ESD pulses have very steep rise times ($t_r \approx 0.1 \ldots 1\ ns$) to very high current values ($I_{ESD} \approx 10 \ldots 40\ A$). With these high time derivatives of the current values already a small inductance value ($L \approx 1\ nH$) can create severe voltage spikes ($V_{peak} > 100\ V$) which can be very critical for electronic components.

ESD robust design means at IC level: provide dedicated current paths to safely shunt the ESD current and avoid physical destruction of the IC. For systems, the boundary conditions change at this point. System can be hit by an ESD event not only in an un-powered mode, but also in the powered up mode when the system is operating and performing the desired functionality. This changes the meaning of ESD robust design fundamentally. On system level also system upsets and unintended resets have to be avoided to guarantee the functional performance of the system, these are the so-called *soft failures.* A malfunction of the system for a short period of time (μs or ms) can be annoying in the case of a computer or phone. Within safety-critical applications inside a car, e.g. airbag control system or steering, malfunctions can lead to severe issues. Such electronic systems must be robust against destruction (hard failures) and disturbance (soft failures) caused by ESD events to a certain extent.

1.2 State of the Art

1.2.1 System efficient ESD design (SEED-approach)

The idea to enhance the ESD robustness on system level has been promoted by the Industry Council on ESD Target Levels by an approach to enable the Co-Design of discrete protection elements and the ESD protection of the IC. They called it the "System Efficient ESD Design (SEED)" approach and published the basic idea within the white paper 3 which is split in two parts [1] and [2]. Part one of the white paper creates a common understanding of the differences in ESD robustness requirements between IC and system level. The goal is to bring together system designers (OEM) and the IC vendors. A comprehensive methodology is formulated to balance the ICs ESD protection capability with discrete ESD protection devices on the PCB, the so-called SEED approach. This approach is schematically shown in figure 1.1. The Co-Design can be done by comparing the quasi-static I-V-curves of the ESD inside the IC and on the PCB. This procedure requires detailed information of the ICs behavior during pulsed stress (TLP or ESD). Usually, this information is not provided by the IC vendor due to IP

protection concerns.

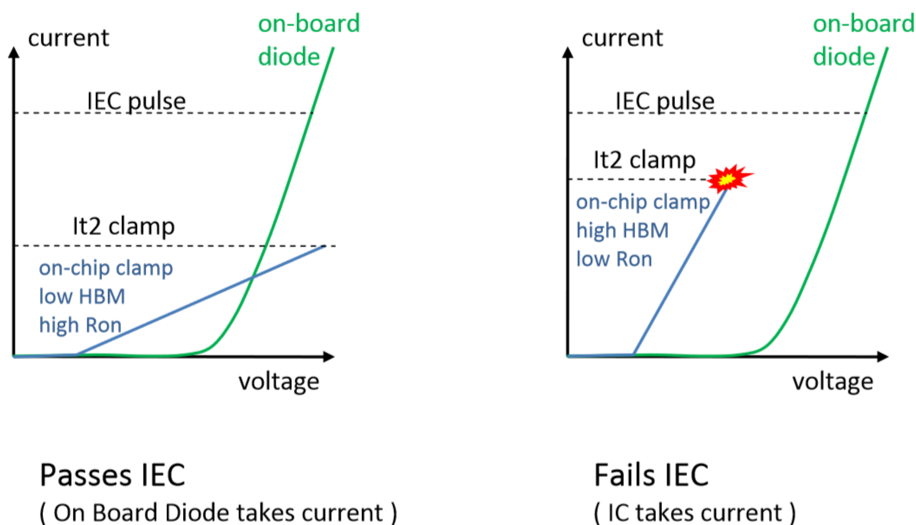


Figure 1.1: Schematic illustration of the SEED approach [1].

Part two of this white paper presents advanced methods to characterize the system response during ESD injection. Using these methods, the weak points during ESD events can be found and made more robust. The focus is set on simulation data to assess the system response against ESD pulses and to detect possible weak points in the system. Additionally, the future development trends are discussed in a common roadmap. Especially emphasized is again that the task of building robust systems needs good communication and an efficient way of working of the involved parties together along the supply chain.

1.2.2 Modeling methodologies for ESD simulations

Since the publication of the SEED approach in 2010 [1] respectively 2012 [2] activities are ongoing to construct IC models for system ESD simulations. At the beginning, nearly all approaches where focusing on the quasi-static behavior of the ESD protection devices, see publications of Lou et.al. [3] or Arndt et.al. [4] respectively Scheier et.al. [5]. The quasi-static characteristic gained by 100 ns TLP measurement reproduces the typical clamping behavior under ESD stress, mainly HBM ESD tests and partly the second peak of the system ESD (HMM) test pulse. It is understood that also the turn-on behavior of ESD protection devices, both as discrete devices and within ICs, can play a major role in the current distribution within the system and hence the point of the physical failure. Table 1.1 summarizes several published modeling methodologies with their capabilities and gaps.

Table 1.1: Comparison of different modeling approaches for complete ICs enabling SEED simulations of (sub-)systems

Feature	Lou et.al. [3]	Escudie et.al. [6]	Scheier et.al. [5]	Cao et.al. [7]	this work [8], [9]
quasi-static behavior (i-v-curve)	✓	✓	✓	✓	✓
SPICE (preferred by system designers)	✓	✓			✓
Verilog-A(MS)/ VHDL-AMS		✓	✓	✓	(✓)
transient effects				✓	✓
static failure model	✓	✓	(✓)	(✓)	(✓)
dynamic failure model			✓	✓	✓
generic architecture (applicable for various protection devices)			(✓)	(✓)	✓
based on IC measurements	✓	✓	✓	✓	(✓)
based on IC design data					✓

1.3 Purpose of this work

The motivation of this work is the development of a methodology to generate IC models for the robustness assessment of electronic systems. These models should also cover stress pulses in the ns to μs range. The basic idea is shown in figure 1.2. The IC model shall be capable of providing the response to the residual pulse in terms of voltage drop and current drain. Additionally, feedback is essential if this stress pulse can be survived or not. Providing this information without disclosing the IP of the IC vendor is key to make this approach widely usable. The goal of this work is to provide pro-actively IC models which are able to replicate the transient behavior in terms of current drain and voltage drop as well as the destruction limit for certain stress pulses.

A certain part of the single pulses needs to be dissipated by the IC itself. This is especially true for ICs manufactured in so-called smart power technologies. These ICs are typically capable of drawing at least several hundreds of mA or even a few A. Furthermore, the voltage classes of these ICs go up to 100 V. Which part of the stress pulse is coming to the IC strongly depends

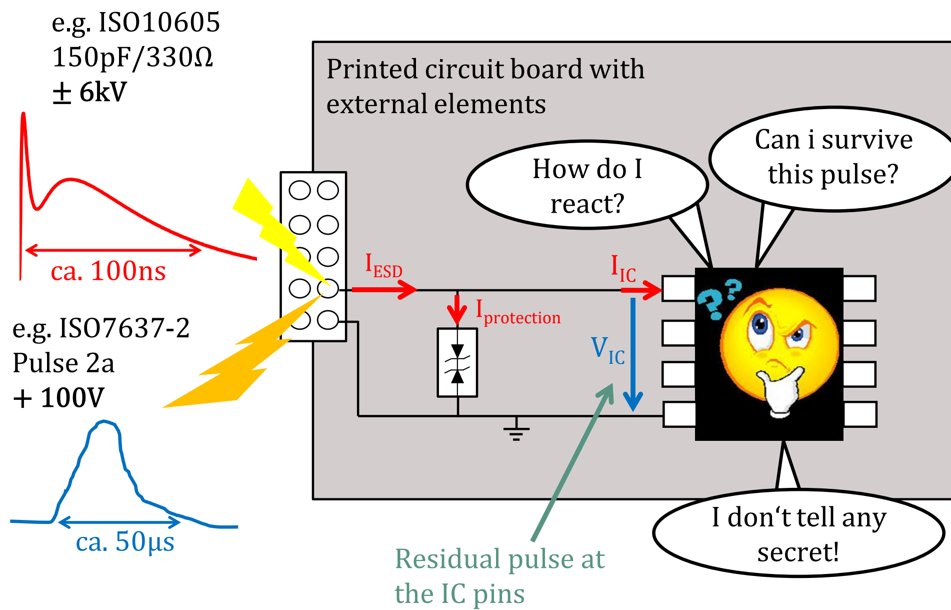


Figure 1.2: Schematic illustration of the proposed simulation approach to design robust systems.

on the additional circuitry on the PCB. During board design an optimization of protection elements on the PCB and the protection capability of the IC itself is easily possible. Later in the system design phase changes need significantly more efforts, both in terms of resources and cost. Up to now there are a few methodologies published to make IC models for certain stress pulses (mainly ESD) from measurement data with the complete IC, c.f. table 1.1.

A methodology to generate IC models out of the IC design data (schematic and layout) for a broad variety of test pulses is desired. One tremendous benefit of a design data based solution is definitely the saving of resource-intense measurement activities with the complete IC. Furthermore, the IC models can be generated even before the silicon is processed and the proposed model architecture can be implemented in various modeling languages. The main focus of this thesis is set on design for robustness against ESD events on system level. In addition, the proposed methodology is capable of building IC models for a broad range of stress pulses when the necessary data is available.

2 Introduction to ESD and protection strategies for electronic systems

A short summary of the electrostatic discharge (ESD) phenomenon and the related test standards on component (IC) level are provided in this chapter. Additionally, pulsed stress tests on system level are mentioned. The scope of this work is to develop a modeling methodology for complete ICs to enable simulations for system level robustness during disturbance pulses like ESD or load dump. The relevant stress pulses are briefly discussed.

2.1 Electrostatic discharge (ESD)

ESD is a well known phenomenon within the electronics industry. The destructive power of ESD events is known since decades within the semiconductor industry. Several qualification tests have been established to ensure that semiconductor products survive the manufacturing processes within electrostatic protected areas (EPAs). Electrostatic charging is happening when two materials with a different electrochemical potential are brought into contact. Then same charge is transferred slowly from one material to the other to compensate the difference in electric potential. When both materials are separated again rapidly this charge shifting stays. And hence one material is building up positive charge while the second one charges up negatively, if both are isolated from charge reservoirs (e.g. earth). This process is cumulative, i.e. the charge built up is done each time the materials are brought in contact and separated rapidly again. To ensure, that electronic devices survive the discharge of a human through the device into the ground, the human body model (HBM) test was developed, see section 2.3.1. Measurements have shown that humans typically do not charge to voltages higher than $\approx 100\ V\ to\ 500\ V$ within EPAs [10]. Therefore ICs are typically qualified with 1 kV or 2 kV according to the HBM standard [11] to have some safety margin. During automated handling processes often the ICs itself are charged and rapidly discharged when they are placed on a conductive surface (e.g. metallic table). To ensure that the ICs survive a certain stress level the charged device model (CDM) test was established (section 2.3.2). When electronic components or systems are handled outside EPAs the ESD stress can be significantly higher, because humans can charge up to higher voltage levels (e.g. 10 kV or even higher). Depending on the involved materials and the air humidity the theoretical maximum charging voltage is $30\ -\ 35\ kV$ [12], which is reached only very seldom. In addition the humans can carry metallic tools in their

hands and discharge through them into the DUT. To ensure a certain robustness of electronic system in this environment the so called human metal model (HMM) test was developed, see section 2.3.3. Furthermore, the standard characterization tool for ESD protection devices and concepts, the so called transmission pulse (TLP) test is described in section 2.3.4.

2.2 ESD window and ESD protection concepts

As ESD pulses are a threat for ICs can not be avoided completely, each and every device needs a certain robustness against ESD. The HBM ESD tester acts in first approximation as a current source, therefore the IC needs to provide a safe current path to shunt the ESD current at a safe voltage drop to the reference pin. In principle an ESD protection shall be high-ohmic in the operating voltage range and low-ohmic above this range. The target is to conduct a certain ESD current at a safe voltage drop to protect all sensitive devices of the IC. Furthermore, the protection device shall not disturb the normal operation. Additionally, a low leakage current is desired to reduce energy consumption especially in battery powered systems.

2.2.1 ESD protection window

The lower voltage border for the ESD protection elements is the maximum operating voltage $V_{max,op} < V_{min,ESD}$. Below that border they shall ideally be invisible, i.e. the protection devices shall have a high impedance to prevent leakage currents and a low capacitance to not distort communication signals. On the other hand the upper voltage border is defined by the maximum voltage $V_{max,ESD} < V_{destruction}$ drop the *element(s) to be protected* can withstand. In between these two voltage borders there is the so called *ESD protection window*, see figure 2.1. Within this window the ESD protection element needs to shunt the ESD current I_{ESD} which is determined by the desired ESD test level. The turn-on voltage $V_{trigger}$ and the dynamic resistance of the ESD protection device R_{on} determine the voltage drop V_{ESD} at the demanded current level I_{ESD}, e.g. 1.33 A for 2 kV of HBM robustness.

Depending on the needed ESD withstand level and the ESD window itself the ESD protection device needs a certain size to safely shunt the ESD current. The outlined quasi-static I-V-curve of figure 2.1 shows the behavior of breakdown diodes (zener or avalanche breakdown) or statically triggered active clamps. Furthermore, there are devices showing a so called snap-back behavior. This means they reduce the voltage drop above a certain trigger current $I_{t,1}$ (see figure 2.3 for instance). This allows to use small ESD design windows more efficiently.

2.2.2 ESD protection devices

To fulfill the tasks of an ESD protection element there are several device types. The most simple ESD protection device is a diode in forward conduction mode. These devices are generally used to guide the ESD current into a certain direction, e.g. towards dedicated, central ESD

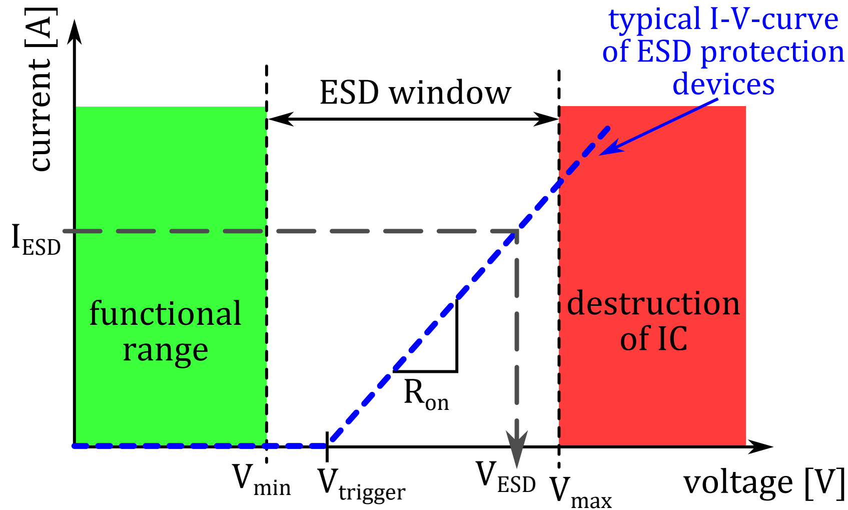


Figure 2.1: Schematic illustration of the ESD protection window.

clamps. For low-voltage protection concepts below ≈ 0.5 V supply voltage, also stacking of forward diodes is possible to use them for higher voltage classes or reduce the leakage current. As semiconductor technologies contain quite a number of pn-junctions these devices can be built easily. The most common devices used for ESD protection are shown schematically in figure 2.2.

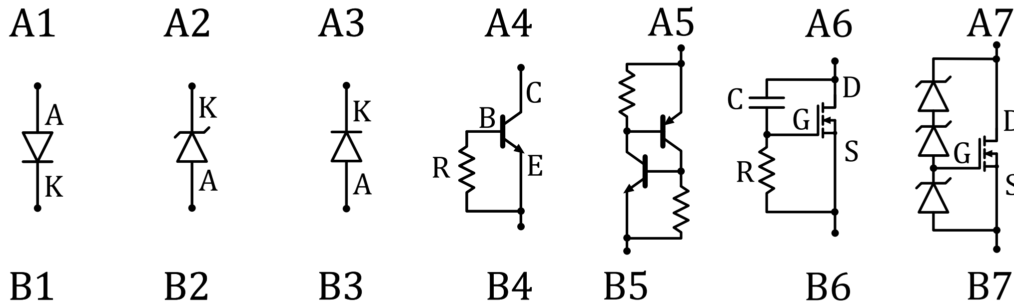


Figure 2.2: Schematic illustration of typical ESD protection devices which provide ESD protection from A to B respectively. The numbers from one to six specify the device type: 1: forward diode, 2: zener diode, 3: avalanche breakdown diode, 4: bipolar transistor, 5: thyristor, 6: RC-triggered active clamp and 7: statically triggered active clamp.

Also very common for ESD protection are bipolar based protection structures like NPN/PNP-transistors (number 4 in figure 2.2) or thyristors (silicon controlled rectifier SCR) (number 5). They offer the advantage of a so called snap-back behavior, i.e. after the activation at a certain trigger voltage/current they reduce the voltage drop (see figure 2.3). This has two main advantages: Firstly, the voltage drop at a certain current level is reduced which enables a better protection of core devices due to the comparably small voltage drop during ESD events. Second,

the reduced voltage at a certain current level reduces also the dissipated power which enables higher current levels to be shunted before the device itself is thermally destroyed. As snap-back based solutions have the risk of unintended triggering during normal operation, which can lead to destruction, there are also ESD devices without snap-back characteristic. These devices are usually diodes in reverse polarization, e.g. avalanche or zener breakdown (number 2 respectively 3 in figure 2.2).

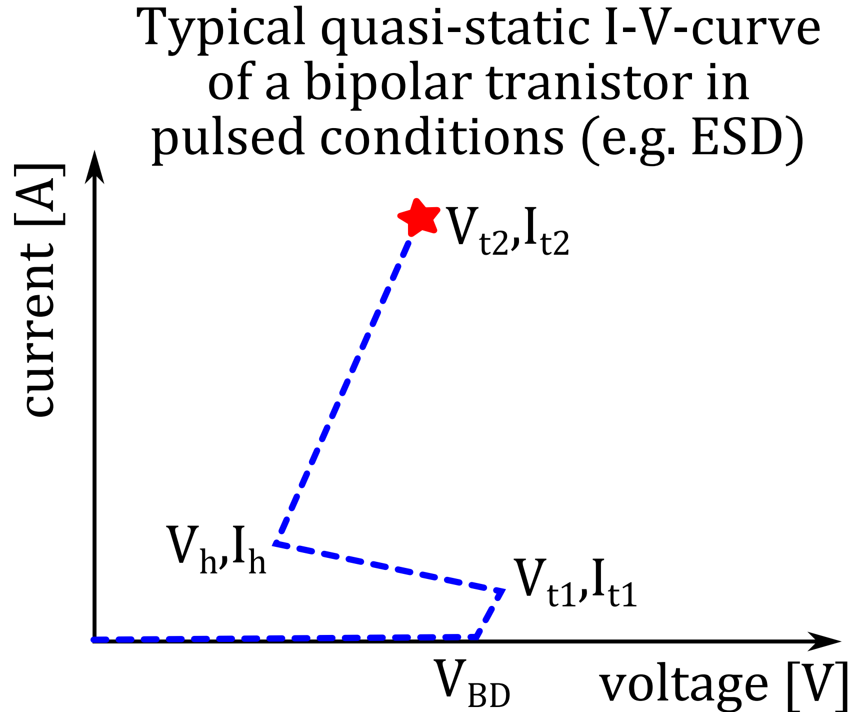


Figure 2.3: Schematic illustration of the current over voltage characteristic (I-V-curve) of a bipolar transistor in pulsed conditions showing the typical snap-back behavior.

The described elements are all single devices itself. Another type of ESD protection elements are the so called active clamps (dynamically or statically triggered, number 6 respectively 7 in figure 2.2). These clamps usually contain a big MOS transistor, which conducts the ESD current and a gate controlling circuit to activate the MOS transistor in case of ESD. So they are a small protection circuits rather than single devices. The controlling circuit can be statically activated above a certain voltage threshold with devices that have a fixed breakdown voltage. For example a stack of zener diodes can be used to activate the big MOS transistor like depicted in figure 2.2 under number 7. This active clamp is turned on for voltages above the breakdown voltage of the zener diode chain. By contrast the RC-MOS clamp of number 6 is activated for pulses with a fast rising edge and deactivated after a certain time $\tau = R \cdot C$.

2.2.3 ESD protection on IC level

With the beforehand described ESD protection elements for each pin of an IC an appropriate protection concept can be developed. Boundary conditions are the operating voltage range, the voltage capability of all sensitive devices and the demanded ESD withstand level of a certain test standard. For each pin-combination there needs to be a dedicated current path in case of ESD pulses. The goal is to protect the functional circuit inside the IC during ESD events. The beforehand described ESD protection elements are used to provide for each pin-combination an intended ESD current path. An example is a central ESD clamp for several I/O-pins versus ground, for example figure 2.4. Each I/O-pin has two diodes to forward the ESD current towards the ESD rails, in this example *VDD* and *VSS*. Between these two ESD rails or buses there is one centralized ESD clamp to shunt the current from *VDD* to *VSS*. Each pin combination of this example has a dedicated current path for ESD pulses of both polarities and hence the IC can be successfully protected against ESD events. By contrast for I/O-pins with different voltage classes often a dedicated ESD protection device for each pin versus ground is used. As both polarities needs to be protected typically the forward diode mode of diode or MOSFET based elements is used for negative polarity protection.

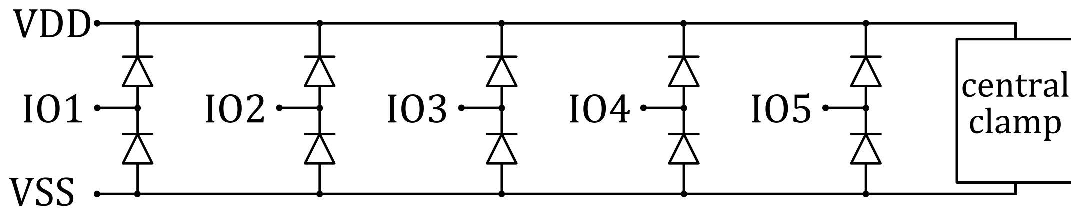


Figure 2.4: ESD protection concept of several I/O-pins with the same operating voltage range portected by a central clamp between VDD and VSS.

The size of each ESD protection element is determined by the target ESD test level and the maximum voltage drop the functional circuit of the IC can withstand, cf. figure 2.1. Depending on the functional circuit and especially the size of the single devices part of the ESD current can be shunted by the functional devices themselves. This enables size reduction of the respective ESD protection element. In some cases the functional device like big output drivers are able to sustain the complete ESD current. In this case the functional devices are called self-protecting. As a consequence no further ESD protection device is needed which results in an optimized area consumption of the IC.

2.2.4 ESD protection on system level

Not only single ICs need a protection against ESD events, but also systems and sub-systems. Within this work every combination of one or more ICs and discrete components is denoted as system. These systems can have different complexity levels and expansion stages. For this work it is not necessary to distinguish between PCB with mounted components and complete

systems incorporating enclosures and housings. When speaking of system level ESD typically the ESD robustness of PCBs with mounted devices is meant. The ESD protection on system or PCB level is usually a combination of components which are there for functionality and dedicated protection devices against disturbance pulses. This means also the IC can be part of the system's ESD protection depending on its ESD capabilities. Furthermore, RC filters for low-pass filtering of signals can shunt part of the ESD current to ground. Also filtering components to improve the electromagnetic interference (EMI) behavior can be part of the ESD protection concept. A typical example are capacitors to reduce electromagnetic emissions or immunity of circuits. Besides their EMI improvements they are able to shunt some part of the ESD current and protect more vulnerable parts like ICs.

If these already existing components are not enough to provide the demanded ESD robustness levels, dedicated protection devices have to be placed in addition. Examples are varistors, conductive polymers or transient voltage suppressor (TVS) devices. They behave comparably to ESD protection elements within ICs. The most commonly used device types are silicon based TVS devices. Usually they are called TVS diodes, although they are often bipolar based protection devices with snap-back behavior.

On IC level the only concern regarding ESD is the destruction of the IC during manufacturing processes. On system level there can be ESD threats also during operation at the final customer. This means two things. First of all, the ESD pulses on system levels are higher compared to IC level, because the end customer is typically handling the electronic systems not within EPAs. This means the humans or devices can charge to quite high levels (e.g. $8 - 15\ kV$). Secondly, there is not only the risk of physical damages, but also the risk of system upsets or resets. Depending on the application and especially the relevance of undisturbed functionality the second one can be also a quite severe problem. For example when a phone is disturbed by an ESD pulse and does not react on a user interaction, it is irritating but not a severe issue which can be usually solved by a reset of sub-system. By contrast when an airbag system within a car is disturbed by an ESD event and does not activate the airbag during a crash, this can mean severe injuries for the occupants. Even worse can be a situation when the car is driving on a highway and the airbags are activated without any crash but accidentally by an ESD event. These examples show that the ESD robustness of systems is a serious task for system designers. Therefore the ESD robustness needs to be approved by final qualification tests. Even better would be to actively develop the ESD robustness already during the development of functional features.

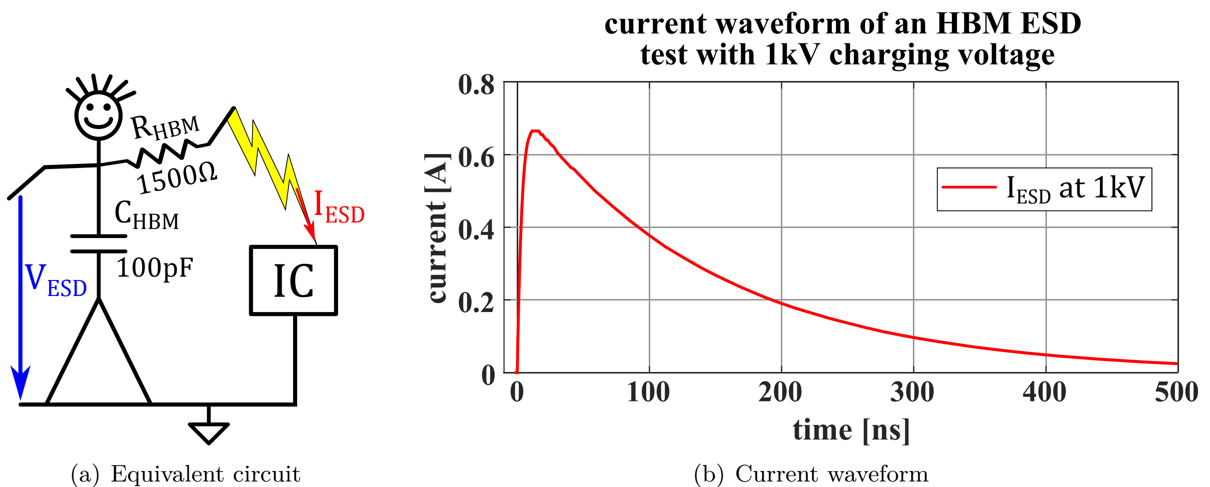
The same as for IC level ESD protection applies here: Finally the component's or system's ESD robustness needs to be proven by standardized qualification tests. These tests are described in the following section in detail, both for IC level and system level. In addition, there are further standards presented which define robustness test of electronic systems against pulsed disturbances different to ESD events.

2.3 ESD test standards

To ensure that electronic devices and systems have a certain robustness against ESD events there are several test standards. They are intended to assure that electronic devices and systems can withstand the ESD threats which they typically face during manufacturing and operating conditions. This section presents the most relevant ESD test standards for ICs and electronic systems. There is the possibility that human persons get charged electrostatically. If a discharge happens through the device or system there is the risk that certain parts of the device or system are destroyed. On IC level there is the so called human body model (HBM) ESD test defined in ANSI/ESDA/JEDEC JS-001-2017 [11]. In addition, the device itself can be charged electrostatically and rapidly discharged when an electrically conducting surface is approached. To ensure the necessary robustness against this kind of ESD event the charged device model (CDM) is defined in ANSI/ESDA/JEDEC JS-002-2014 [13]. During these tests the IC is charged capacitively to the demanded test level and rapidly discharged via a low ohmic resistor, typically 1 Ω. Furthermore, on system level in operating conditions the system can be disturbed which can result in malfunction or system resets. To ensure that these system upsets do not disturb the operation of the system, there are the test standards IEC 61000-4-2 [14] and ISO10605 [15].

2.3.1 IC level HBM - ANSI/ESDA/JEDEC JS-001-2017

Also within EPAs the electrostatic charging cannot be eliminated completely, but it can be reduced significantly. With state of the art techniques the charging of humans can be limited to voltages typically below $100 - 200\ V$ within electrostatic protected areas [10]. Therefore, the demanded ESD withstand levels for ICs are usually in the range from $500\ V$ to $2\ kV$ for the HBM ESD test [10].



(a) Equivalent circuit

(b) Current waveform

Figure 2.5: Schematic equivalent circuit and current waveform of an HBM ESD tester.

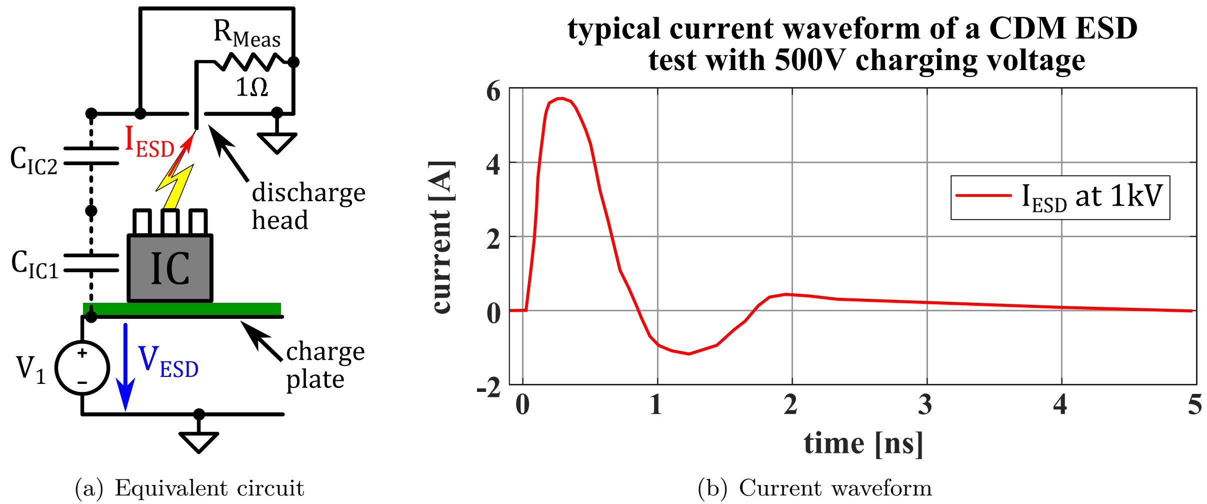
The capacitance of an average human body is modeled with a capacitor of 100 nF with respect to ground potential. This capacitor is charged to the ESD test voltage and discharged via a 1.5 $k\Omega$ resistor into the device under test (DUT) which models the discharge of a human through the skin [11]. The resulting equivalent circuit of an HBM ESD tester is presented in figure 2.5(a).

As this equivalent circuit is in first approximation a current source with an exponential decaying waveform for the low-ohmic IC, a target ESD voltage translates into a current peak value with a certain energy. The time constant τ can be calculated as follows: $\tau = R \cdot C = 1500\ \Omega \cdot 100 \cdot 10^{-12}\ F = 150 \cdot 10^{-9}\ s = 150\ ns$. The resulting peak current level is $0.67A$ per $1kV$ charging voltage. This current value is the basis to design ESD concepts for HBM protection. The ESD protection devices must be able to withstand this peak current value as well as the energy of the complete HBM pulse. Equally the IC core must sustain the voltage drop over the protection device at this peak current value. The typical destruction modes during HBM testing are thermally induced junction burnouts due to the high power dissipation. Also the triggering and destruction of parasitic devices within the silicon chip are a common failure mechanism during HBM testing.

2.3.2 IC level CDM - ANSI/ESDA/JEDEC JS-002-2014

During the manufacturing processes there is also the risk that the IC itself is charged up. This charging can be caused by automated handling tools like conveyor belts or pick and place machines. In addition, the ICs can be charged indirectly by charged objects which are placed nearby. When a charged IC is for example placed on a conductive surface like a table or a PCB, then the IC is rapidly discharged via a low ohmic path. These conductive surfaces can either be grounded directly or can have a quite high capacitance with respect to ground. In both cases the charge is equalized via nearly a short circuit and hence the discharge current is very short, has a high amplitude and a very steep rising edge. The duration of this discharge is typically in the range of a few nanoseconds with a risetime in the range of $\approx 100\ ps$, which strongly depends on the DUT itself. The peak current value depends on the amount of charge which was stored within the IC. This strongly depends on the geometrical size of the IC itself. The bigger the area of the silicon die is, the higher is the capacitance and hence the amount of charge at a certain voltage level.

To proof the robustness of an IC against this type of ESD events the ANSI/ESDA/JEDEC JS-002-2014 [13] is typically used. Dealing with charging and discharging of devices this standard is known as charged device model (CDM) ESD test. The test specifies an apparatus with a huge, metallic coupling plate which is charged to the test voltage and a discharge head to rapidly discharge the DUT. The measurement setup for CDM ESD tests is shown schematically in figure 2.6. In between both plates the IC is placed and charged capacitively by the charge plate. The capacitance between the charge plate and the IC C_{IC1} is mainly determined by the



(a) Equivalent circuit

(b) Current waveform

Figure 2.6: Schematic equivalent circuit and typical current waveform of an CDM ESD test.

area of the silicon chip and the thickness of the IC package. The second parasitic capacitance is from the IC to the grounded part of the discharge head C_{IC2}. Both capacitances are rather small ($< 1\ nF$) but the relation is usually $C_{IC1} >> C_{IC2}$. Due to this capacitive voltage divider the IC is charged to a voltage level close to the ESD test voltage with respect to ground. The DUT is charged to the desired test level, the discharge head approaches the pin under test (PUT) until the IC is discharged rapidly. To monitor the current waveform and especially the peak value a 1 Ω resistor is added into the path between PUT and ground. One exemplary waveform of an CDM discharge is plotted in figure 2.6(b). The discharge current is quite short (in the range of 1 ns) and has a steep rise time (typically ≈ 100 ps) up to several amperes. These very short but steep pulses mainly cause oxide breakdowns due to excessive voltage drops within the IC. In some cases also junction burnouts are reported at CDM testing.

2.3.3 System level HMM - ISO10605 and IEC 61000-4-2

All IC level ESD tests assume that the ICs are handled in EPAs and hence the charging voltages are limited to moderate levels. By contrast, the end products at the customer are no longer handled within EPAs. Therefore, the charging voltages of humans can be significantly higher than 2 kV. In addition there is the possibility that a charged human is approaching the electronic system with a metallic tool in his hand. This can be a car mechanic holding a screwdriver in a garage when a car gets repaired. The same situation can occur when a computer or mobile phone gets repaired and a screwdriver is needed to open the housing. This causes a different waveform of the discharge current which is defined in the so called human metal model (HMM). Generally, for electronic systems the HMM ESD test is defined in IEC 61000-4-2 [14]. This standard applies for all electronic products in general while for automotive systems and sub-systems there is the ISO10605 [15]. The IEC 61000-4-2 specifies a discharge

network of $R = 330\ \Omega$ and $C = 150\ pF$. Compared to HBM the energy content is 50 % higher due to the higher capacitance. Furthermore, the discharge resistance is significantly lower than in the HBM definition. As a consequence, the discharge current is higher ($2\ A/kV$), but the time constant of the pulse is shorter ($\tau = 49.5\ ns$). Additionally, there is a very short initial pulse ($\approx 2\ ns$) with a quite high amplitude ($3.75\ A/kV$). This is the discharge of the metallic tool via nearly no resistance into the DUT. As a result the discharge current waveform is constituted of two pulses, one short initial peak to high amplitude values and a second broader peak to a moderate amplitude level. The superposition of both gives the current waveform specified in IEC 61000-4-2 [14]. For automotive applications there is also the possibility that the human is sitting inside the car and hence has a higher capacitance with respect to ground compared to a human standing next to a car. Therefore, the ISO10605 specifies two capacitance values for the network of the ESD generator ($150\ pF$ and $330\ pF$). In addition, there are two discharge resistances defined ($330\ \Omega$ and $2\ k\Omega$). All combinations of R and C are allowed according to the standard and result in different waveforms of the discharge current. Although the second peak of the ESD pulse is strongly influenced by the R and C values, the first peak is not influenced at all by these values. The first peak represents the discharge of the metallic tool and is created by the discharge tip of the ESD generator. It is not related to the capacitance and resistance of the human body respectively the discharge network of the ESD generator.

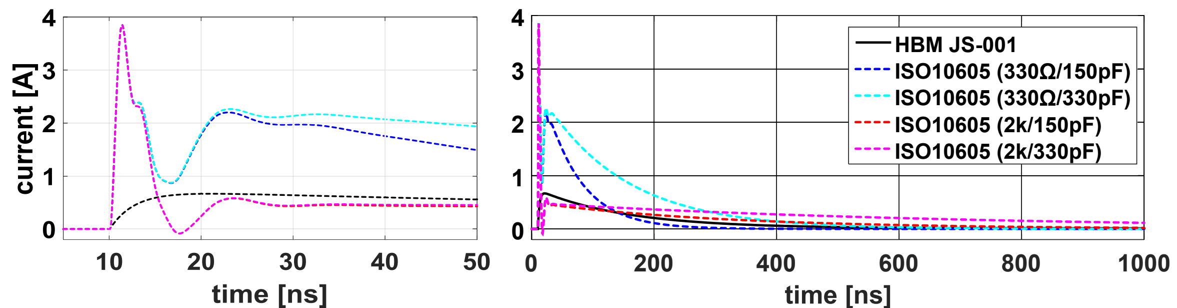


Figure 2.7: Comparison of discharge currents of a HBM (ANSI/ESDA/JEDEC JS-001) and the different System ESD discharge networks (ISO10605) at 1kV ESD voltage.

The IEC 61000-4-2 and the ISO10605 specify the rise time of the ESD pulse ($0.6 - 1\ ns$), the first current peak ($3.75\ A/kV\ \pm\ 20\ \%$) and the current values at $t_1 = 30\ ns$ ($2\ A/kV \pm 20\ \%$) respectively $t_2 = 60\ ns$ ($1\ A/kV\ \pm\ 20 + \%$). Different values (time and current amplitude) are specified in ISO10605 for discharge networks other than $R = 330\ \Omega$ and $C = 150\ pF$. The time constants for the different networks range from $\tau = 49.5ns$ for $R = 330\ \Omega$ and $C = 150\ pF$ up to $\tau = 660\ ns$ for $R = 2\ k\Omega$ and $C = 330\ pF$. The current waveforms of discharges from $1\ kV$ ESD voltage with the different discharge networks defined in the ISO10605 are shown in figure 2.7 and compared to the HBM waveform of ANSI/ESDA/JEDEC JS-001. This variety of pulses coming to the IC pins is getting even broader when external components, e.g. capacitors or

inductors, are used within systems. As a consequence, the complete ESD test setup, consisting of ESD generator, PCB schematic, PCB layout, ICs and grounding concept during the test, can influence the result significantly. Hence, system simulations to find the root cause of failed tests or design for a certain robustness during system design phase are inevitable. Needless to say that adequate models of each component for ESD events (high current respectively voltage levels and short pulse durations) are crucial to get accurate results. On system level there is not only the challenge of physical destruction, but also the concern of disturbances within the system due to ESD events. Depending on the type of application, an ESD induced soft failure can cause severe damage to persons or systems, e.g. electrical power steering or airbag system of a car. This is the reason why there are also ESD tests in powered conditions on system level. These soft failures can be system hangup, unintended resets or wrong output signals due to corrupted communication data. The typical test levels range from 2 kV up to 15 kV or even 25 kV, for tests in unpowered conditions as well as tests during normal operation.

Sometimes there is no hard ground connection between equipment under test (EUT) and the tester ground. Therefore, the electronic components are not always stressed with a high power pulse, but more often with electromagnetic disturbance pulses. Usually real world ESD events at these high voltage levels are air discharges with an ionization of the air gap before the two electrodes make contact.

2.3.4 IC level characterization method TLP - IEC 62615

In the middle of the 1980s transmission line pulse (TLP) measurements were established for ESD characterization of devices and circuits [16]. TLP has the big advantage of precise measurement possibilities of current and voltage values during the pulse compared to HBM tests. It is known, that the failure current of thermal induced failures correlates very well from HBM peak current to 100ns rectangular pulses. The TLP system delivers a highly reproducible pulse of rectangular waveform and constant power.

Therefore, it has been the standard characterization method for the ESD properties of semiconductor devices and circuits since the 1990s. To make TLP measurement results comparable, an international standard was published [17]. Details on the measurement procedure with TLP and the resulting quasi-static i-v-characteristic are explained in section 7.1.

2.4 Test standards of automotive transient disturbances/electrical fast transients

For systems and sub-systems ESD pulses are not the only threat which can cause malfunction or destruction. There are some more pulses which are in the range of ns up to μs or even ms which can be caused by the system itself, e.g. inductive voltage spikes due to load dump. The most relevant pulses are briefly described in the following subsections.

2.4.1 ISO7637-2 Electrical transient conduction along supply lines only

In general, cars are quite complex systems with a lot of sub-systems or modules combined together. These modules are distributed all over the car and hence long and complex wiring harnesses are needed to connect all of them together. This circumstance requires quite a lot of communication lines and as well as many power supply lines as the car has typically a centralized power supply. The generator combined with a battery is usually placed close to the engine and coupled mechanically to convert kinetic energy into electric energy. A lot of connectors are used to connect the power supply wires to the modules. These connectors can open the contacts unintended and close them again within very short time periods due to vibrations of the car. Although the mechanical design of the connectors is done in a way to avoid these connection interruptions, they cannot be prevented under all conditions. When the current flow into a module is suddenly interrupted the inductance of the wiring harness further pushes the current towards this open connection and the voltage rises. This inductive voltage spike due to a load dump can be a danger for other modules connected to this power supply line. Furthermore, the switching of inductive loads can create such voltage spikes on the supply line. To ensure a certain robustness of the single modules against such kind of fast transients on power supply lines, the ISO7637-2 [18], containing the definitions of several pulses and respective test procedures, is frequently used for automotive sub-systems. Both failure categories, soft and hard, are evaluated during and after the tests. As example, waveform of pulse 2a, defined in the ISO7637-2, with an amplitude of 100 V and a supply voltage of 13.5 V on a 10 $k\Omega$ load is shown in figure 2.8.

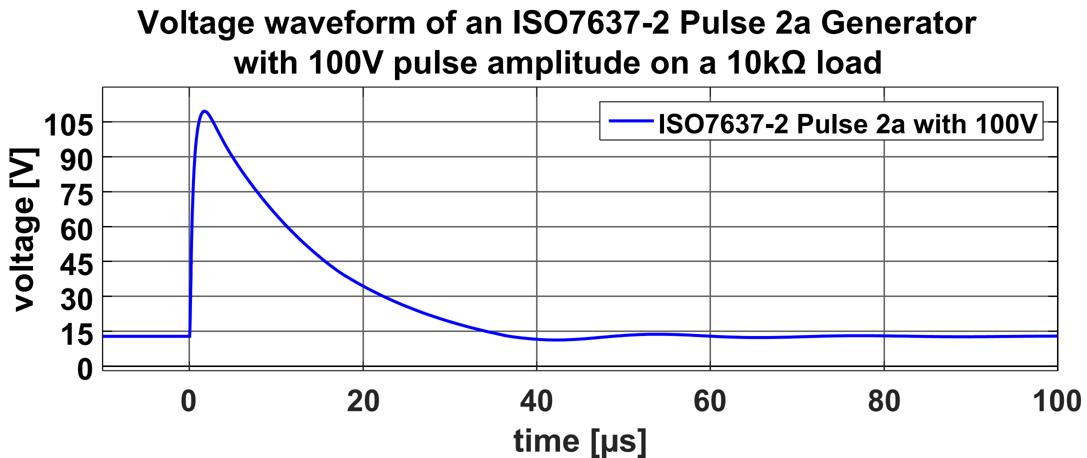


Figure 2.8: Pulse waveform of an ISO7637-2 Pulse 2a with 100 V pulse amplitude and 13.5 V DC supply voltage on a 10 $k\Omega$ load.

As the specified pulses are in a time domain which is close to the ESD time domain, ideally one IC model is valid for all these pulsed threats. Optimally the IC model reflects the transient behavior, in terms of current drain and voltage drop, during the injection of the different

stress pulses with an acceptable accuracy. Typically ± 20 % is accepted by system designers. Furthermore, the indication of the physical failure level with the same accuracy would be highly appreciated.

2.4.2 ISO7637-3 Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines

According to the beforehand described transient on supply lines there can be pulses on lines other than supply lines within the wiring harness. The ISO7637-3 [19] defines test pulses and measurement procedures to test the robustness of automotive modules against these kind of pulses. The transients can be coupled capacitive, inductive or directly on the lines which are tested. The defined pulses are similar to these of ISO7637-2 solely the tested lines and the coupling differs. The main goal is to prove that the system is not disturbed by these pulses. Although the physical destruction of an IC during these tests is possible and shall be predictable by system simulations.

2.4.3 IEC 61000-4-4 Electrical fast transient/burst immunity test

The beforehand described test standards of the ISO7637 family are made for systems and sub-systems which go into cars. There are a lot more fields of application besides the automotive applications. For example mobile phones, computer or other consumer electronic products are one major field of application. Furthermore, electronic systems for industrial applications are another example for the usage of electronic devices. For general electronic equipments and systems the IEC 61000-4 family provides definitions of test pulses and measurement instructions to verify the robustness of electronic equipment against stress pulses. The IEC 61000-4-4 [20] specifies procedures to validate the robustness of electronic systems against repetitive electrical fast transients (EFTs) and burst pulses. The disturbance pulses shall be directly applied to power supply terminals, comparably to the ISO 7637-2 definition. Signal - or more generally spoken - non-supply terminals shall be stressed via a capacitive coupling clamp comparable to the ISO 7637-3 test standard. Again the thresholds for system failures and physical destruction are the main points of interest for system designers. The voltage waveform of the burst pulse defined in the IEC 61000-4-4 on a 50 Ω load and a test level of 2 kV is plotted in figure 2.9.

2.4.4 IEC 61000-4-5 Surge immunity test

Going to higher power levels and longer duration of the stress pulses, one comes to the IEC 61000-4-5 [21]. This standard defines the measurement setup, procedure and typical stress levels to prove the immunity of electrical and electronic equipment against surge pulses. These surge pulses can be originated by switching or lightning transients. They focus on power supply systems and the related stress pulses which can be generated by switching of big loads within

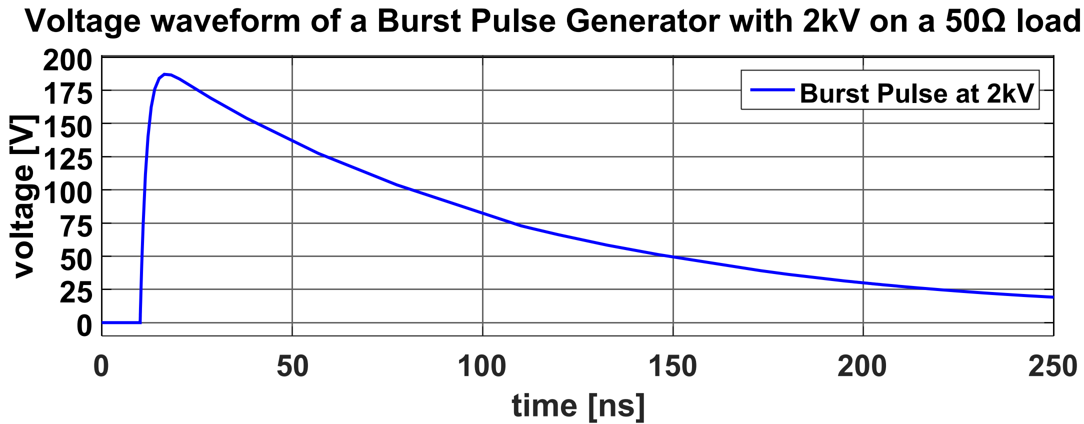


Figure 2.9: Pulse waveform of an IEC 61000-4-4 Burst Pulse with 2 kV pulse amplitude on a 50 Ω load.

the power supply grid or by a lightning strike directly into lines of the power grid. These pulses appear at the main power supply lines of electrical and electronic equipment. For systems without these connections, like traditional cars, this test standard is not applicable. The generator shall be verified in open load and short circuit conditions. The typical current waveform into a short circuit with 1 kV test level is shown in figure 2.10. However, within the automotive industry, electrical drive trains gain more and more importance, either in combination with classical combustion engines (hybrid cars) or as the main drive-train (electrical cars). As a result, the test standard also gets more and more important within the automotive industry.

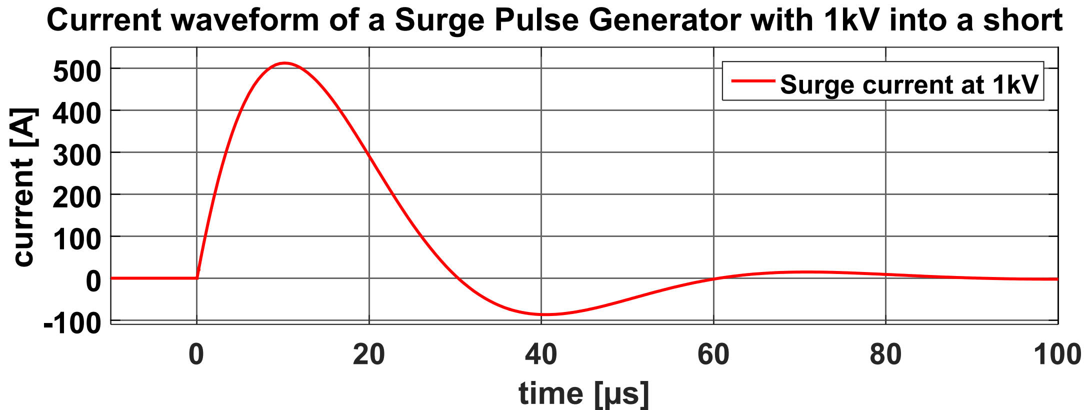


Figure 2.10: Pulse waveform of an IEC 61000-4-5 Surge Pulse with 1 kV pulse amplitude into a short circuit.

Summary

This section presented a brief summary of the ESD phenomenon and the relevant ESD test standards for ICs and electronic systems. Additionally, some further stress pulses and the

corresponding test standards were introduced. The basics of ESD protection design on IC and system level were presented. For ESD events always a safe current path is needed to shunt the incoming ESD current without physical damage within ICs or systems. The further presented pulses have an origin different than ESD, but if current is forced into the IC mainly the ESD protection devices shunt the current to protect the vulnerable parts like the core.

Since the goal of this work is to develop a methodology to model the transient behavior including destruction limits of ICs under various stress pulse conditions, this section is needed to provide a comprehensive overview on the manifold stress. The background why they exist and why they are standardized as qualification tests is explained. The standardized tests are needed to ensure that all the components within a car can survive the quite harsh electrical conditions during operation. Adequate models of all single components are needed to understand the system response to the defined stress pulses, when qualification tests failed or to design a certain system robustness already during design phase. How a generic model of complete ICs for such system simulations can look like, is presented in chapters 5 and 6.

3 Physical destruction mechanisms of semiconductor devices

The main concern of semiconductor manufacturers regarding ESD pulses is the physical destruction of the IC. Due to high currents and voltage drops destructive processes can be initiated within the IC during ESD stress. There are different physical mechanisms which lead to a physical destruction.

The first group can be called thermal failure because the destruction process is started when a certain critical temperature is reached due to joule heating. These type of failures are often called Wunsch-Bell failures as D.C. Wunsch and R.R. Bell described this failure mode as one of the first for semiconductor devices [22]. They investigated for semiconductor devices the relation between power-to-failure and pulse length for rectangular pulses. They found a relation between pulse length and power-to-failure for discrete diodes and transistors with pulse lengths from $0.1\mu s$ to $20\mu s$. A correlation was established between the dynamic heat distribution within the silicon device and a certain critical temperature. This work was extended by D.M. Tasca [23] and later on by F. Dwyer et.al. in 1990 [24] to further pulse lengths. The heat transfer equation (equation (3.1)) was solved for several cases and a relation of power to failure P_f and pulse duration t was established (equations (3.3) through (3.6)).

Another important failure category are the electrically induced failures. This group contains all failure modes which are initiated by an excessive electric field, e.g. breakdown of oxide layers [25].

Furthermore, high voltage drops during ESD pulses can cause parasitic bipolar transistor activation and destruction, e.g. inherent bipolar transistor of a DMOS transistor in BCD technologies [26]. All beforehand described failure modes are expected to be relevant for system level ESD and electrical stress robustness evaluation. Therefore, they are described in more detail in this chapter and the physical effects are explained. This is the basis for modeling the physical destruction limits of ICs under pulsed conditions.

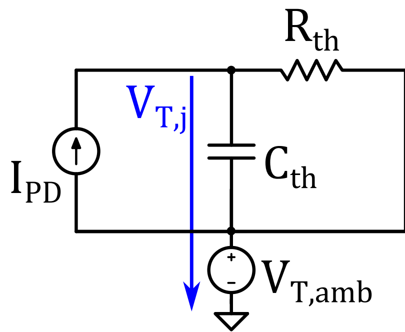
3.1 Thermal induced junction burnout

As ESD pulses force high currents through the IC, the current conducting elements are heated up due to power dissipation. The thermal destruction is very common during ESD tests and ESD threats in real world. Therefore, the physical details of this failure mode need to be

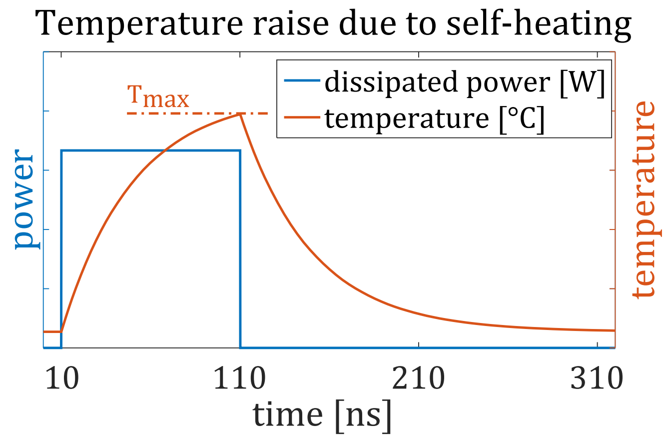
thoroughly reviewed.

3.1.1 Theory of heat flow in solid state materials and thermal destruction of silicon semiconductor technologies

During ESD pulses a certain current needs to be shunted to ground. As a consequence, a specific heat is generated within a fixed volume due to power dissipation within the semiconductor. As semiconductors are solid state materials there is only heat conduction and no convection. Each material has a specific thermal conductivity and a specific thermal heat capacity. Hence, the heat distribution is varying in different materials, e.g. silicon Si and silicon oxide SiO_2. At transient events the temperature rise caused by the power dissipation depends on the transient waveform and the material specific heat conduction properties. For a more vivid explanation the electrical equivalent circuit is used. The power dissipation P_D is depicted by a current source I_{PD}, the thermal conductivity λ by an electrical resistance R_{th}, the specific heat capacitance c_P by an electrical capacitance C_{th} and the temperature T of a certain point is represented by the node voltage, e.g. junction temperature $V_{T,j}$. The ambient temperature is represented by a voltage source $V_{T,amb}$, like presented in figure 3.1(a). The step response of this circuit is like the voltage rise at a capacitor charged with a constant current. The resistor enables some part of the heat flow (*in the equivalent circuit: current*) to bypass the capacitor (figure 3.1) and to discharge the capacitor. The equivalent quantities in the electrical respectively thermal domain are additionally summarized in table 3.1.



(a) Simplified equivalent circuit for self-heating



(b) Pulse response of equivalent circuit

Figure 3.1: Simplified electrical equivalent circuit to show the self-heating in semiconductor devices and its resulting pulse response to a rectangular power pulse with 100ns duration

Table 3.1: Equivalent quantities in the thermal and electrical domains

	thermal domain	**electrical domain**
potential	temperature (T, ϑ $[K, ^\circ C]$)	elect. potential (ϕ $[V]$)
potential diff.	temperature diff. (ΔT $[K]$)	voltage (V $[V]$)
quantity	heat (Q $[J]$)	charge (q $[C]$)
flux	heat transfer rate ($\dot{Q}$ $[W = \frac{J}{s}]$)	current (I $[A = \frac{C}{s}]$)
resistance	thermal resistance (R_{th} $[\frac{K}{W}]$)	electrical resistance (R $[\Omega = \frac{V}{A}]$)
conductivity	thermal conductivity (λ $[\frac{W}{K \cdot m}]$)	electrical conductivity (G $[S = \frac{1}{\Omega}$)

If a rectangular pulse is applied to this circuit, the voltage rises up to a certain peak value T_{max} at the end of the pulse figure 3.1(b). As long as this peak value stays well below a critical temperature, no destructive process is initiated. For increasing pulse amplitudes with the same pulse length at a certain point a critical temperature is reached and a destructive process is initiated within the semiconductor, usually at one single spot. For thermal destruction of semiconductor devices this critical temperature is at the point where an increase in temperature leads to a lower resistivity. Usually, the resistivity of doped silicon increases with a rising temperature, see 3.2. The figure shows schematically this temperature dependency of the resistivity for different doping concentrations [27]. As it can be seen each curve has a turning point at the critical temperature T_{crit}. Hence, the resistance goes down above this border. This point is reached when the thermally generated charge carriers are getting more than the charge carriers provided by the doping, i.e. the semiconductor gets intrinsic. This means, that an increasing temperature causes a significant increase in the number of charge carriers. As a result the current density is increasing respectively the resistivity decreases. Hence, the resistivity has a negative temperature dependence. This may cause current crowding at the hottest spot within the device where heating is even stronger. A feedback loop with positive gain is closed and ultimately leads to silicon melting in a very short time. In consequence, the junction is destroyed and therefore the device is no longer working as intended [27].

3.1.2 Power to failure depending on the pulse length for constant power pulses

As pointed out beforehand the thermal destruction of a silicon device is initiated at a critical temperature and the RC-network equivalent of the thermal surrounding of the device itself. Different power levels are needed with different pulse lengths to reach the critical temperature. As every material has its own thermal resistance R_{th} and thermal capacitance C_{th}, each single material layer needs to be modeled with one single RC-network to get the thermal path from the junction to the ambient. Additionally, to get a detailed temperature distribution within the device itself during ESD stress, it is necessary to discretize the thermal network like in finite

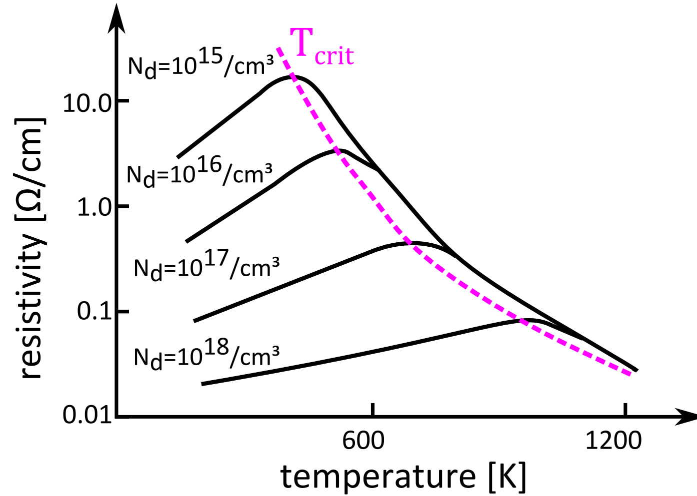


Figure 3.2: Schematic illustration of resistivity as a function of the temperature for different doping concentrations [27]

element method (FEM). Therefore, the thermal network is extended to several RC-networks for representing the thermal behavior of the ESD device 3.3. In the ESD time regime mostly the specific heat capacitance and thermal conductivity of the device itself is dominating. For very short pulses there is no heat flux out of the device itself, this is the so called adiabatic region. This means the power to failure P_f is inversely proportional to the pulse length td, $P_f \propto \frac{1}{td}$. Dwyer et.al. derived in 1990 [24] from the heat transfer equation (equation (3.1)) formulas for different time domain regions to calculate the power-to-failure depending on the device geometry of silicon devices. As the defect volume a cuboid is assumed with the dimensions a, b and c whereas $a > b > c$. The defect volume is equivalent to the physical geometry of the silicon device itself. Borders are generally materials with lower thermal conductivity than silicon itself, e.g. insulating layers of silicon oxide. The mass m of the defect volume is calculated by the volume ($v = a \cdot b \cdot c$) multiplied with the specific mass ρ In addition the heat generation is assumed to be in the center of the device. The adiabatic region is when heat distribution is possible in all three dimensions without reaching a thermally insulating material (e.g. silicon oxide). The formula postulated by Dwyer et.al. to calculate the power to failure dependent on the pulse duration for the adiabatic region is given in equation (3.3).

Moving to longer pulses some portion of the heat is already distributed away from the heat generating junction itself. This time regime was described quite detailed by Wunsch and Bell in 1968 [22], therefore it is often called the “Wunsch-Bell region”. In this region the power to failure is inversely proportional to the square root of the pulse length, $P_f \propto \frac{1}{\sqrt{td}}$.

For long pulse lengths and already static (DC) conditions the power to failure is a constant value as the heat distribution through the thermal resistances is dominating, $P_f = const$. In between these two sections the power to failure is inversely proportional to the logarithm of

the pulse length, $P_f \propto \frac{1}{log(td)}$. The explanation for this section was added by Dwyer et.al. in 1990 [24]. Based on the heat transfer equation (3.1) within solid state materials failure borders for thermal failures dependent on the pulse length can be defined in the model. Dwyer et.al. solved this equation for a rectangular parallelepiped shaped defect, subjected to constant input power. They expected that this geometry models the defect in many semiconductor devices accurately. Furthermore, their solution allows all three dimensions of the defect to take on the full range of values [24]. The results are four different power to failure P_f formulas (equations (3.3) to (3.6)) valid in different time domains. These four equations result in the four different gradients of figure 3.4. The joule heating caused by power dissipation generates heat directly at the junction of the device and rises the temperature starting from the initial value T_0. As pointed out beforehand the destruction process is initiated when a critical temperature is reached within the device. The different formulas have their origin in the fact, that at very short pulses heat distribution is possible in all three dimensions away from the junction. At a certain time t_c the heat flow reaches a different material, typically silicon oxide, which reduces heat flow significantly due to the low heat conductivity. At this point the heat can only be spread into two dimensions. Hence the temperature rises faster and the critical temperature T_{Crit} is reached faster.

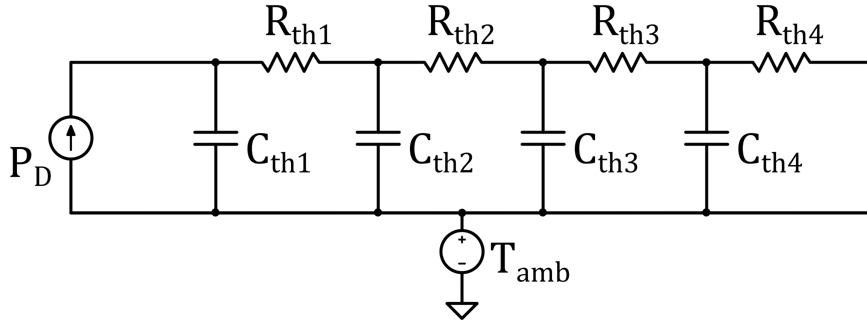


Figure 3.3: Extended electrical equivalent circuit to replicate the thermal response due to self-heating within semiconductor devices

$$\frac{\delta T}{\delta t} - d\nabla^2 T = \frac{q(t)}{\rho \cdot C_P} \tag{3.1}$$

$$m = a \cdot b \cdot c \cdot \rho \tag{3.2}$$

$$Region\ I: \quad P_f = m \cdot C_P \cdot (T_{crit} - T_0)/t_f \tag{3.3}$$

$$Region\ II: \quad P_f = \frac{a \cdot b \cdot \sqrt{(\pi \cdot \kappa \cdot \rho \cdot C_P) \cdot (T_{crit} - T_0)}}{\sqrt{t_f} - \sqrt{t_c}/2} \tag{3.4}$$

$$Region\ III: \quad P_f = \frac{4\pi \cdot \kappa \cdot a \cdot (T_{crit} - T_0)}{ln(t_f/t_b) + 2 - (c/b)} \tag{3.5}$$

$$Region\ IV: \quad P_f = \frac{2\pi \cdot \kappa \cdot a \cdot (T_{crit} - T_0)}{ln(a/b) + 2 - (c/(2 \cdot b)) - \sqrt{t_a/t_f}} \tag{3.6}$$

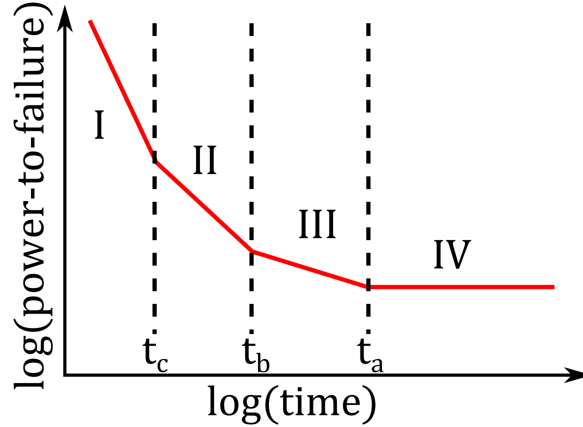


Figure 3.4: Schematic illustration of typical power to failure vs. pulse length of silicon devices, I=adiabatic region, II=Wunsch-Bell region, III=logarithmic region and IV=constant region [24]

Summing up, it can be stated that for short pulses like ESD high levels of power can be dissipated by the ESD protection devices before thermal destruction occurs. Going to longer pulses this power to failure P_f gets lower with several different gradients until thermal equilibrium is reached. The power to failure is no longer depending on the pulse length. The different gradients are schematically shown in figure 3.4. Based on the results of Dwyer et.al. generic formulas for power to failure P_{FAIL} and energy to failure E_{FAIL} can be stated dependent on the pulse length and with fitting parameters to replicate the failure borders for different devices. Two dedicated functions for modeling the thermal destruction limits of semiconductor devices E_{fail} and P_{fail} are chosen, see equations (5.6) and (5.7) (section 5.2.4 on page 53).

3.2 Electrically induced failures

Another prominent failure category caused by ESD pulses are electrically induced failures. The most typical failure of this category is the breakdown of oxides. This sort of failures is initiated by an excessive electrical field applied to an insulation layer. Furthermore, there are quite a lot of undesired devices formed during an IC manufacturing process, e.g. parasitic bipolar transistors due to alternating doped zones. Especially the avalanche breakdown of a reverse biased pn-junction is started at a certain voltage. The breakdown current often activates

unwanted current paths which may lead to destruction. Both failure types are explained in this section.

3.2.1 Oxide breakdown due to excessive electric fields

The intrinsic oxide of silicon SiO_2 or silicon oxynitride $SiON$ are used as insulator materials in silicon based semiconductor technologies. Each insulator has a certain insulation capability, which means that above a certain value of electrical field the insulator breaks down and a conductive path is formed. Also in the ESD time domain, the breakdown voltage V_{BD} is dependent on the stress duration td [25]. This failure is typically occurring at gate oxides of input stages or between two adjacent metal traces at different potentials during ESD events.

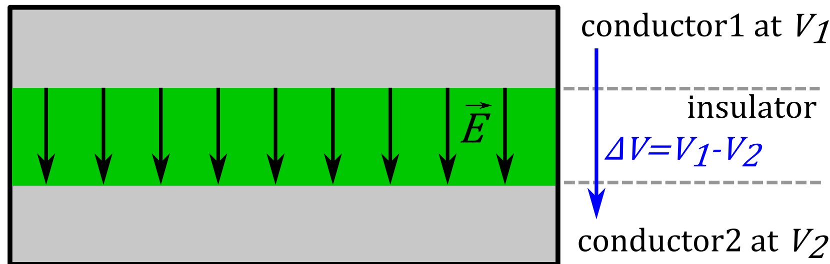


Figure 3.5: Electric field $\vec{E}$ within an insulator due to an external potential difference ΔV

The purpose of an insulator is to electrically separate two different regions, e.g. metal traces or gate and channel region of a MOSFET. During an ESD stress, high voltage differences occur in an IC caused by high currents with a fast rise-time. A voltage difference ΔV above the layer creates an electric field $\vec{E}$ within the insulator (figure 3.5). Each insulator can withstand a certain electric field strength before breaking down depending on the material, thickness and defects. At a critical field strength the insulator breaks down and a conductive path is created through the insulator. Depending on the insulator this path formation may result in a permanent damage or the insulation property maybe restored after the stress. In solid state insulators this process is generally irreversible, i.e. a permanent damage. By contrast, the spark formation in air is reversible and the insulation property of the air is restored after the spark quenching. The breakdown voltage depends on the material properties and additionally on the stress duration. Time dependent dielectric breakdown (TDDB) is the technical term often used in this context [25]. Comparable to the thermal failures, oxide breakdown occurs for short pulses at higher stress levels [28]. Figure 3.6 shows that for very short pulses like ESD the insulating layers (e.g. gate oxides) can withstand higher stress voltage levels than under "DC" conditions. Additionally, it was shown that the breakdown voltage increases with layer thickness. For detailed modeling the destruction limit, a time dependent critical voltage is best suitable. In ESD time domain the stress duration for oxide layers is limited to a certain time frame where the breakdown voltage has only a small variation with stress time. Therefore, it is

reasonable to model the critical voltage value as a constant value with acceptable accuracy.

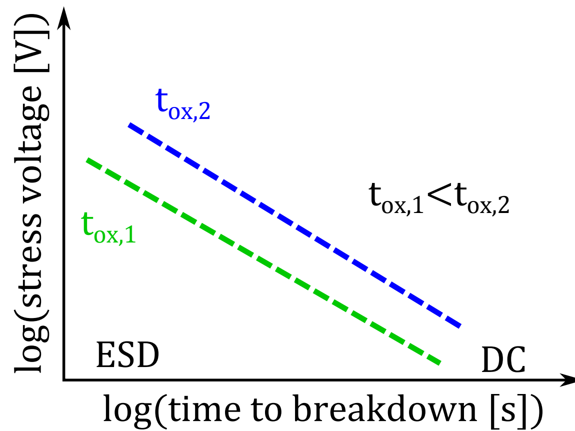


Figure 3.6: Schematic illustration of the time to breakdown at different stress voltage levels of silicon oxide layers (SiO_2 or $SiON$) in a double logarithmic plot according to [28]

3.2.2 Triggering and destruction of parasitic elements

Another important failure mechanism within ICs is the triggering of parasitic elements. These parasitic devices are not designed for carrying ESD current and as a result they are destroyed usually after activation. Many of these parasitic devices are formed by the junction isolation concepts, e.g. npn-transistor between neighboring n-wells with a p-substrate (figure 3.7) [29]. Parasitic bipolar transistors can partly be avoided by different isolation concepts like silicon on insulator (SOI). Other parasitic devices cannot be avoided as they are formed by the construction of the intended device itself, like the inherent npn-bipolar transistor of a n-channel MOSFET device (figure 3.8). Furthermore, the construction of complementary metal-oxide-semiconductor (CMOS) technologies, with n-channel and p-channel MOSFETs next to each other, always creates a parasitic silicon controlled rectifier (SCR) (figure 3.9). All these parasitic devices are not activated within the operational voltage range as they have breakdown voltages above the functional voltage range. In case of ESD, however, the voltage drops can be higher than the functional voltage range due to the high currents. These high voltages values can cause an avalanche (or zener) breakdown of a pn-junction in reverse polarization, e.g. collector-to-base breakdown of a npn-transistor (see figure 3.8 for example). This current is then conducted for example to the ground net of the IC. Although base B and emitter E are usually shorted together at least on a metal layer, there can be an electrical potential difference between base and emitter due to the silicon resistance R and the base current I_b. If this potential difference goes above one diode forward voltage (typically $\approx 0.6\ V$) the bipolar transistor is activated. The $V_{BE} \approx 0.6\ V$ turns on the transistor which conducts current from collector C to emitter E with a reduced voltage drop, the so called snap-back (figure 2.3).

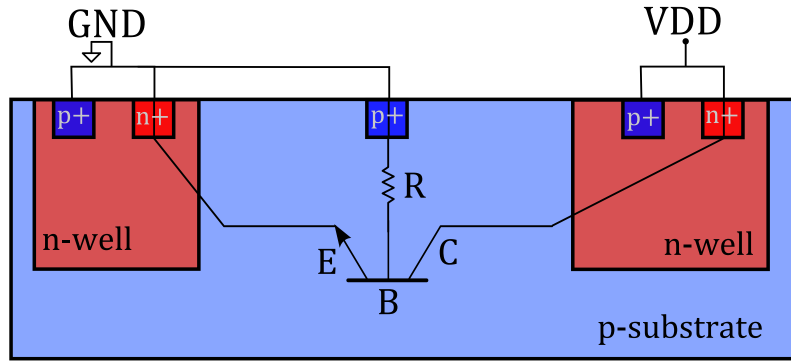


Figure 3.7: Schematic illustration of a NPN-transistor between two neighboring n-wells through the p-substrate

Inherent parasitic bipolar transistors within MOSFETs

Every MOSFET has also an inherent, parasitic bipolar transistor due to its device construction. A n-channel MOSFET (like schematically depicted in figure 3.8) is constructed of two highly doped n-implants ($n+$) (source and drain of the transistor) with a p-doped region in between. This p-region forms the current conducting channel of the MOSFET device and its conductivity is controlled by the gate electrode above. When the gate-bulk V_{GB} voltage is below a certain threshold, the transistor is off and no significant current is conducted rather independent from the drain-source voltage. If the gate-bulk voltage is above the threshold voltage, charge carriers (electrons) from the p-region are accumulated at its surface and the current conducting channel is formed, i.e. the transistor is switched on and can conduct electron current from source S to drain D [30]. The highly doped n-regions also form an npn bipolar transistor together with the p-region as indicated in the drawing. Accordingly each p-channel MOSFET possesses an inherent pnp bipolar transistor. As explained before, this bipolar transistor can be activated during high current injection, like ESD events. It has to be distinguished between MOSFET devices where this bipolar transistor is used as an ESD protection element like a grounded gate NMOS (ggNMOS) on the one hand. In this case the bipolar transistor is optimized to conduct the ESD current homogeneously over the whole device width and hence has a significant ESD current capability. On the other hand there are MOSFETs which are optimized for functional reasons, e.g. high voltage DMOS in BCD technologies, but where the inherent bipolar transistor cannot conduct any ESD current at all. They show destruction more or less immediately after triggering due to the snap-back phenomenon accompanied by a highly non-uniform current spreading. This section focuses on the latter one. The triggering of the bipolar transistor which is the destruction point of the MOS transistor is dependent on the gate-bulk potential, current density and the device temperature. Hence the modeling of this destruction limit is a complex endeavor. Within ICs the MOSFETs have usually a gate driver circuit which limits the gate voltage during ESD. This reduces the complexity of this modeling topic and the onset of the

bipolar can usually be described with the thermal failure equations.

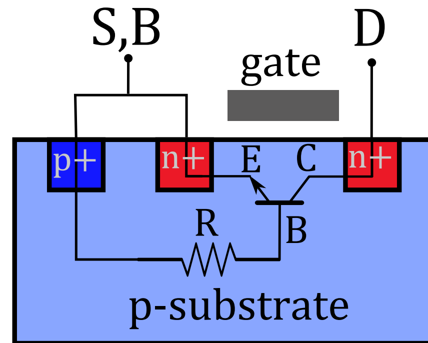


Figure 3.8: Schematic illustration of a n-channel MOSFET with its inherent, parasitic NPN-transistor

Parasitic bipolar transistors through the substrate

Within a silicon IC there are lots of n-wells which may be electrically isolated due to functional or EMC reasons. If during an ESD event the neighboring n-wells get a potential difference, the inherent NPN-Transistor through the substrate can be activated. This transistor is generally not optimized to conduct ESD current and hence gets destroyed after activation. A basic illustration of this substrate-npn-transistor is shown in 3.7. As the substrate cannot be left floating in an IC, it is usually connected to one of the ground nets within the IC. Because the p-doped substrate is the base of the bipolar transistor, a current flow out of the substrate connection increases the substrate potential locally. When this potential reaches $V_{BE} \approx 0.6\ V$ the NPN-Transistor is activated and destroyed easily [29]. Modeling of these substrate bipolar transistors is challenging as they strongly depend on the layout [31] [32] and they are not in focus in this work. Nevertheless, an extraction is possible, if they are described with a model, they can be included in the complete IC model to show the failure points at certain stress levels.

Parasitic thyristor in CMOS technologies

Another well-known parasitic device is a SCR formed by nearby PMOS and NMOS transistors typically found in CMOS technologies. Figure 3.9 shows schematically how the thyristor is formed by the two MOSFETs. Especially in advanced CMOS technologies the thyristor is often used as an ESD protection element. In this case again the device needs to be optimized to conduct the ESD current homogeneously over the whole device width. These modifications usually need additional effort. Also other combinations of NPNP or PNPN layers can form a parasitic thyristor which can be hard to identify. Generally, a model to describe the turn on behavior together with the dynamic resistance and a quite low thermal destruction limit

shall be enough. This reproduces the activation of the SCR and early failure due its low ESD robustness when it is not optimized for ESD.

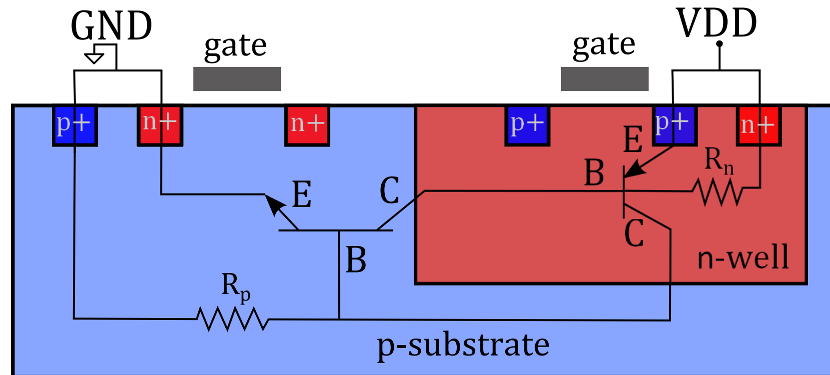


Figure 3.9: Schematic illustration of a CMOS inverter and its inherent thyristor between *VDD* and *GND*

Summary

To sum up this chapter, it can be stated that different failure mechanisms need different failure recognition mechanisms within the model. Thermal failures can be well described with generic formulas for power-to-failure and/or energy-to-failure over pulse time derived from the solution of the heat equation established by Dwyer et.al. Oxide breakdown can generally be simplified to a certain critical voltage. If a higher accuracy is desired, the critical voltage level for oxides can be modeled as a function of the stress time. The parasitic bipolar transistors or respectively thyristors can be modeled with a ESD behavioral model combined with a very low thermal failure threshold which can be constant over the pulse duration. The higher effort is to detect these devices from design data and extract their ESD behavior.
This work focuses on modeling the ESD behavior and thermal destruction limits of dedicated ESD protection devices.

4 ESD robust system design - SEED approach

For precise system ESD robustness simulations accurate models for each single component are necessary. During ESD injection high currents with fast rise-times are present. Hence, the models of all components need to be valid in the ESD time and current regime [33]. Multilayer ceramic capacitors (MLCCs) show a degradation of the capacitance when they are exposed to high voltages like during ESD stresses [34]. Transient voltage suppressor (TVS) devices can have a high voltage overshoot due to their turn-on characteristics [35]. Furthermore, PCB traces often have a few nH of inductance per cm trace length which can cause inductive voltage spikes in case of ESD events while the trace inductance plays usually a minor role in the functional range [36]. All these effects are discussed extensively in literature [37], [38], [39] and need to be taken into account for precise ESD robustness simulations on PCB level. Therefore, the typical effects and their possible model implementation are discussed in this chapter.

4.1 System Efficient ESD Design (SEED)

The topic of system level ESD robustness design is not new and has been discussed in literature extensively in the past. At one point the Industry Council on ESD Target Levels summarized all known misunderstandings regarding this topic. A broad variety of experts in this field came together and summarized the literature in a white paper [1]. Based on this work, a methodology to design for a certain ESD robustness of systems, was developed and called the "System Efficient ESD Design (SEED) Approach" published in [2]. This methodology focuses on designing for a certain ESD robustness of a system (e.g. PCB, phone, ECU, etc.) according to [15], [14] or [40]. The approach is based on measurements to characterize the response of the single components to a system ESD pulse. Based on these results the residual pulse waveform at the IC is estimated. Together with the characterization measurements of the standalone IC an evaluation is done, if the IC in the system is likely to be damaged at the required test level. If this is the case, the PCB is optimized (additional/different external protection elements, change in PCB layout, etc.) until the IC is able to survive the residual pulse at its pins [2]. The methodology can either be deployed by simulation or by manual comparison of the component‘s pulsed I-V-characteristics. Crucial for this methodology is the knowledge of the transient behavior of the single components, either in the form of accurate simulation models or transient characteristics (e.g. TLP i-v-curve of different pulse lengths). This approach is quite resource intense, especially in terms of measurement equipment and time consumption. Alternatively,

the needed information can be provided by the component vendor as he might know best the transient behavior of the component. This can be an IC model for simulations or in written form, e.g. application note or data sheet. This procedure seems to be the best way for the involved parties to get detailed and accurate information of the components‘ transient behavior. Unfortunately, this approach has crucial drawbacks which seem to be blocking points: The component vendors have the justified fear that they disclose some intellectual property (IP) and, in addition, that they have to guarantee the communicated transient behavior under all circumstances. Those are seen as the main reasons why no extensive exchange of IC models or further transient information in the data sheet is done up to now. Therefore, a methodology needs to be developed which can model on the one hand the relevant transient behavior of the components in a simplified manner. While on the other hand the IP of the component vendor is effectively protected.

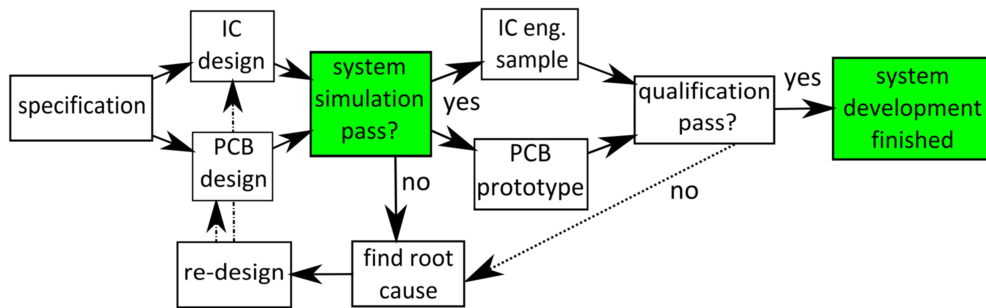


Figure 4.1: Proposed development cycle for optimized ESD robustness of electronic systems even before hardware prototypes are available

During system level ESD stress there is not only physical destruction possible, but there are also the so called soft-failures (system resets, communication loss, etc.) according to [15], [14]. As these effects are not primarily addressed by the SEED approach, the *extended SEED* approach was discussed in literature [41]. For the latter methodology the transient behavior is necessary, in addition to the quasi-static behavior used for the standard SEED approach. Furthermore, the core behavior of the IC (e.g. digital logic) needs to be integrated into simulation on behavioral level. The first step is, providing a behavioral model including destruction limits of complete ICs, to enable system ESD robustness evaluation of systems by simulation. This is the main focus of this work. Later on the IC modeling framework can be extended to address also functional failures and enable the *extended SEED* approach by simulation.

In an ideal situation the system ESD robustness is optimized already during the system design phase (selection of discrete components, PCB layout, etc.) even without a hardware prototype (figure 4.1). System simulations in an early design phase allow an optimal co-design of the ESD protection placed inside an IC and on the PCB. Ideally the functional behavior

of the system is not influenced by the ESD protection design. This work proposes a novel methodology to generate behavioral IC models for system ESD simulations including typical destruction limits. The necessary transient behavior during ESD events as well as the typical destruction limits are included in a generic model architecture. This enables short simulation runs by simplified models and an evaluation of the system ESD robustness. A generic model architecture allows to combine several devices into one model which can effectively protect the IP of the IC vendor. No detailed information is included in the model. Neither details about ESD protection devices (device type, performance per cell, silicon area, etc.) nor the circuit of the ESD protection concept or the functional parts of the IC are disclosed. First of all, a methodology is presented to generate these behavioral ESD models based on measurements (chapter 5). Later on a methodology is described to generate the complete IC model from design data (chapter 6) without measurements on the complete IC. The effectiveness of the proposed methodology is shown in chapter 7, where simulation results are compared with measurement data.

4.2 Modeling PCB traces for ESD simulation

ESD pulses can have a rise time below one nanosecond up to peak current values of several tens of amperes [15], [14]. At these high current change rates (di/dt) an inductance of even a few nano Henry can generate voltage spikes of several tens of volts. Therefore, the parasitic inductance of PCB traces can strongly influence the system response to ESD pulses. Hence, all the parasitic values (inductance, capacitance and resistance) shall be included in the system ESD simulations. Depending on the complexity of the PCB layer stack and the routing several approaches for this task are possible. For PCBs with a low number of layers and no crowded layout a lumped element model of the PCB traces calculated with the formulas for embedded microstriplines can be suitable [36].

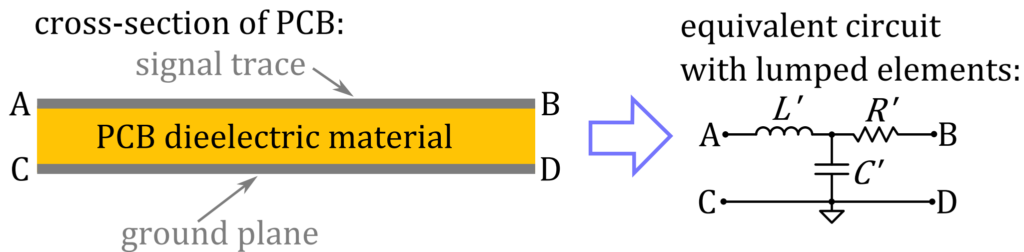


Figure 4.2: Simple equivalent circuit of PCB traces with inductance L', resistance R' and capacitance per length C'.

One lumped element (R‘, L‘ and C‘) per trace can be implemented as shown in figure 4.2. For a more detailed analysis or longer PCB traces a ladder of these elements in a row can represent one trace. This structure is also able to reproduce the signal propagation delay on the

traces. For more complex PCB designs sections of transmission lines were shown to be a precise solution [42]. Furthermore, one can think of describing the PCB routing with S-Parameters extracted by measurements or with a field solver from the design data [43].

All approaches have some drawbacks and advantages and there is no optimum solution, as it depends on the application and the system complexity which amount of effort is suitable and gives adequate results.

4.3 Behavioral modeling of discrete components

Discrete components used on PCBs, like ferrite core inductors or ceramic capacitors, can have a very special behavior during ESD pulses. The reason for this is mostly that, ESD pulses are larger than the useful signals in terms of current and voltage magnitudes. Therefore, high current/voltage effects can occur in these devices and change their behavior completely [43], [44]. The real transient behavior of the external components is crucial for system level ESD simulations, hence these effects need to be modeled accurately. This section will highlight a few device types, their ESD behavior and the resulting model implementation to enable precise system simulations.

4.3.1 Modeling multi-layer ceramic capacitors (MLCCs) for ESD analysis

Capacitors are widely used in the PCB design to stabilize supply voltages or filter out high frequency noise. Therefore, they are often mounted on PCBs and also used for ESD protection as they can shunt some part of the incoming ESD current to ground. They are often combined with series resistors to limit the current flow into the IC pins in the manner of a low pass filter. In this case the capacitors often face very high voltage levels during ESD events when there is no low-ohmic discharge path in parallel to them. For example on automotive PCBs often capacitors with a DC rating of $50V$ or $100V$ are used. During ESDs they can sustain much higher voltage drops due to the very short pulse duration. However, at these high voltages the capacitance is often significantly reduced. This means they are less effective in ESD protection as expected. This phenomenon was investigated and described in detail by Scheier et.al. [45]. Furthermore, the capacitors are sometimes less good discharge paths than expected when the PCB layout is not optimized in terms of short connections from the signal line via the capacitor to ground [36]. Also, the capacitor itself has a parasitic resistance R_{ESR} and a parasitic inductance L_{ESL}. The L_{ESL} value is typically in the range of $1nH$ or below, but this can have significant influence.

These are the main reasons why capacitors cannot be modeled by an ideal capacitance. By contrast, they need to be modeled with their parasitic values and also the degradation in capacitance at high voltage levels is expected to be relevant. The equivalent circuit of figure 4.3 was proposed by Scheier et.al. [45], is accurate and well suited for system ESD simulations. When a low-ohmic discharge path in parallel to the capacitor is present, the

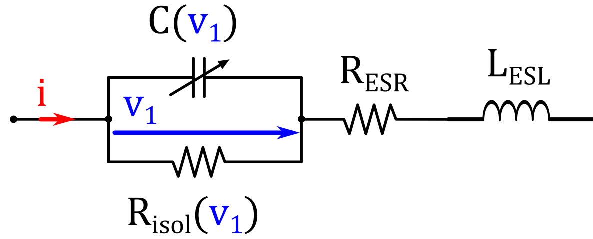


Figure 4.3: Advanced equivalent circuit to model the behavior of MLCCs during ESD injection proposed by Scheier et.al. [45].

capacitance degrading at high voltages can often be neglected.

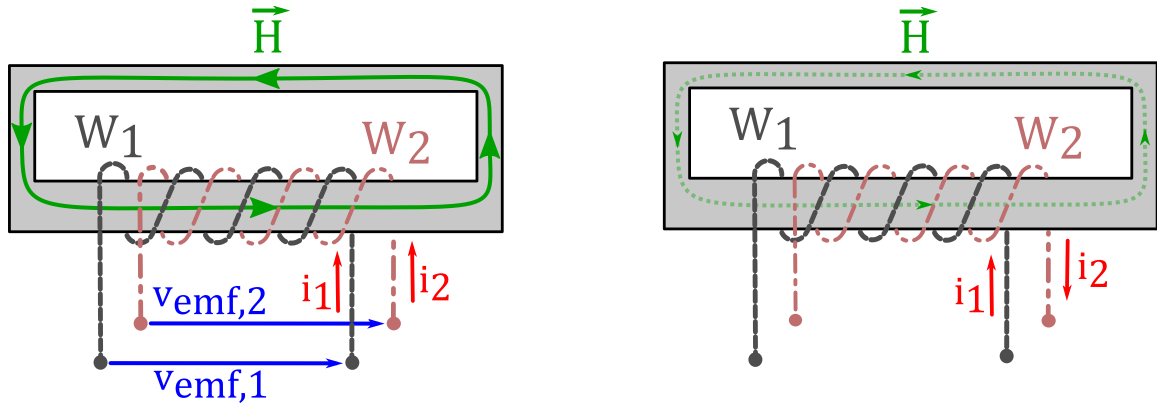
4.3.2 Modeling transient voltage suppressor (TVS) devices

Transient voltage suppressor (TVS) devices are very common to protect electronic systems against disturbance pulses, like ESD, EFT, load dump, surge or burst. Several device types are available, e.g. TVS diodes, varistors or gas discharge elements. They have different underlying physical mechanisms, but the protection principle is common for all. In the functional range they are high-ohmic not to influence the functional behavior of the system and to guarantee a low leakage current. Above a certain voltage threshold they turn on and shunt the disturbance pulse to ground to protect vulnerable devices like ICs or micro-controllers. Their transient behavior can be accurately characterized by TLP measurements [44]. There are several modeling approaches discussed in literature [46], [47], [48], [8] and [49]. The number of different approaches already gives the hint that there is no optimum modeling approach for all devices, but that there are specialized approaches for specific device types. For a model it is important to replicate the real transient behavior of a device regardless of the model architecture and simulator implementation. The turn-on behavior needs to be handled carefully, e.g. turn-on delay or conductivity modulation, as this creates significant voltage overshoots at the device to be protected. Furthermore, some time-dependent behavior of the dynamic on-resistance, like self-heating, needs to be modeled. It is obvious that parasitic elements, e.g. inductance and resistance of bond wires, needs to be taken into account as these can create also severe voltage overshoots. Ideally these TVS device models include also the typical destruction limit to see in simulation when their limit of the protection capability is reached.

4.3.3 High current effects in ferrite core inductors - characterization and modeling

Common mode chokes (CMCs) are often used in differential communication buses to enhance the electromagnetic compatibility (EMC) in terms of low emissions and high noise immunity. To achieve high inductance values and therefore high damping performance of the common mode currents, they are usually made with ferrite cores. By its construction, the common mode

inductor damps effectively common mode currents while differential currents are transmitted nearly without losses. In the functional range the currents seen by the inductor are comparably low. In case of ESD pulses the current can be very high. It is expected that the ferrite core goes into saturation and hence loses the damping behavior. If this behavior is appropriately characterized and modeled, the influence on the system behavior during ESD testing can be simulated. This subsection introduces a comprehensive methodology for characterizing and modeling the high current behavior of common mode inductors. This enables to quantify the residual pulse waveform at single components like integrated circuits.



(a) Common mode choke with resulting H-field at common mode current injection

(b) Common mode choke with resulting H-field at differential mode current injection

Figure 4.4: Basic sketch of a common mode choke with two windings (W_1 and W_2) on a bar-shaped ferrite core, often used in differential bus systems. a) The CMC is driven with a common mode current on the two windings, thus the overall H-field in the ferrite is high. b) showing the CMC with a differential mode current, hence the overall H-field in the ferrite is nearly zero and no significant emf is induced.

CMCs are basically two or more electrically separated windings on a common ferrite core to create a strong magnetic coupling between the windings, see figure 4.4. This results in low impedance for differential signals due to the cancellation of magnetic fields in the ferrite core. The elements are used for both reducing the common mode emissions of e.g. transmitting communication ICs or switch mode power supplies (SMPS) as well as damping the common mode noise on the receiver side for a better signal to noise ratio (SNR). As these devices for communication buses are designed for small signal amplitudes, it is expected that they show saturation and reduced damping of common mode currents [50].

Construction of common mode chokes

In general, electrical current through a wire causes a magnetic field (*H-field*) in the surrounding area. Depending on the material the *H-field* causes a certain flux density (*B-field*, see equation (4.1)). Furthermore, a change in the magnetic flux (Φ) creates an induced electromagnetic

force (emf) within N wire loops surrounding the magnetic field, see equation (4.2). The emf is working against its root cause current (Lenz's rule). This means the emf tries to push a current in the opposite direction to the existing current, hence decelerates the change in current.

$$\vec{B} = \mu_0 \cdot \mu_r \cdot \vec{H} = \frac{\Phi}{A} \tag{4.1}$$

$$V_{emf} = N \cdot \frac{d\Phi}{dt} = -L \cdot \frac{di}{dt} \tag{4.2}$$

A magnetic field in the ferrite core induced by one of the windings is seen by all windings as they share the ferrite core. If a current is flowing in one winding, the resulting change in magnetic flux $d\Phi/dt$ induces, in first approximation, the same electromagnetic force (emf) in all windings (figure 4.4(a)). By contrast, if two windings induce a magnetic flux with the same value but opposite orientation, then the resulting magnetic field in the ferrite is nearly zero as both fields cancel out each other. This is the so called differential mode (figure 4.4(b)). Without a magnetic flux in the ferrite there is no induced emf at the windings, i.e. the windings show only an ohmic resistance much lower than the impedance obtained in the case of common mode current.

High current behavior of CMCs

Characterization of device behavior during ESD events is typically done with rectangular pulses (TLP). The result is a quasi-static i-v-curve for a certain pulse length. By contrast, common mode inductors are usually characterized in the frequency domain with an vector network analyzer (VNA) to see the behavior in the functional range. The scattering parameters (S-parameters) of the DUT are measured with a sinusoidal signal across a frequency range and under small signal conditions (e.g. $V_{pp} = 1V$). This characterization indicates the small-signal damping behavior of the CMC in the operational range.

As expected during ESD events ferrite core inductors show saturation, which changes their behavior drastically [43], [50]. Therefore, the pulsed large signal behavior of ferrite core inductors is characterized up to several tens of amperes with the TLP and with different pulse lengths. The resulting quasi-static behavior shows this saturation (figure 4.5). The measurements are shown exemplary on the ACT45B-101-2P with nominal inductance of 100 μH typically used in CAN applications. The TLP measurements were done on one winding, i.e. the current pulse is forced through one winding and the resulting voltage at this winding is measured (cf. figure 4.6). Up to the nominal current rating (150 mA), the common mode choke acts as an inductor, as expected. This can be seen as constant slope in the log-log-plot in figure 4.5. The different pulse duration (different colors) have different zero crossing values which is related to the decreasing voltage drop when a constant current is applied.

Above this current threshold, the ferrite enters saturation and hence the voltage drop is rapidly

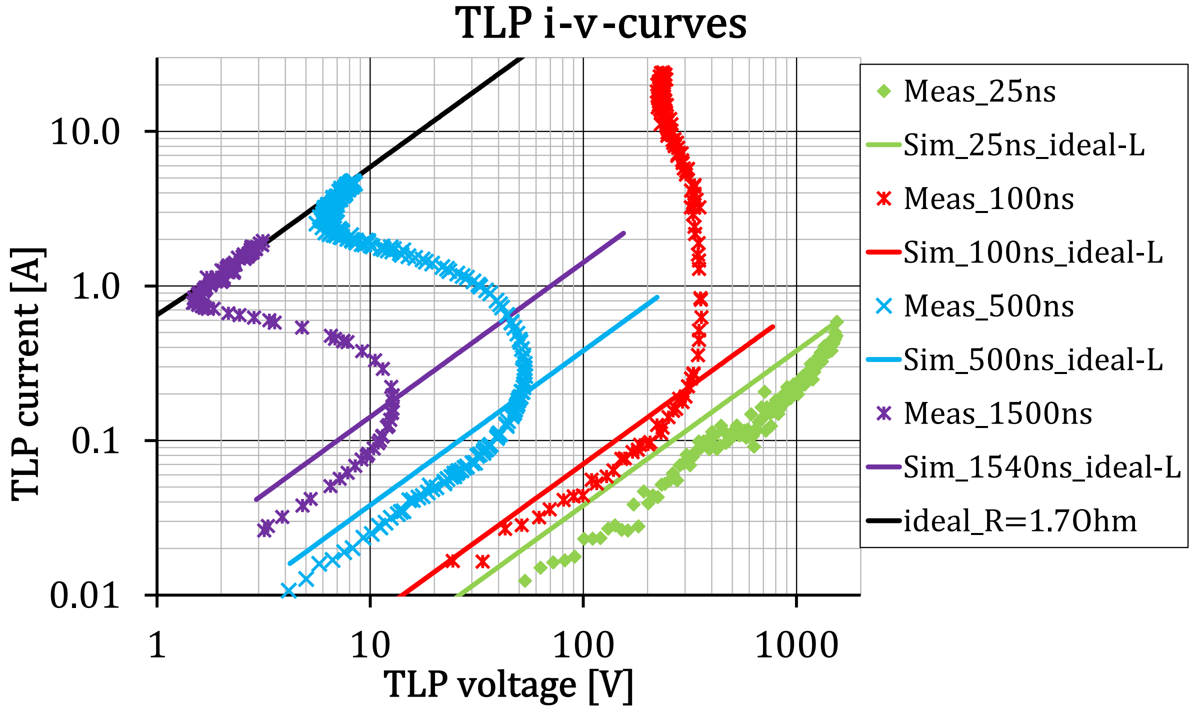


Figure 4.5: Quasi-static i-v-curves of a CMC type ACT45B-101-2P obtained by measurements and simulations with an ideal inductance.

reduced, see figure 4.5. At high current levels ($I > 2.5\ A$) and long pulse durations ($td > 500\ ns$) the saturation is so strong that only the copper resistance of the wire ($R_{copper} \approx 1.7\ \Omega$) can be measured. The measurement of the current and voltage setup was done with the TLP Kelvin setup [51]. For the current measurement a Tektronix CT-1 is placed between the TLP pulse out and the pin a. With a 5 $k\Omega$-resistor the voltage at pin a is measured with the oscilloscope with reference to ground respectively pin c. The voltage can either be measured on the pulsed winding V_{ac} or on the second (floating) winding V_{bd}. The measurement of V_{ac} shows directly the saturation behavior (see figure 4.5) while with V_{bd} the coupling behavior during pulsed stress can be measured.

The saturation behavior is better visible in the transient voltage and current waveforms, see figure 4.7. The figure shows the voltage (light blue) and current (red) waveforms measured at an 1540 ns TLP pulse on one winding while the second one is left floating. At the beginning of the pulse current is nearly zero and voltage is at the maximum, the CMC shows a very high impedance as expected. The current linearly increases while the voltage drop decreases within the first 300 ns. This behavior is expected from an ideal inductance. After $\approx$ 400 ns the voltage drops rapidly to nearly zero while the current rises to maximum current the TLP can deliver at this pulse amplitude. The ferrite core of the CMC is strongly saturated. As a result, the impedance of the CMC winding drops significantly down to the ohmic resistance of the winding wire. The figure also includes simulation results with an ideal inductance model

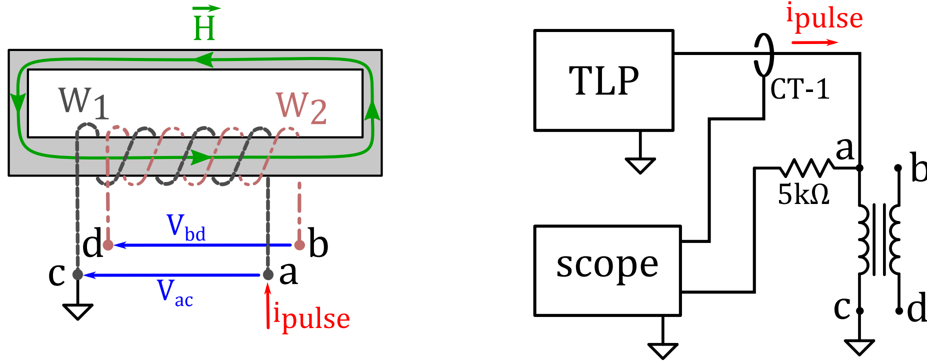


Figure 4.6: Pulsed high current characterization (TLP, ESD, etc.) of the CMC.

without saturation effects in dotted lines. The ideal inductance model is only correct up to $\approx 150\ mA$. Above this current level an ideal inductance is not able to reproduce the CMC behavior. This range above $150\ mA$ is for functional considerations not in focus, but for system ESD injection this range of main interest.

Data evaluation of the transient voltage and current waveforms, in terms of inductance value at certain current levels, show clearly the saturation behavior. Figure 4.8 shows the evaluated inductance plotted versus current level for numerous TLP pulse with a width of $1540\ ns$. The saturation above $150\ mA$ is clearly visible together with the drop of inductance down to nearly zero. At current levels below $150\ mA$ it is hard to see any clear correlation of inductance value and current level, this might be related to measurement uncertainties as the TLP system is optimized for high current levels (several amperes).

Modeling the high current behavior of CMCs

Based on the measurement results plotted in figures 4.5 and 4.7, a model architecture is developed to model the saturation effects during ESD current injection. A comparable approach to [43] is chosen to model the saturation effects within a SPICE simulator.

The first step is to divide the coupled inductor ($0 < k_1 < 1$) into the stray inductance ($k = 0$) and the perfectly coupled mutual inductance ($k = 1$, c.f. 4.9) in order to prepare for modeling the saturation behavior.

Generally, a common mode inductor with ideal coupling ($k = 1$) can be modeled by a circuit like shown in figure 4.10. The induced emf is created by a multiplication of the inductance value L and the time derivative of the current through it di/dt, like stated in equation (4.2). The time derivative of the current is created by the small differentiating circuit on the right of figure 4.10. Although two coupled inductors can be modeled by two separate inductors and a coupling factor k in SPICE transformer, this circuit is better suitable for the expansion towards saturation modeling. The proposed model architecture has been presented at the 2019

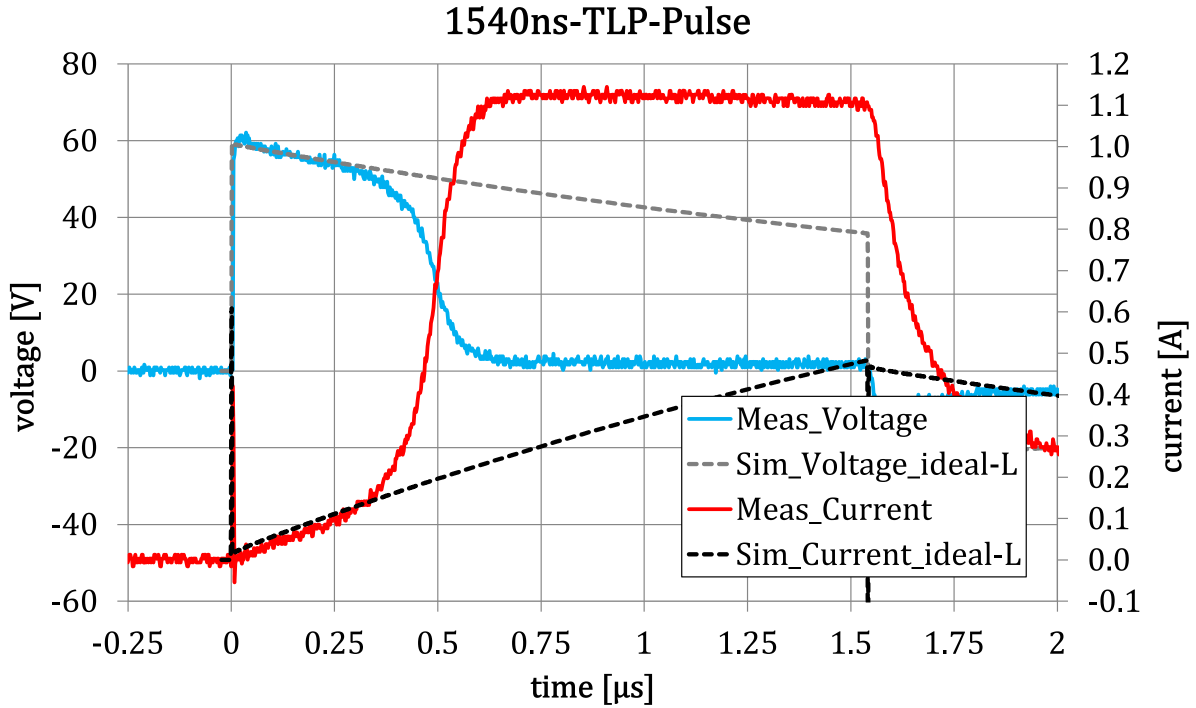


Figure 4.7: Comparison of current and voltage waveforms of a TLP pulse obtained by simulations and measurements.

EOS/ESD Symposium [52].

If the underlying transient waveforms of the i-v-curves in figure 4.5 are evaluated in terms of current value and calculated inductance value at each point in time according to equation (4.2), a relation between current level and inductance value is found. This correlation can be fitted with the empirical equation (4.3), including fit parameters x and y, and integrated into the advanced model, see figure 4.11. The model topology can also be integrated into more detailed models, e.g. extension with additional stray inductance. Furthermore, the value of the inductance needs to be limited to the typical value, otherwise the inductance value would go to infinite values when going to small currents.

$$L = x \cdot i^{-y} + z \tag{4.3}$$

Surprisingly, the measurements show that at the beginning of the pulse the induced emf is built up in the first few tens of nanoseconds. It would be expected from an ideal inductor that the induced emf has its peak value at the beginning of the pulse and decrease constantly over the pulse duration. It seems that the magnetic field needs some charge to fully build up. It is assumed that this kind of delay is somehow related to the alignment of the single Weiss domains within the ferrite. This process "consumes" a portion of the magnetization current which is no longer contributing to the magnetic field. Therefore, a certain amount of charge ($Q = i \cdot t$) is

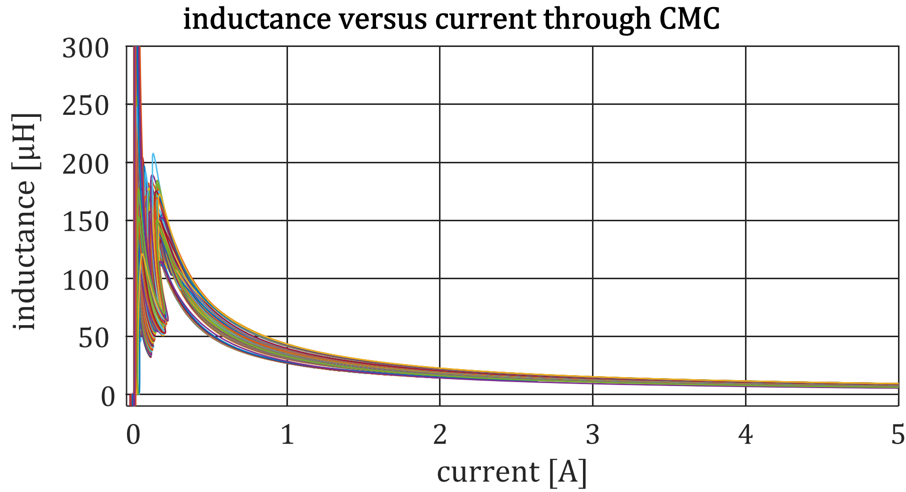


Figure 4.8: Inductance vs. current level through CMC, evaluated from transients of TLP pulses with 1540 *ns* width.

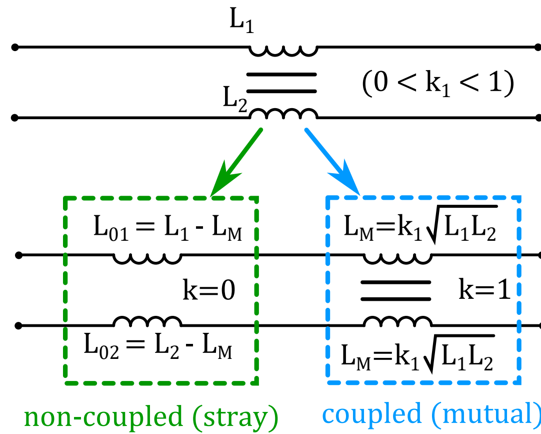


Figure 4.9: A coupled inductor (CMC) can be divided into two parts, the non-coupled stray inductance and the ideally coupled mutual inductance.

necessary before saturation can start regardless of the current level. This phenomenon is also integrated in the advanced CMC model.

Matching of the proposed CMC model with measurement data

The following parts presents some simulation results with the proposed modeling methodology compared to measurement data. Simulation results with an ideal inductance are also included to emphasize the necessity the proposed, complex CMC model for system ESD simulations.

The beforehand presented TLP-i-v-curves of figure 4.5 are completed by the results of the proposed CMC model im figure 4.12. The matching of the proposed model with measurement data is significantly better than the results with the standard CMC model (ideal inductance L). The proposed model is able to reproduce the impedance decrease at high current levels (i.e.

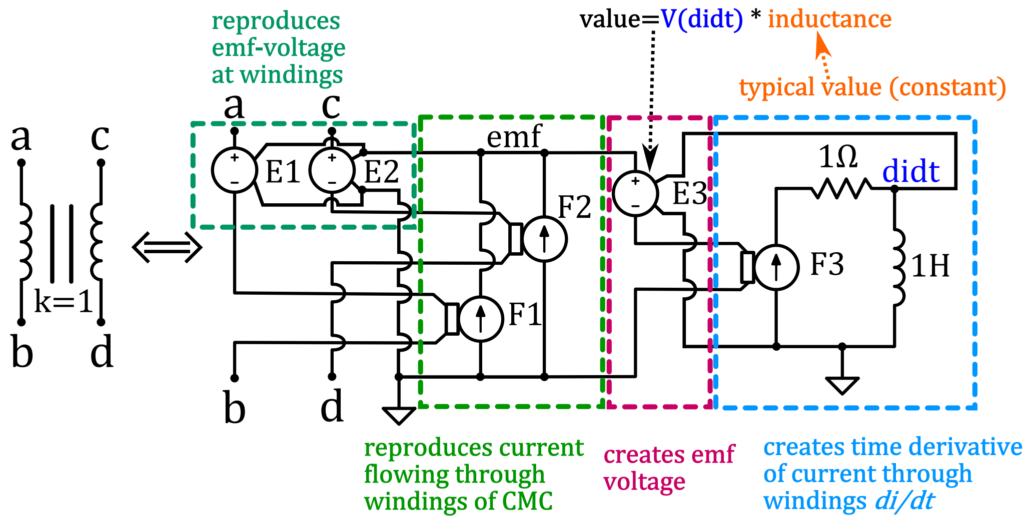


Figure 4.10: Basic model of a common mode choke with ideal coupling. A change in the time derivative of the current di/dt induces in both windings the same emf-voltage.

saturation) which can be seen be the low voltage drops at high current levels.

As the system level ESD pulse does not have a rectangular waveform, but rather a double pulse shape [15], [14] additionally HMM-TLP measurements [53] and simulations were done to prove the model quality. Within the system the important to know is the residual pulse waveform which reaches the IC through the CMC. Without this information it is not possible to make a reasonable design of the overall system ESD robustness. The figure 4.13 shows the transient waveforms of a HMM-TLP injection into one winding of the CMC. Again an excellent matching of measurements and simulations is obtained with the proposed CMC model. The simulated waveforms with the advanced CMC model (dark red=current, dark blue=voltage) match well with the measured waveforms (light red=current, light blue=voltage). Also the saturation starting at ≈ 30 ns is replicated well. By contrast, the basic CMC model (dashed lines) is not able to model the transient behavior during high current pulses.

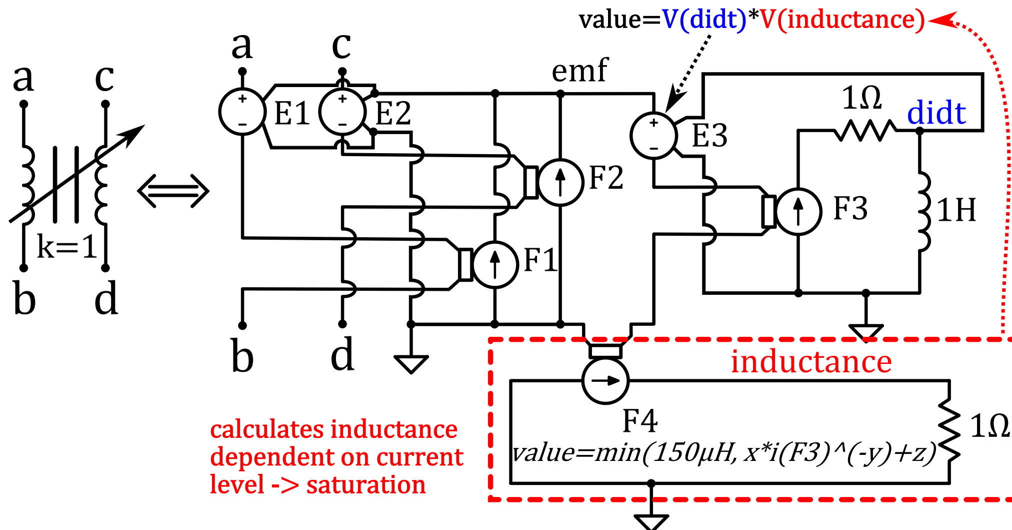


Figure 4.11: Advanced model of a common mode choke with ideal coupling and saturation during high current injection. Based on the setting of the parameters x, y and z the saturation, which is dependent on the current level, can be fitted to the measured values.

Summary

Detailed models of the single components in a system can enable precise ESD simulations on PCB level. A lot of transient effects show up during ESD tests, but the effects can be described by extended behavioral models. The SEED approach was presented as the basic idea to design for a certain robustness of a system against ESD events. This approach can be very promising, but only under the premise that the models of all single components are valid in the ESD domain (high currents/voltages and very short pulses). Several modeling techniques for discrete elements are summarized. Additionally, a novel methodology to characterize and model the behavior of ferrite core inductors in the ESD regime is developed in this work [52].

The existing gap of precise and compact IC ESD models will be closed by the following two chapters.

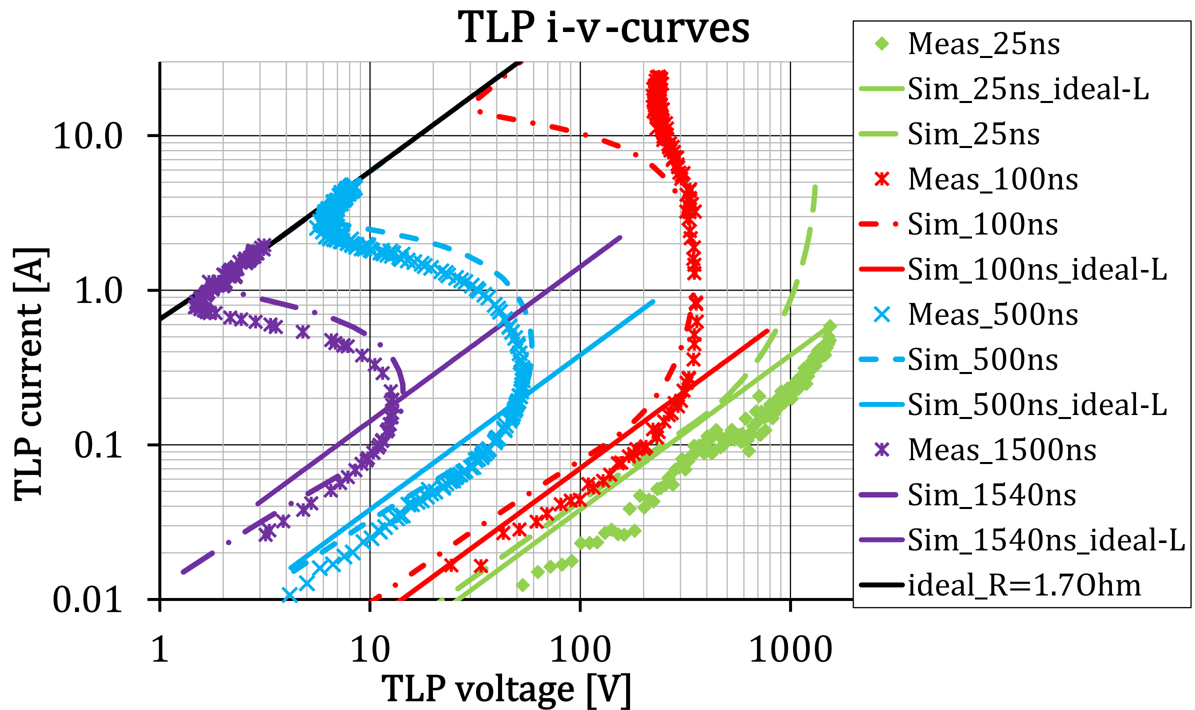


Figure 4.12: Quasi-static i-v-curves of a CMC type ACT45B-101-2P obtained by measurements and simulations with an ideal inductance.

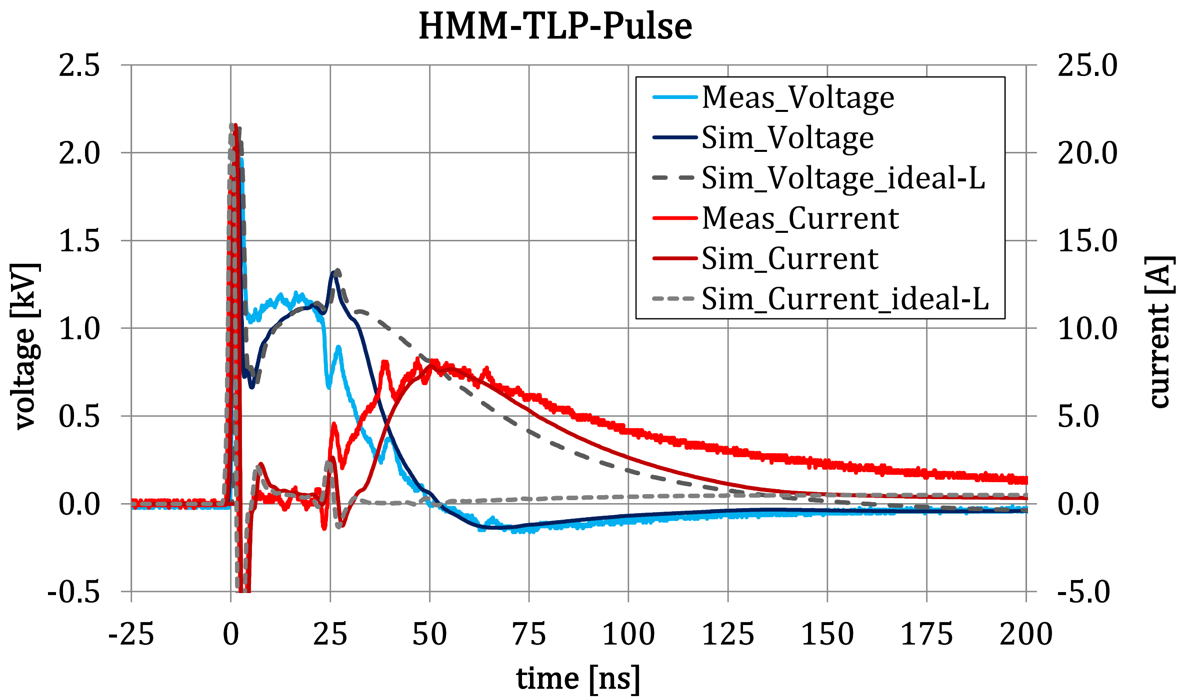


Figure 4.13: Comparison of current and voltage waveforms of an HMM-TLP pulse obtained by simulations and measurements.

5 Transient behavioral modeling methodology of semiconductor devices

This section will give detailed information about a novel methodology for generating behavioral models of ESD protection elements. The model describes the transient response to stress pulses above the operating conditions as well as the nominal destruction limit of the device. The proposed generic model can also be used for pin combinations of complete ICs. With this model architecture ESD and electrical stress simulation regarding the system robustness are enabled. The generic model architecture enables the exchange of models between IC vendor and system designer. An implementation of the generic model architecture for SPICE simulators is shown in this chapter, but the model architecture can be transferred also to hardware description languages (HDLs) or other simulator languages.

5.1 Requirements on the novel modeling approach

To develop an appropriate modeling methodology it is necessary to know typical requirements on the IC models and to consider them. Hence, the major requirements are discussed in this section. During the IC design phase it is nearly impossible to determine which residual pulse will occur at the IC pins during disturbance pulses applied to the system, like ISO10605 [15] or ISO7637-2 [18]. Even if IC designers know which pulses will be applied to the PCB connector, it is difficult to predict how the external elements and PCB traces will shape the pulse along the propagation path. On the other hand system designers cannot evaluate the behavior of the system without having information about which components playing which roles under certain stress conditions. System simulation without IC can be done for the worst case check. It can be accurate for ICs which can only conduct small currents before being damaged (e.g. advanced CMOS ICs). On the contrary, power ICs manufactured for example in BCD or smart power technologies can take up to several amperes for a limited pulse duration without physical destruction. In this case a co-design of IC and external protection leads to an optimized protection solution as proposed by the SEED approach [2]. Furthermore, some types of ESD protection devices are turned on dynamically and conduct transient current below the absolute maximum ratings (AMR) of voltage values. In this case, it is not sufficient only to check whether the voltages applied to the IC pins are below the AMR during a system ESD event. This work focuses on co-design of smart power ICs and PCB components by the use

of system simulation even during IC and PCB design phase to obtain a system's robustness against pulses.

5.1.1 Transient behavior in case of disturbance pulses above operating conditions

As the nominal compact models for on-chip devices focus on the functional operation, they do not always describe correctly the high current behavior during ESD stress. Therefore, the nominal models are in general not suitable for ESD simulations. The high current behavior of an IC is desired for ESD modeling. Reference [54] presented a methodology for the modeling of the on-chip ESD protection devices both in the ESD regime (high currents and short pulses) and in the functional regime to get the correct leakage currents during operation. Those models also contain the physical destruction limits as well as self-heating of the devices and the linked change in on-resistance. These are the major requirements on the models for ESD simulations. Despite of the existing modeling approach [54] a generic ESD model is desired which can describe the ESD behavior of various device types.

5.1.2 IP-Protection for IC vendors

Another major concern of IC vendors when providing ESD models of ICs is to give away their intellectual property (IP) for free. Usually the circuit details such as circuit concepts, device specific parameters and performance data are company confidential information. As the ESD models of ICs shall be offered on the open market, a black box behavioral modeling methodology is chosen as a solution. To encrypt the model library can be another option. This offers also a strong IP protection. However, it has the drawback that simulation with encrypted models is usually limited to certain simulators which might not be available to every system designer.

5.1.3 Simplification for simulation speed-up

It is often preferred by system designers to have short simulation runs for cost reasons when simulating the system behavior under ESD stress. In the ideal case, ESD simulation results can be obtained within a few minutes or hours of computation time. Therefore, complete full-chip models are in general not suitable as the simulation would require too much time. A methodology is needed to generate simplified models for the ICs to replicate the high current behavior with an acceptable accuracy. Optimally, the IC models contain only one or a few subcircuits or elements per pin-combination.

5.1.4 Relevant pin-combinations for system-level simulation

To further reduce the model complexity the IC model shall focus on system-level relevant pins. This means all pins which are connected to the PCB connector, referred to as global pins as well as all the pins connected to external capacitors, need to be modeled with high accuracy.

The rest of the pins can be modeled primitively to reduce modeling effort and model complexity because these pins are unlikely to face ESD or other disturbances which can result in high currents through the pins. Therefore, it is usually sufficient to model these pins as high-ohmic resistance connected to ground and define a critical voltage as a failure criterion.

5.1.5 Physical destruction limits of semiconductor devices

Simulations on system level can first of all provide the correct current distribution and voltage drops. This helps to determine if a physical damage is likely to occur at a certain ESD stress voltage. Many of the physical destruction caused by ESD are thermal breakdowns. This means the energy dissipated in the chip is so high that the critical temperature of circuit elements in the ESD current path is reached due to self-heating, see chapter 3. As the IC models are designated to be used for various pulse lengths, a constant threshold for the physical damage is not adequate. By contrast, based on the results of Dwyer, Wunsch and Bell the power-to-failure versus pulse length needs to be modeled with functions which are able to replicate the different gradients of the curve. The second failure mechanism during ESD tests is dielectric breakdown mainly occurring at gate oxides. This failure mechanism is not linked to a certain power or energy of the pulse, but to an excessive voltage drop over an insulator [25]. Ideally this dielectric breakdown is also time-dependently modeled. For simplicity the failure threshold can often be modeled as time invariant with sufficient accuracy.

Another failure mechanism related to ESD was reported for DMOS transistors [26]. It was reported that the failure power is no longer increasing when going to shorter pulse durations but rather stays at a certain current level. The explanation pointed to the electrical SOA of the DMOS: a critical current density in the device triggers the parasitic bipolar transistor which is destroyed immediately after snap-back. Such failure border can be modeled with a critical current threshold in contrast to the voltage threshold described beforehand. Depending on the device to be modeled one or several failure threshold levels are considered and implemented in the models.

5.2 Black box transient behavioral modeling (TBM)

A generic, behavioral model architecture with a set of parameters is developed [8]. The generic model can reproduce the transient behavior of single ESD protection elements as well as complete pin-combinations of an IC. The model is intended to replicate one polarity of the device to be modeled. To implement both polarities of a device they need to be characterized and modeled separately. The resulting models can be combined anti-parallel to replicate both polarities. The following sections present specific circuits to model certain transient effects which play a role during ESD pulses. All used circuit elements are defined on the official homepage of the UCA Berkeley [55] where the first *Simulation Program with Integrated Circuit Emphasis*

(SPICE) was developed and is further maintained. The current version is called Spice3f and directly based on SPICE2G.6, which are usually the basis for most of the commercial available SPICE simulation tools. Therefore it is expected that the presented model architecture is usable within numerous SPICE based circuit simulators.

5.2.1 Switch-based behavioral model for ESD protection elements

The basic behavior of every ESD protection element is to be high-ohmic in the functional range and to enter conduction mode above a certain voltage threshold, see figure 5.2(a).

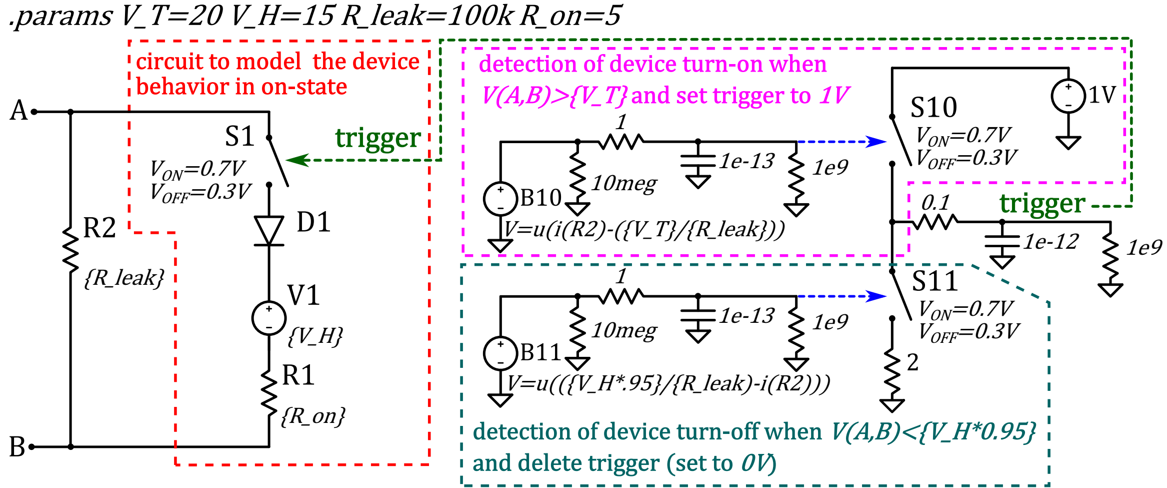


Figure 5.1: Basic schematic of a switch-based behavioral model for ESD protection elements which allows also snap-back phenomena with a black box model.

The most basic model for this behavior is a high-ohmic leakage resistance *R2* and in parallel a switch *S1* which turns on at a certain voltage (see figure 5.1 based on [47], [5]). To replicate the dynamic on-resistance during pulses a resistor *R1* is used in series to the switch. Additionally, a voltage source *V1* is placed in series to model the additional voltage drop. Furthermore, an ideal diode *D1* is placed to allow current flow only in one direction (see figure 5.1). The switch *S1* is controlled by the voltage *trigger* which is usually set to zero $V(trigger) = 0\ V$. If a voltage above the trigger voltage $V_{A,B} > V_T$ is detected, the behavioral voltage source *B1* (equation (5.1)) activates the switch *S10* to charge the node *trigger* to one volt $V(trigger) = 1\ V$. This closes the switch *S1* and the current can be conducted via *S1*, *D1*, *V1* and *R1* from terminal *A* to terminal *B*. The signal *trigger* is set to $1V$ as long as the voltage $V_{A,B}$ is above the holding voltage V_H. When $V_{A,B} < V_H * 0.95$ the behavioral voltage source *B2* (equation (5.2)) activates the switch *S11* to set the node *trigger* to $0V$ again and hence the switch *S1* is opened again. As a threshold only 95 % of the holding voltage V_H is used for numerical stability, especially to avoid ringing between on- and off-state. The additional elements in the control circuit for the node *trigger* are added for numerical stability and low-pass filtering of the pulse voltages

generated by *B10* and *B11*. The low-pass filtering improves the convergence of the circuit as the time derivatives of current di/dt and voltage dv/dt are limited to acceptable values. This structure can model avalanche breakdown based elements very well. But there are often bipolar transistor based ESD protection elements which show a typical snap-back after turn on (figure 5.2(a)). This behavior can be successfully modeled when the voltage source *V1* does not reproduce the trigger voltage V_T, but rather the holding voltage V_H [8].

Quite often used within the behavioral sources is the unit step function $u(x)$ which gives 1 as a result when $x > 0$ and 0 for $x < 0$. This enables an easy detection, if a certain signal is above a threshold or below. Furthermore, within behavioral sources each current through a device or terminal of a device ($i(X)$) as well as every node voltage ($V(X)$) or voltage difference between two nodes ($V(X, Y)$) can be used for calculation. Moreover, the basic numerical functions and also some typical functions (e.g. square root, logarithm, etc.) are implemented [55].

$$V(B1) = u(i(R2) - (V_T/R_{leak})) \tag{5.1}$$

$$V(B2) = u((V_H \cdot 0.95/R_{leak}) - i(R2)) \tag{5.2}$$

5.2.2 Dynamic on-resistance during ESD pulses

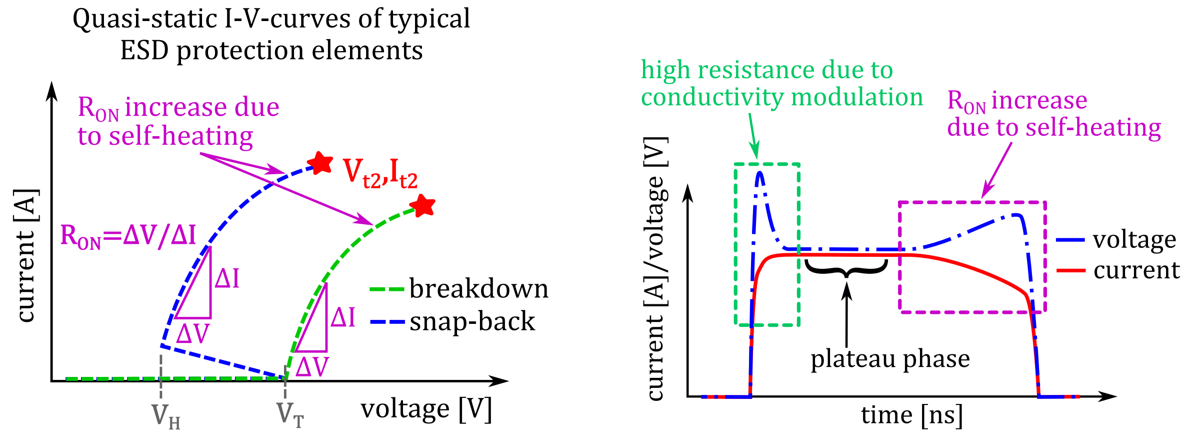
One important device characteristic for ESD and EFT pulses is the dynamic on-resistance during the pulse. There are phenomena like self-heating or conductivity modulation during turn-on well known from literature [56]. As they can influence significantly the device behavior during short pulses they need to be integrated in the model.

$$i(B4) = V(n2, B)/(R_a \cdot V(Energy)^{R_b} + R_c) \tag{5.3}$$

$$i(B3) = V(n22, n2)/\left(R_c \cdot 0.01 + \frac{R_{sm}}{1 + V(qm)/q0}\right) \tag{5.4}$$

$$R_s = R_{s0} + \frac{R_{sM}}{1 + Q_M/Q_0} \tag{5.5}$$

As depicted in figure 5.2(a) at high current levels the dynamic R_{ON} increases often due to self-heating. This effect is typical for high voltage ESD protection devices used in BCD technologies for HV pins ($\approx 10 \cdots 100\ V$). Furthermore, ESD devices often show conductivity modulation effects, also well known as forward recovery especially with diodes in forward current conduction [56], [57]. Figure 5.2(b) illustrates the conductivity modulation effect and the self-heating at transient waveforms. Schematically a rectangular pulse (TLP) is applied to a DUT which shows both effects. At the beginning of the pulse the DUT is very high-ohmic due to the conductivity modulation (forward recovery) and hence has a high voltage overshoot at a



(a) Schematic quasi-static behavior of typical ESD protection elements.

(b) Schematic illustration of conductivity modulation and self-heating during a rectangular pulse.

Figure 5.2: Schematic illustration of self-heating and conductivity modulation and how they are affecting the dynamic resistance in the quasi-static behavior (figure 5.2(a)) and also in the transient waveforms (figure 5.2(b)).

comparable low current. Due to the exponential declining of the recovery resistance transient voltage and current waveforms go to a stable plateau phase. After this plateau phase the self-heating with an increasing dynamic resistance is shown by a rising voltage while the current goes down. Therefore, the dynamic R_{ON} is implemented dependent on the dissipated energy of the device. This is realized by integrating the power dissipation during the pulse within the model with the behavioral current source *B14* and a capacitor of $C = 1F$ (figure 5.3). The resulting node voltage *Energy* is used in the behavioral current source *B2* to model the resistance increase due to self-heating, see equation (5.3). The basic idea is to model the current with the voltage drop over it and the desired resistance value $i = V/R$.

The conductivity modulation is implemented with current source *B1* which is dependent on the charge already flown into the device (see equation (5.4)) comparable to equation (5.5) found by [56]. In this equation there is the term $+R_c * 0.01$ which ensures numerical stability when the recovery resistance goes to zero. So a minimum value of 1 % of the nominal dynamic resistance is the minimum value which allows still short computation times while the dynamic R_{ON} is only minimal influenced. Within the model the charge calculation is done by the current source *B13* and a capacitor of $1F$ which is basically the integration of the current flow through *B1* during the pulse. With the implementation of variable resistors by behavioral current sources a broad variety of resistance values and also dependencies can be realized. Also one could think of combining both behavioral current sources to model the single phenomena in only one behavioral source.

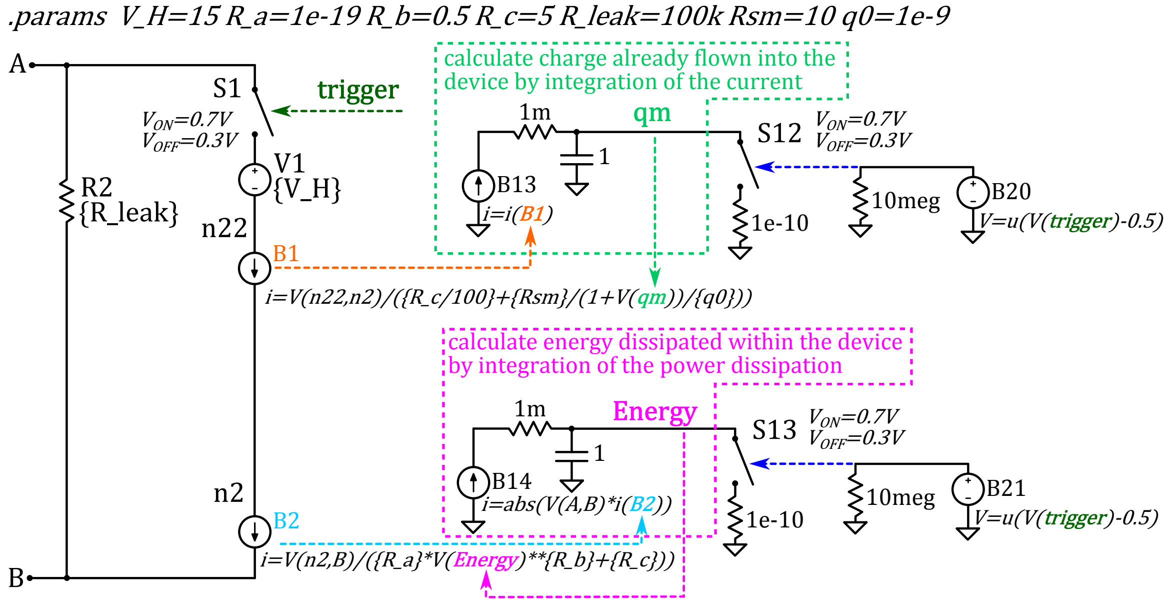


Figure 5.3: Schematic which can model resistance change effects during ESD pulses, namely conductivity modulation and self-heating.

5.2.3 Voltage- and/or current-thresholds for changes in effective on-resistance

Especially for pin-combinations, but also for single devices there are sometimes kinks in the quasi-static I-V-curve. These kinks indicate a change in the conduction mode of the device itself or the start of conduction of parallel (parasitic) current paths without immediate destruction. They can be voltage or current density driven. Therefore, one current controlled switch *S2* is implemented in parallel to the dynamic resistance R_{ON}, see figure 5.4. In series to the switch there is again a voltage source and a resistor to model the transient resistance of this parallel current path. The voltage source *B3* needs to replicate the voltage over the energy dependent R_{ON} at the trigger current level I_r2 and therefore it is implemented with the energy dependent resistance multiplied by the trigger current value. The dynamic resistance of this path is modeled with *R3*. Moreover, the switch *S3* is added to model the voltage dependent activation of parallel current paths. It is a voltage controlled switch and directly controlled by the voltage drop from node *n2* to node *B* $V(n2, B)$ and activated at V_r2. In this path there are as well a voltage source *V2* and a resistor *R3* implemented in series. For numerical stability reasons the turn-off of the switches is 10% below the turn-on threshold.

For sure the illustrated dynamic resistance *R1* shall be implemented dependent on the energy as described beforehand. This is neglected in figure 5.4 for simplification reasons as this is not the core of this subsection. One can think of additionally implementing further parallel current paths either voltage or current triggered. Furthermore, one can think of implementing the parallel current paths as well with an energy dependency and/or conductivity modulation.

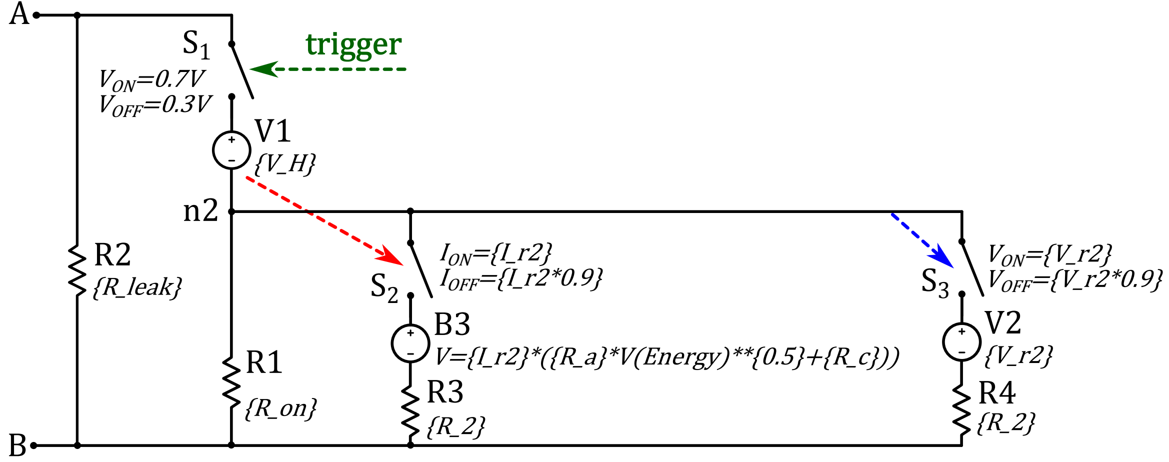


Figure 5.4: Model implementation of parallel current paths to model kinks in quasi-static I-V-curves due to additional current paths starting at certain voltages or current densities.

This can be done according to section 5.2.2 for each current path respectively. For the current smart power ICs this was not necessary and hence not implemented up to now.

5.2.4 Destruction limits

One essential part to successfully simulate the ESD robustness of ICs is the destruction limit. Ideally, the failure borders are integrated in the simulation model and there is an automated check if these borders are exceeded or not. And hence a direct feedback is given to the user, if the applied ESD stress level is likely to damage the IC or not. Chapter 3 summarized the relevant failure mechanisms and the related failure borders. The most common failure mode during ESD testing is the thermally induced junction burnout due to Joule heating. ESD protection devices are designed to dissipate the energy of the ESD pulse in order to protect the functional circuit of the IC and hence heated up. Depending on the pulse duration and the thermal properties the critical temperature is reached at different energy levels for various pulse lengths. Derived from the work of Dwyer et.al.[24] a generic formula (equation (5.7)) for the energy to failure is implemented in the behavioral model. This failure border is theoretically enough to model the thermal failure border. To get higher accuracy and security if something went wrong with the fitting parameters additionally the power to failure border is implemented, see equation (5.6). Additionally, a voltage threshold as another failure border V_{fail} is implemented. For the time being this threshold is simply implemented as a constant value. A further extension can be also a pulse duration dependency of this threshold.

$$P_{fail} = P_a \cdot td^{-0.5} + P_b \cdot td^{-1} + P_c + P_d/log(td) \tag{5.6}$$

$$E_{fail} = E_a \cdot td^{0.5} + E_b \cdot td + E_c + E_d \cdot log(td) \tag{5.7}$$

Both failure functions are dependent on the pulse duration td and have four fitting parameters to match the measured values. Both are derived from the four segments in the power to failure curve described in section 3.1 [24]. One can think of combining the equations (3.3) to (3.6) by simply adding them. This results in one power to failure equation for several pulse durations which is dependent on the geometry and thermal properties of the device. By replacing all constant factors by combined fitting parameters one gets equation (5.6). As this fitting function is based on the underlying physical mechanisms it is well suited to describe the power to failure of a silicon device without containing detailed information about the device itself. TLP is the standard tool for characterization of ESD protection elements and their destruction limits. Because of the constant power during the TLP pulse the energy is calculated by simply multiplying the power with the time $E_{TLP} = P_{TLP} \cdot td$. In first approximation the energy to failure is calculated accordingly $E_{fail} = P_{fail} \cdot td$. So the energy to failure equation (equation (5.7)) is derived from the power to failure formula (equation (5.6)).

.params E_a=1e-19 E_b=1e-19 E_c=1e-6 E_d=1e-19 P_a=1e-19 P_b=1e-19 P_c=1e6 P_d=1e-19 V_fail=70

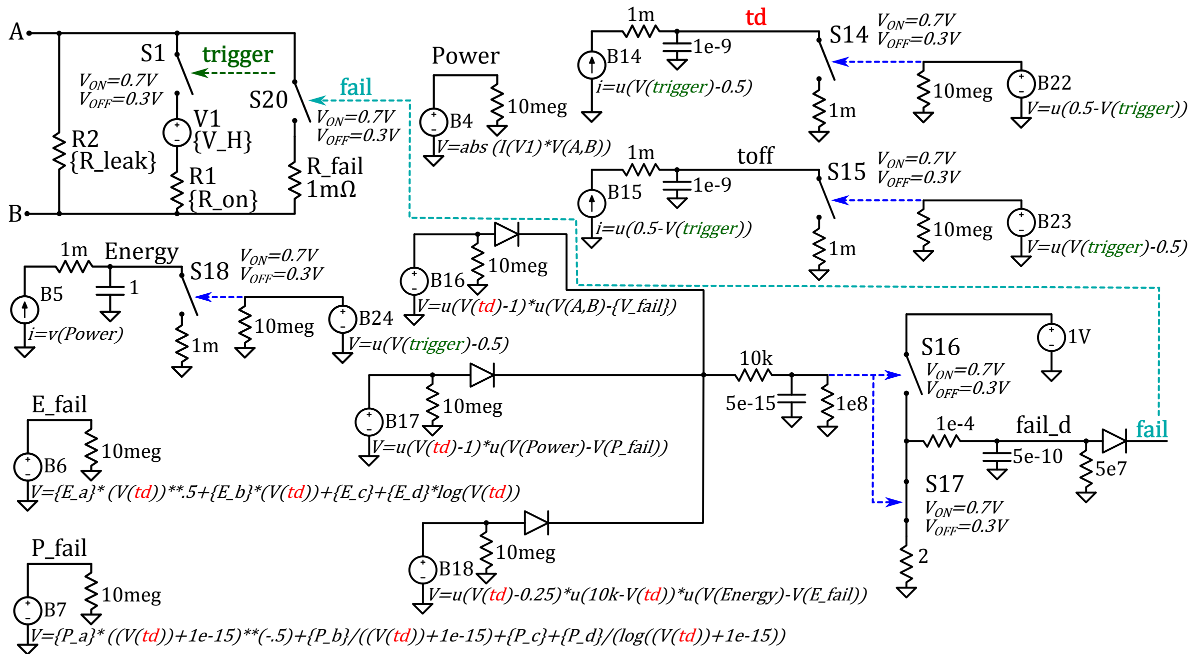


Figure 5.5: Basic schematic of a circuit to model the failure borders and detect if these borders are exceeded during stress pulses.

The complete implementation of the failure detection is shown in figure 5.5. In the upper left corner there is the ESD element itself with the pins A and B together with the main switch *S1*. Next to it there is a circuit which represents the power currently dissipated within the device, behavioral voltage source *B4* and node *Power*. Below there is a circuit to calculate

the energy already dissipated within the device during the pulse. This is done by the current source *B5* which deflects the electrical power and the integration with a capacitor of $1F$. For future applications to multi-pulse events the energy value can be deleted again with switch *S16* which is closed when the trigger voltage is zero. On the lower left there are two voltage sources *B7* and *B6* which replicate the power to failure, respectively the energy to failure, dependent on the pulse duration. The upper right corner shows the circuits to calculate the current pulse duration *td* in nanoseconds, again by integration with a capacitor. This capacitor has $1nF$ of capacitance to get the time value directly in nanoseconds. The current on-time of the device *td* is used within the functions of energy to failure *B6* and the power to failure *B7*. Furthermore, the off-time since the last time the trigger was set $V_{trigger} > 0.5\ V$ is calculated by integration. The evaluation, if one of the failure borders is reached, is done by the circuit in the lower right corner. Voltage source *B17* gives zero volts as long as the actual power is below the power to failure at each time point during the simulation. When the currently dissipated power *B4* goes above the power to failure *B7* and the pulse duration *td* is greater than 1 *ns* the voltage goes to 1 V at the voltage source *B17*. This closes the switch *S16* and opens the switch *S17* (normally on) which raises the potential of the node *fail* to 1 V. The detection, if the energy to failure E_fail or failure voltage V_fail is exceeded, is done accordingly with *B18* respectively *B16*. The *failure* node is comparable to a digital flag which is either 1 V when one of the failure borders is exceeded or otherwise 0 V. Therefore, this signal is an output signal of the model. This enables an automated data processing if a certain stress pulse level on the system or IC is likely to damage the IC or not. Additionally, a low-ohmic current path, formed by *S20* and R_fail, indicates the failure in the waveforms during transient simulations.

Again in most of the circuits there are additional elements to improve numerical stability. Parallel to each voltage source there is a high-ohmic resistor to ground (typically 10 $k\Omega$) to enable convergence. Furthermore, RC-filter elements are used as low-pass filters to improve convergence by reducing the dv/dt and di/dt to finite values. In addition, one can think of including some significant delay of single signals with the RC-elements if desired.

5.2.5 Generic model architecture of TBM

The combination of all beforehand described phenomena and their model implementation result in a generic, behavioral model architecture for ESD protection elements including destruction limits. A simplified schematic is shown in figure 5.6. A set of parameters controls the transient behavior of the device and also the failure thresholds. This generic subcircuit can be used to describe one single ESD protection element of a complete pin-combination of an IC depending on the device used for the characterization. It has to be noted that each subcircuit is only able to reproduce the transient behavior for one polarity. If both polarities are desired, a dedicated TBM for each polarity is needed. Both shall be connected anti-parallel to get the transient behavior of both polarities.

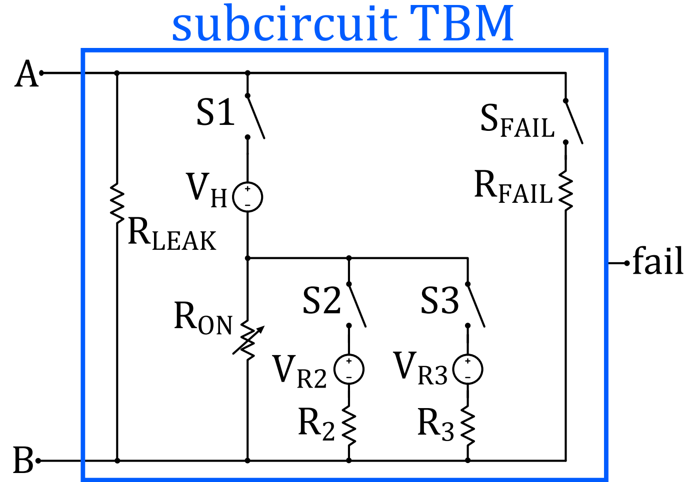


Figure 5.6: Simplified schematic of the TBM model architecture to model the behavior of ESD protection elements during ESD events including destruction limits.

By combining several TBM subcircuits in parallel and/or in series one can get a black box model for a complete IC. Such a black box model is suitable for system ESD and electrical stress simulation on PCB level [8]. In combination with the external circuitry of the IC the robustness of systems can be predicted by simulation [36]. This enables robustness optimization against disturbance pulses in an early design phase of the system. Furthermore, these black box IC models can simplify the trouble-shooting when a qualification failed at a desired stress level. By simulation the detailed current and voltage distribution can be evaluated and hence critical current paths can be found and prevented.

5.2.6 Known gaps and issues of TBM

There are some known gaps and possible issues of the model architecture TBM. One possible gap is definitely the simplified thermal failure threshold. For characterization usually rectangular pulses (TLP) are used. During stress tests the waveform is usually not rectangular, but rather exponential decaying or completely arbitrary. Exponential decaying pulses typically have a higher power to failure respectively energy to failure than a rectangular pulse at the same pulse duration. This cannot be denied and is one possible source of inaccuracy of the failure threshold. The proposed model architecture is seen as a starting point which shall be further developed. For the time being the achievable accuracy for the failure point is sufficient. But an improvement with a comparable simple usability and high IP protection is desired for future development steps.

Moreover, the extensive use of switches and pulsed sources are a potential reason for convergence problems and long computation times due to discontinuities. The extensive use of RC elements to low-pass filtering these signals is one measure to prevent converge problems

by limiting voltage and current change rates (dv/dt and di/dt). A combination of several subcircuits to a complete IC model further increases the possibility of convergence problems and high computation times. Additional small inductors (typically $\approx$ a few pH) in series to the switches can help to improve the convergence of the circuit. Another possibility is to add capacitors in parallel to the switches or pulsed sources. Care has to be taken that no unintended LC circuit is formed which again has only poor convergence due to a possible ringing of this circuit.

There may be some more sources of potential convergence issues or gaps within the model which are not known by now. Additionally, it is also possible that some further transient effects has not been seen up to now which deserve to be included in the modeling methodology. The presented straight forward modeling methodology allows a model extension of further effects due to its modular and flexible architecture.

5.2.7 Application example of TBM

An application example of modeling one pin-combination of an IC is shown here. TLP measurements on package level are done to characterize the transient behavior and destruction limits at several pulse durations. The characterization measurements show a snap-back ESD protection element which dominates the transient behavior, see figure 5.7. It illustrates the measured quasi-static I-V-curves obtained by measurements (colored, solid lines) and simulation (black, dotted or dashed lines) with different pulse durations.

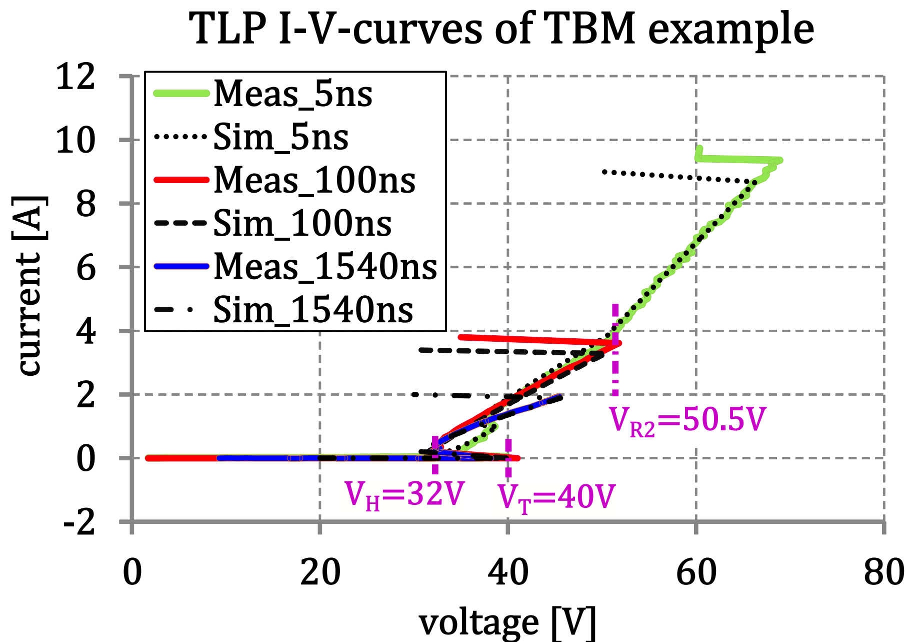


Figure 5.7: Comparison of TLP I-V-curves with different pulse widths obtained by measurements and simulations of an application example of TBM.

At short pulses ($5ns$ pulse width) the quasi-static I-V-curve shows a kink at roughly 50 V. Additionally, at low current densities there is conductivity modulation which leads to a higher dynamic resistance at these short pulse durationss. The 1540 ns TLP curve shows also a higher dynamic resistance, but in this case the reason is self-heating. Both effects are more clearly visible in the transient waveforms which are not shown here. At high current and voltage levels all curves show some kind of snap-back behavior, which indicates the thermal breakdown and hence the destruction point. For all pulse durations a good matching of measured and simulated curves is obtained including the destruction limits. The modeling approach is further validated with the system ESD tests to find the destruction limit. This pin-combination is tested with and without external components. In both cases a good agreement of measured and simulated destruction limits was found (± 20 %) [8], [36].

Further details about the parameter setting/fitting and application examples are provided in chapter 7. A detailed description of the parameter extraction flow is also provided there. Finally, the models of complete ICs are evaluated in terms of transient behavior and destruction levels both as stand-alone devices and combined with external devices.

5.3 Black box transient behavioral modeling for MOS transistors (TBM-MOS)

MOS transistors, especially high voltage DMOS transistors, show a quite unique transient behavior during ESD pulses. Because of that the generic model architecture TBM cannot reproduce their response to ESD pulses. This is the reason why a second generic model architecture is developed for MOS transistors called TBM-MOS. The details of the black box model are presented in this section.

5.3.1 Dynamic MOS channel current due to capacitive coupling from drain to gate

As seen from measurements high voltage DMOS transistors show a capacitive coupling from *drain* to *gate* [58]. This enables a significant channel current of the transistor during ESD events [59]. The gate controlling circuit has same finite resistance which discharges the gate capacitance with the time constant $\tau = R_{GS} * C_{GS}$, see figure 5.8. Therefore, the channel resistance increases during the pulse due to the declining gate voltage V_{GS}. Depending on the discharge time constant τ this behavior can or cannot be used for ESD protection. For very short time constants, e.g $\tau < 1$ ns, the gate potential is already below the threshold voltage V_{TH} before the ESD pulse really starts. By contrast, comparably large time constants, e.g. $\tau > 1$ μs, allow to shunt the complete ESD current pulse safely through the channel of the MOSFET. In between there is some not clear defined behavior. In this cases the MOS channel conducts current at the beginning of the ESD pulse but after the gate voltage is below the

threshold current conduction in the channel is no longer possible. Hence, the rest of the pulse needs to find an alternative path. This can be a dedicated ESD protection element in parallel to the MOS transistor or avalanche breakdown of the drain-bulk junction of the NMOS itself. It is a question of the device design if this avalanche breakdown is immediately destructive or it leads to a stable current conduction mode in ESD conditions up to a certain destruction limit.

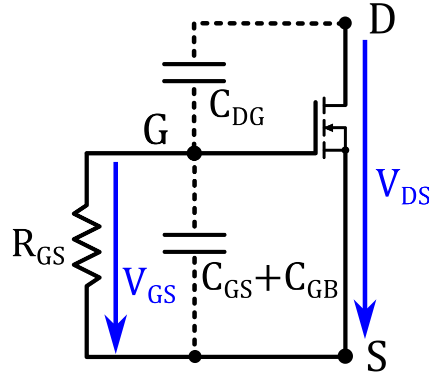


Figure 5.8: Equivalent circuit of a MOS transitor with the parasitic capacitances from *drain* to *gate* (C_{DG}) and from *gate* to *source* ($C_{GS} + C_{GB}$). Additionally a resistance from *gate* to *source* (R_{GS}) is shown which indicates the finite resistance of the gate-controlling circuit.

High voltage DMOS transistors are often optimized to conduct some pulsed avalanche current without destruction due to application needs. This current capability can be used for ESD protection. After the transient channel current has stopped due to the declined gate potential $V_{GS} < V_{TH}$ the ESD current can be further conducted in the avalanche mode within the DMOS. At a certain current density level at one pulse length the inherent npn-bipolar transistor is activated and immediately destroyed. Generally other types of MOS transistors are often optimized in such a way that the inherent bipolar transistor is able to conduct a certain ESD current without destruction. So they change from dynamic channel current into the bipolar mode to further conduct the remaining ESD current. To describe the dynamic channel current during ESD pulses a very basic MOSFET model for the saturation mode is used [30], see figure 5.9. A capacitive voltage divider is formed by C_{DG} and C_{GS} between the main terminals A and B of the model. The middle point is named gate G and connected via a resistor to the source terminal B of the model. The values of these three components are set with the respective parameters. In parallel to the capacitive voltage divider there is a current source I_{MOS} which models the channel current. The current is controlled by the gate potential $V(gate, B)$ and the drain-source voltage $V(A, B)$. Furthermore the parameters gain factor *kp* and threshold voltage $Vd0$ are used to fit the measured behavior. Again an ideal diode *D1* is used to prevent reverse current within the model.

This very basic model of MOS transistors is able to describe the dynamic channel current during ESD events without containing details about the transistor itself (e.g. device construction,

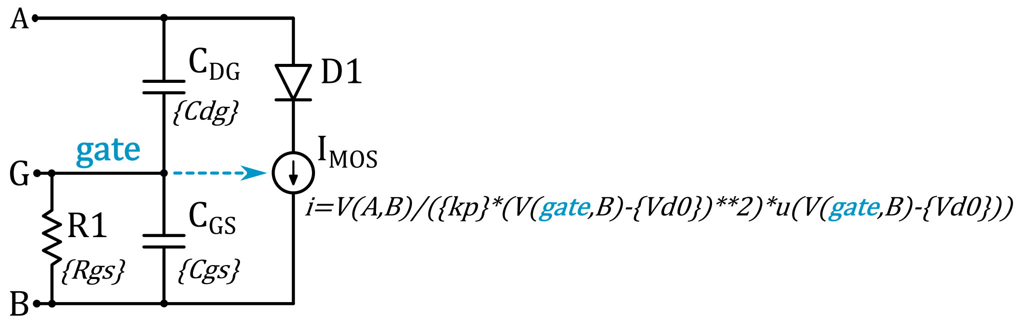


Figure 5.9: Circuit to model the dynamic coupling from *Drain* to *Gate* and the related channel current during ESD events.

area consumption, etc.). Additional effects need to be modeled with additional circuits/parts, like the avalanche breakdown behavior of HV DMOS transistors described in the following section.

5.3.2 Breakdown behavior at high voltage levels

As described beforehand HV DMOS transistors often show avalanche breakdown phenomena during ESD events. This breakdown behavior is dependent on the gate-source voltage of the DMOS transistor and hence dependent on the pulse duration for transistors with a fixed gate controlling circuit. As this behavior is not relevant in the functional range it is usually not implemented in the compact models typically used for functional modeling (e.g. BSIM).

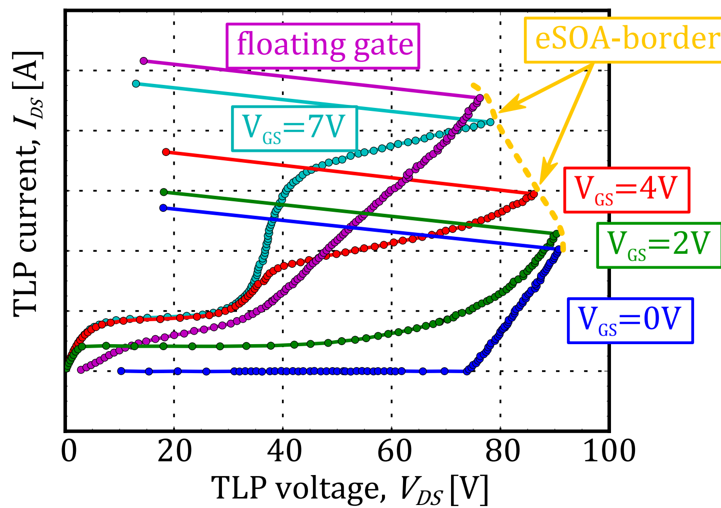


Figure 5.10: Typical eSOA of a HV DMOS transistor, i.e. TLP I-V-curves (I_{DS} vs. V_{DS}) at different gate voltages V_{GS}.

Generally, this breakdown behavior can be modeled with a switch based architecture compa-

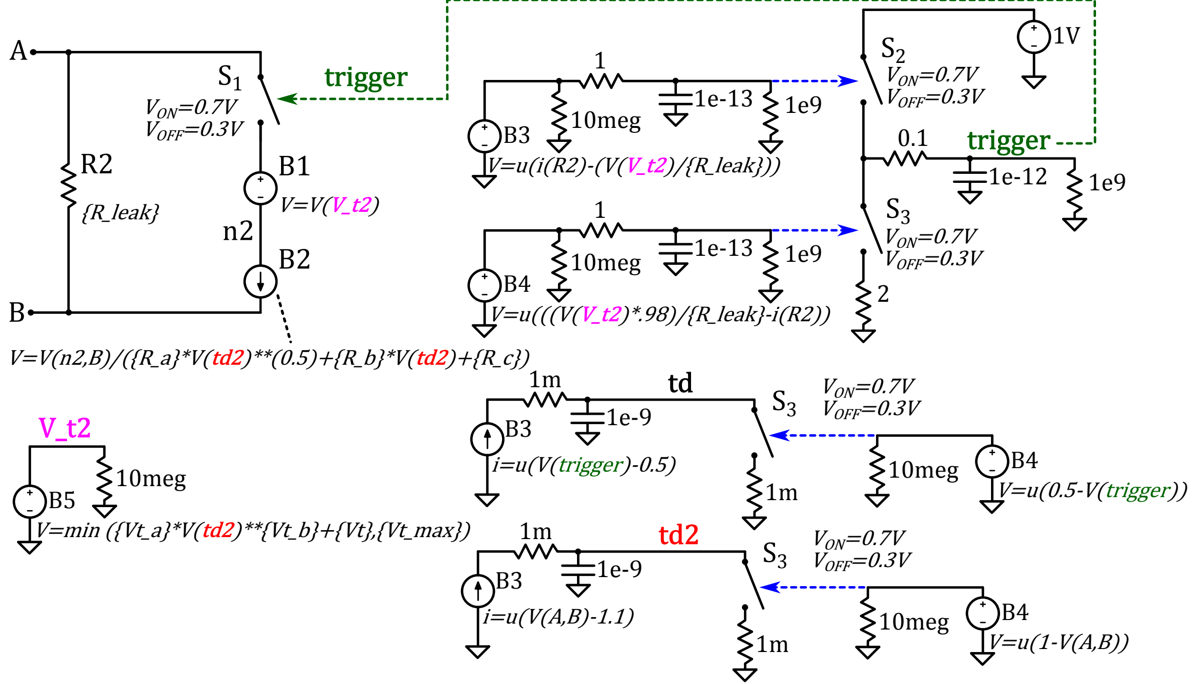


Figure 5.11: Basic schematic to model the breakdown behavior of HV DMOS transistors dependent on the pulse duration.

rably to the TBM described in section 5.2. The proposed model structure is illustrated in figure 5.11. However, the turn-on voltage (in this case breakdown voltage) needs to be described dependent on the pulse duration. Furthermore, the dynamic resistance is not dependent on the pulse energy but rather on the pulse duration as seen from measurements. There is not only one switch-on time as there are two main current paths. Two separate circuits to calculate the turn-on time are implemented to account for this. The circuit to measure *td* delivers the turn-on time of the breakdown current path. By contrast, the circuit for *td2* gives the current on-time for the whole model. It counts the time when a dynamic channel current is present as well as the case when breakdown current is flowing. Therefore, *td2* is used as time basis for the time variable breakdown voltage V_t2 (*B5*). This voltage increases with the time *td2* according to the parameter setting (Vt_a, Vt_b and Vt). The value is limited to Vt_max. The calculated voltage V_t2 is used for calculating the turn-on and turn-off points of the breakdown path done with behavioral sources *B3* and *B4*. Furthermore, the value is used for the series voltage source *B1*. This allows to model a pulse duration dependent breakdown voltage with simple tools. The simplicity of this solution also hides the physical details of the underlying effects which is often desired by the semiconductor manufacturers. The time dependent dynamic resistance is described with the behavioral source *B2*. To fit the measured resistance at different pulse durations the parameters R_a, R_b and R_c are used.

5.3.3 Destruction limits

For DMOS transistors the failure point is often related to the triggering of the parasitic bipolar transistor which is immediately destroyed after triggering. This activation of the bipolar transistor is related to the gate-source voltage and to the temperature of the drain-bulk junction. As in the products the MOS transistors always have a gate controlling circuit and hence a defined gate source voltage during ESD pulses the destruction limit is in first approximation solely dependent on the pulse power/energy. Therefore, the destruction limit modeling of TBM (section 5.2.4) can be used as well for TBM-MOS. Additionally, a critical current density is often found for very short pulses as onset of bipolar triggering [26]. This failure border can be modeled by an additional circuit in parallel to *B16*, *B17* and *B18* which initiates the change of *S16* and *S17* when this critical current is exceeded (see figure 5.5).

5.3.4 Generic model architecture of TBM-MOS

The combination of all above discussed components results in a black box model for MOS transistors suitable for ESD simulations on system level. The generic, black box approach allows to exchange IC models between IC vendors and system designers with a strong IP protection and hence enables ESD robustness optimization early in the design phase. The simplified schematic for the model architecture TBM-MOS is shown in figure 5.12.

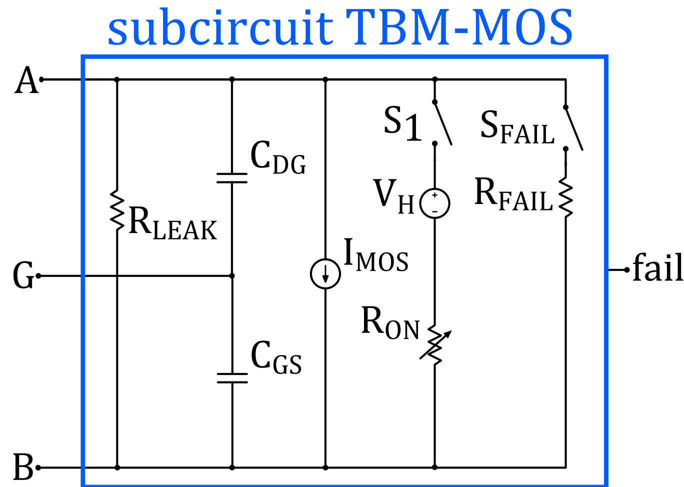


Figure 5.12: Simplified schematic of the TBM-MOS model architecture to describe the behavior of DMOS transistors during ESD events including typical destruction limits.

5.3.5 Known gaps and issues of TBM-MOS

The presented architecture of *TBM-MOS* is a first proposal and might be further optimized. Up to now there are no critical issues known for this model topology. A critical point of device

models is always possible numerical instabilities and convergence issues. The discontinuity of switches or functions within behavioral sources are a possible source of bad convergence. So combining a lot of these elements in one simulation can really cause troubles. Therefore, the presented model topology works well with a small number of placements in one transient simulation. But it might create convergence issues when a high number of those circuits (e.g. models for single elements of an IC) are placed in one simulation setup.

5.3.6 Application example of TBM-MOS

A smart power IC with a large DMOS as an output driver is chosen to show the accuracy of TBM-MOS. The DMOS transistor is connected to two pins with *drain* respectively *source*. Figure 5.13 shows the quasi-static I-V-curves for three different pulse durations. The measured values are plotted with colored, solid lines while the curves from simulation are plotted with black, dotted or dashed lines. For short pulses (20 *ns* and 100 *ns*) the dynamic channel current below 40 *V* is clearly visible. The 1540 *ns* curve shows no dynamic channel current, i.e. the gate voltage V_{GS} is already declined below the threshold voltage V_{th} for this pulse duration.

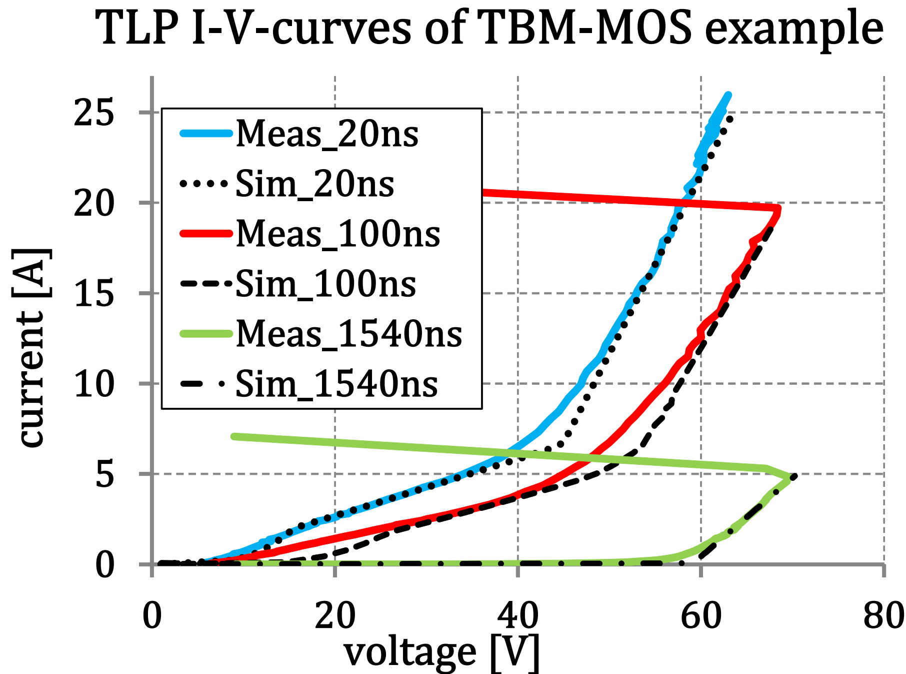


Figure 5.13: Comparison of TLP I-V-curves with different pulse widths obtained by measurements and simulations of an application example of TBM-MOS.

At high current levels all curves show a breakdown behavior with a kink in the I-V-curve. The short pulses have a lower on-set voltage of this breakdown behavior than the longer pulses. This is the time dependency of this breakdown voltage. Furthermore, the dynamic resistance of this breakdown behavior is increasing when going to longer pulse durations. Again measurement

and simulation show good matching for all three pulse lengths.

A complete ASIC with three pins was modeled with *TBM-MOS* and *TBM* for system ESD simulation. Together with the application specific external circuitry system ESD tests were done up to the destruction limit. The same procedure was also done in simulation to find the destruction limit indicated by the proposed modeling approaches. The destruction limit is evaluated for several pin-combinations and polarities. Again measured and simulated failure thresholds show good agreement ±20 %) [59].

Summary

This section presented two generic model architectures *TBM* and *TBM-MOS* which allows to describe the behavior of most silicon devices during ESD events. Both are capable of describing the major transient effects necessary for ESD simulations of certain device types. The destruction limits dependent on the pulse duration are also implemented. This enables the evaluation of a system's pulse robustness by simulation. The black box IC models show the detailed current distribution and voltage drops within the system. Furthermore, the model indicates if a certain stress level is likely to cause damage to the IC or not. This enables electrical stress simulation against disturbance pulses like ESD [15], [14], EFT [60], [19] or further disturbance pulses like [20]. An extensive use of simulations allows to optimize the system robustness against these pulses already during the design phase. It has to be noted that this approach requires a comparably high number of measurements with the packaged IC to get its transient behavior during pulsed stress. Depending on the desired coverage of stress pulse durations a high number of different pulse lengths is necessary for characterization up to the destruction limit.

The black box approach allows to exchange the models for complete ICs among system designer and IC vendor without disclosure of IP. The high degree of simplification enables quite compact IC models and hence short simulation runs on system-/PCB-level. The validity of the modeling approaches were shown on two application examples. With and without external circuitry the TBM and TBM-MOS are able to predict the failure level during system ESD tests with an accuracy of ±20 %. This is a really good value for system ESD simulations especially despite the high simplification level of the modeling approaches. Both modeling approaches have been presented at the EOS/ESD Symposium 2017 (TBM) [8] respectively 2018 (TBM-MOS) [59].

Compared to other published modeling approaches the proposed one is not fixed to one certain type of devices which allows the combination of several, different devices into one model structure. Moreover, modeling transient effects like self-heating and forward recovery is only rarely seen in literature. Especially the combination of all effects into one parametrized model architecture is new compared to the state of the art. All in all is to say, that the advantages

more than counterbalance the found drawbacks and hence this modeling approach is able to improve the robustness design of systems against disturbance pulses. Up to now the modeling methodology focuses on products manufactured in smart power technologies. With future work an extension to advanced CMOS nodes or discrete protection device technologies are feasible.

6 Generating IC-ESD models out of IC design data

As the measurement based model generation is quite time consuming and needs a completely manufactured IC, a methodology to generate the full chip behavior model (chip-TBM) out of IC data is desired. This chapter presents a methodology how these models can be generated out of the IC's schematic and layout data. This enables system simulation in an early design phase even before the silicon is processed. So the first improvement cycle of the IC in terms of electrical stress and ESD robustness can be made quite early. In a classic development cycle of electronic modules the ESD and EFT robustness evaluation is done at the very end during product qualification, see figure 6.1.

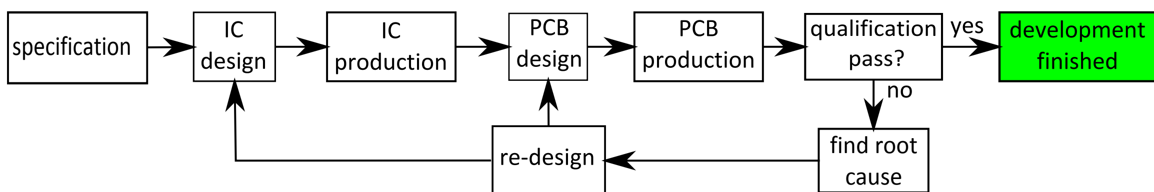


Figure 6.1: Classic development cycle for electronic modules.

In this late phase a re-design of an IC or the PCB has only very little options while it takes usually a huge amount of effort especially monetarily, see figure 6.2.

To give the designers more possibilities to improve the system robustness at low costs, system simulation should be done right after or even during design phase. If any weakness in the system is found, the system robustness can be optimized before the first prototypes are assembled. In figure 6.3 the improved development cycle is depicted. After the system robustness is optimized in the design phase, a fail during qualification is very unlikely to occur. This helps to effectively reduce the overall development time and costs.

The proposed development cycle might look costlier and longer because an additional system simulation step is included, but in fact the early and very short re-design loop without production steps helps to speed up the development process. Additionally, the design and optimization of the IC and PCB can be parallelized which can significantly reduce the overall development time.

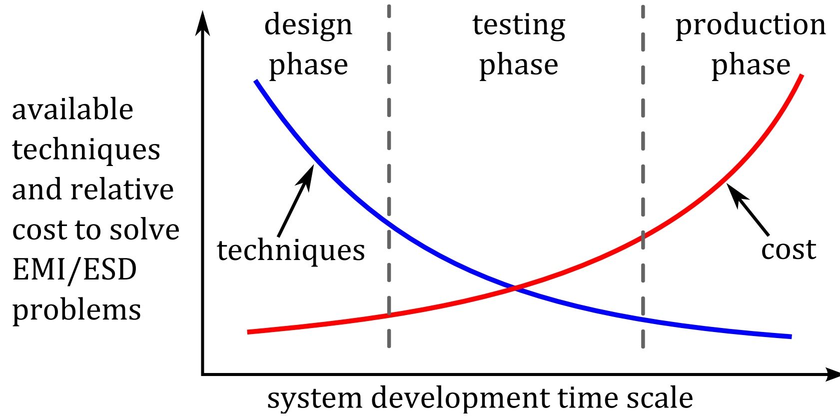


Figure 6.2: As system development proceeds, the number of available techniques to enhance EMC/ESD robustness goes down while the costs go up fast [61].

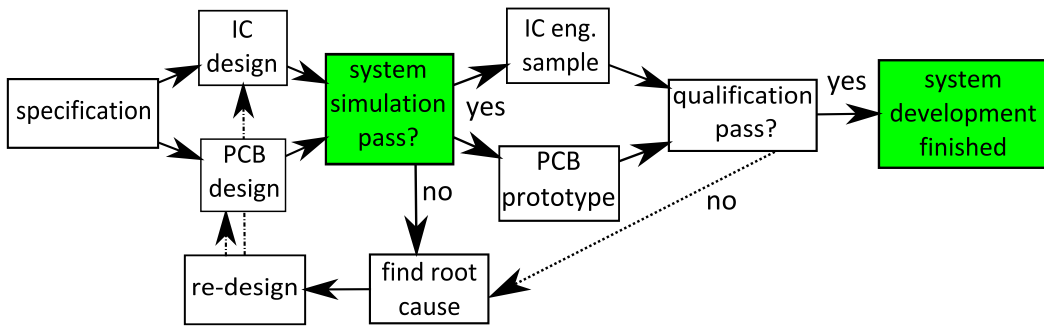


Figure 6.3: New development cycle for electronic modules with full system robustness simulation before production.

6.1 Methodology for generating full-chip behavioral models out of IC schematic and layout

What is necessary to generate the IC behavior model pre-silicon? The IC behavior during ESD or EFT stress is dominated by the behavior of the ESD protection network which is mostly consisting of dedicated ESD protection elements and self-protecting output drivers. These elements dominate the transient response to short pulses (ns to μs range) while the destruction limit is determined by both *protection elements* and *elements to be protected*, like core devices of the IC. A simplified schematic of an ESD protection scheme between *PinA* and *PinB* is shown in figure 6.4 to point out the difference of *protection device* and *device to be protected*. The ESD protection element is intended to draw the most ESD current i_{ESD} at a low voltage drop to safely protect the element(s) to be protected. The ESD stress is assumed to be from *Pin A* to *Pin B*. In this case the ESD protection is realized with a diode in reverse breakdown (from cathode C to anode A). This can be a zener-diode or a high voltage breakdown diode. The MOS-transistor is in parallel to the protection diode with drain D to source S. In addition,

there is the IC core in parallel to them.

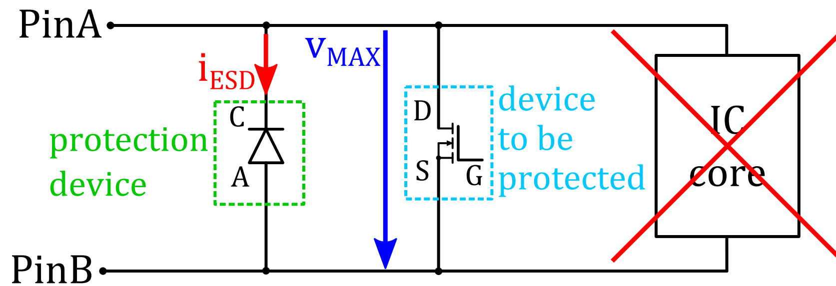


Figure 6.4: Simplified ESD protection scheme between *Pin A* and *Pin B* with a diode as an ESD protection element and a MOS-transistor as a device to be protected.

As ESD pulses can be very short (only a few *ns*) and can go up to very high currents (tens of *A*) also the inductance and resistance of the on-chip wiring can have a significant influence. Moreover, the parasitic inductance and capacitance of the package have an influence on the behavior of the chip in case of fast transients. So they also need to be integrated in the transient behavior model.

The general modeling flow is presented in figure 6.5. The first step to generate a full-chip transient behavior model is to reduce the IC schematic down to only these elements which contribute significantly to the transient behavior and destruction limits. This can be done by a transient simulation, a topology check, identification of markers or by an experienced engineer. This step shall enable a compact model while the necessary transient behavior is fully covered. This can be accomplished by extracting the relevant current paths for fast transients to replicate the transient behavior on the one hand. While on the other hand the destruction limits of all endangered devices, both *protection device* and *device to be protected*, are necessary to correctly replicate the failure threshold of the complete IC. Furthermore, the on-chip wiring can influence the transient behavior as well, mainly the ohmic resistance and inductance of the metal interconnects. When the IC-layout is finished these parasitic values can be extracted directly from the layout. If the layout is not finished yet, there are usually some ESD design rules with a maximum allowed resistance and/or inductance in a certain path which can be used as worst case for the transient behavior model. The last thing to add are the parasitic resistance, inductance and capacitance of the IC-package. All these elements together form the full-chip transient behavior model.

6.1.1 Reducing the full-chip schematic

As the complete schematic of an IC is much too complex for transient stress simulation, the schematic of the IC needs to be reduced. To model the transient behavior during high current injection correctly it is not necessary to model the core of the circuit in detail. Most of the current is flowing through the ESD protection devices, therefore they dominate the transient

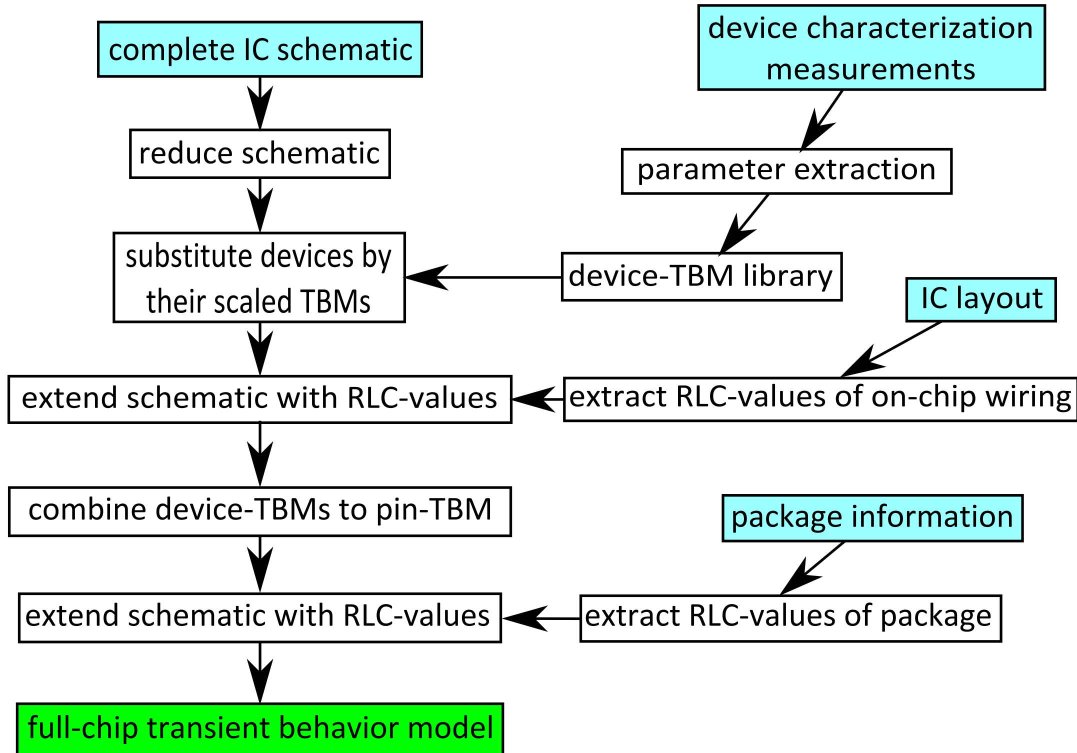


Figure 6.5: Proposed model generation flow for extracting full-chip transient behavior models out of layout and schematic of an IC.

behavior together with the nearest elements to be protected. There are several approaches to reduce the full-chip schematic. The first approach can be a manual selection of the necessary devices conceivable. This approach might be time consuming, but has the advantage that an ESD expert can judge which elements will conduct the ESD current. There are several ways how the devices identification can be automated. One possibility is to add a marking to all ESD devices in the library and pick the marked devices from the schematic. Another solution is to determine the current path by simulating either transient or static. In this case all devices which conduct a notable current (e.g. $I_{device} > 10\ mA$) are selected for the transient behavior model. All of these solutions have some advantages and drawbacks which are summarized in table 6.1. Once the relevant devices are identified, all device models in the schematic are substituted with their transient behavior model. These selected devices are called *ESD devices* in the following sections.

The next step is to identify all endangered core devices which are in parallel to the ESD devices and see the voltage drop over the ESD devices while they conduct current. These *endangered devices* should be modeled high-ohmic with a voltage threshold as a failure criterion. This ensures that also the failure mechanism of an excessive voltage drop over a core device is integrated in the model. A higher accuracy of the failure level is reached when these elements are also modeled with their transient behavior.

Table 6.1: Schematic reduction approaches

Approach	**Advantages**	**Drawbacks**
Manual selection	• Expert judgment • Precise	• Time consuming • Error-prone
Marker based	• Automatable • Fast	• Markers needed • Only ESD protection devices
Static current distribution	• Automatable • Fast	• Need for static analysis • Transient ≠ static
Dynamic current distribution By transient simulation	• Automatable • Precise	• Comparably slow • High computing power needed

Right now the manual selection process is seen as the best option as it is the most precise one. The involvement of a human makes it error-prone, but validation procedures like the four-eyes principle can overcome this drawback. The additional effort for this task is expected to be adequately low because the ESD engineer has to completely evaluate the ESD protection concept and endangered devices at a certain point during IC development. In this case the classification of ESD protection devices and endangered devices is already existing and can be exploited. For future developments the automation of the device selection process is definitely the task with the highest priority. One promising approach can be a combined solution. First of all, a transient simulation for the respective pin-combination of interest is started with a pulsed stress applied, e.g. TLP pulse or system ESD pulse. All current paths with a significant portion of the pulse current (e.g. $I > 10\ mA$) are taken/marked as ESD protection paths/devices and later on transferred to the reduced netlist/schematic. In a second step a DC voltage ramp is applied to this pin-combination. At a certain level some devices will indicate their destruction limit. These devices are taken/marked as devices to be protected as they are endangered by the voltage drop over ESD protection devices.

6.1.2 Library generation of transient behavior models

In order to extract a full-chip model out of schematic and layout, behavioral models of the ESD protection elements need to be available beforehand. A good way is to generate a library of transient behavior models of ESD protection elements and self-protecting elements. The single models shall be generated out of stand-alone test structures without any parasitics or additional devices to replicate really the transient behavior and destruction limit of the element itself. A methodology to build transient behavior models is pointed out in chapter 5. The effort for characterizing and modeling the transient behavior needs to be done for each device of a technology which can conduct a notable part of the current during an ESD event. This needs to be done only once for a technology like the characterization and modeling of the devices

in the operation range. Ideally, the transient behavior models are scalable in all parameters depending on the real device geometry. Additional to the dedicated ESD protection devices the devices with self-protecting capabilities need to be modeled. Furthermore, the devices which can be parallel to the main ESD current path are necessary to be characterized and modeled. The goal of this extensive library is to go through the schematic of a chip and identify the main ESD current paths between the single pins. All the devices along this current path have to be superseded by their transient behavior model.

6.1.3 Scaling of TBM parameters for area scaling of silicon devices

Usually the devices within a product are not the same size as they were on the test chip which was used to build the respective TBM. Therefore, the TBMs need to be scaled to match the device size within the product. There are parameters in the TBM which do not depend on the device size like V_T and V_H. By contrast, other parameters, e.g. R_{ON} and P_{FAIL}/E_{FAIL}, are dependent on the active area of the device. The functions for R_{ON} and P_{FAIL}/E_{FAIL} with their respective parameters are shown in equations (5.6), (5.7) and (6.1). Although the fitting parameters for E_{FAIL} (E_a, E_b, E_c and E_d) and P_{FAIL} (P_a, P_b, P_c and P_d) can be scaled with the device width, it would be more convenient to have a table with the failure current and voltage at certain pulse durations. With this table it is also easier to calculate the failure points for a few elements in series. When this step is successfully done, the parameters for the fitting functions of P_{FAIL} and E_{FAIL} can be fitted afterwards. An example for such a table described above is given in table 6.2.

Table 6.2: Suggested parameters for failure points of a device

pulse length td $[\mu s]$	**0.01**	**0.05**	**0.1**	**0.5**	**1.0**	**1.5**
failure current I_{t2} $[A/m^2]$	29.1	18.6	12.2	2.8	2.2	1.9
failure voltage V_{t2} $[V]$	156	135	117	80	74	71
failure power P_{FAIL} $[W]$	4540	2511	1427	224	163	135
failure energy E_{FAIL} $[\mu J]$	45	126	143	112	163	202

For devices size scaling the R_{ON} is inversely proportional to the device active area. This means the bigger the device is, the lower the resistance gets. The parameters R_a and R_c need to be scaled inversely proportional to the total device size. The calculation of R_b is not that easy, but when R_b is set to a fixed value, e.g. $R_b = 0.45$, from the beginning this problem is solved. This value was found to fit well to the experimental data for different device types. The scaling of the fitting parameters for P_{FAIL}, E_{FAIL} and R_{ON} is just linear algebra of polynomial equations, see equations (6.2) to (6.4). The scaling of the residual parameters of the TBM is accordingly.

$$R_{ON} = R_a \cdot energy^{R_b} + R_c \quad (6.1)$$

$$y_1(x) = a_1 \cdot x^2 + b_1 \cdot x + c_1 \quad (6.2)$$

$$y_2(x) = a_2 \cdot x^2 + b_2 \cdot x + c_2 \quad (6.3)$$

$$y_1 + y_2 = a_1 \cdot x^2 + b_1 \cdot x + c_1 + a_2 \cdot x^2 + b_2 \cdot x + c_2 = (a_1 + a_2) \cdot x^2 + (b_1 + b_2) \cdot x + (c_1 + c_2) \quad (6.4)$$

6.1.4 Extracting parasitic values of on-chip wiring from IC layout

As ESD pulses on system level can have a first peak of several ten A with a risetime below one ns even inductances of one nH and below can create voltage drops which can destroy devices within the chip. Therefore, it is necessary to extract the inductance of the on-chip wiring. Furthermore, the very high currents can create a significant ohmic voltage drop along the metal lines. So they are also necessary for the full-chip model and need to be extracted from the IC layout. Alternatively, the maximum allowed resistance and/or inductance for a certain path (e.g. the main ESD path) can be taken from the ESD design rules if available. This enables a full-chip TBM even before the IC layout is finished. Extracting of on-chip wiring parasitics is not a new task. In fact, there are several commercial software tools available which can extract them from the IC layout. The resistance of a metal trace R can be easily calculated from the specific resistance of the material ρ, cross sectional area A and length of the trace l, see equation (6.5). The specific resistance is known for a certain material. Cross sectional area and trace length are taken from the IC layout for each interconnect segment.

$$R = \rho \cdot \frac{l}{A} \quad (6.5)$$

As the metal layers of the on-chip wiring can be seen as microstrip or embedded microstrip lines the corresponding formulas can be used to calculate the parasitic inductance (equation (6.6)). Need for updated formula with a reference (EMC or RF book, microstrip line theory).

$$L = 2 \cdot 10^{-7} \cdot ln\left(\frac{5.98 \cdot H}{0.8 \cdot W + T}\right) \quad (6.6)$$

6.1.5 Combining several elements into one model

One big advantage of pure behavioral models like presented in section 5.3 [8], [36] is that several different elements can be combined into one single model. For example for several elements in series the trigger voltages and transient resistance can be simply added like depicted in figure

6.6. If there are not only elements in series but also in parallel, they can be combined into one TBM equally as the generic TBM offers several main current paths in parallel. An example is given in figure 6.7. This allows quite compact models of the complete IC while the IP of the IC vendor is very effectively protected as the single ESD protection elements are no longer visible as well as the ESD protection concept can be hidden.

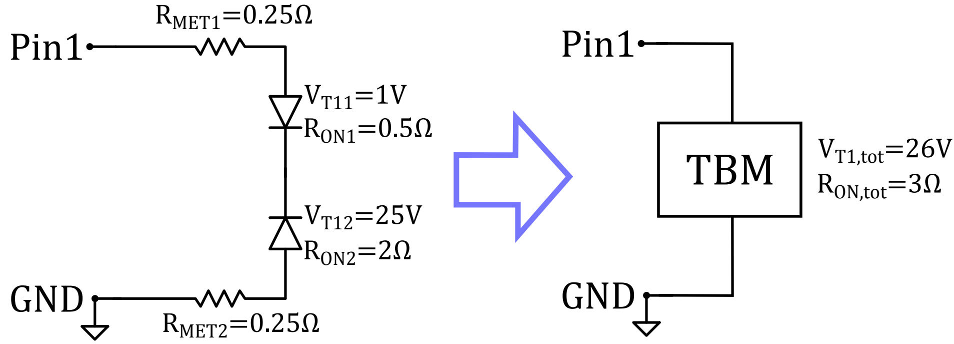


Figure 6.6: Combining several elements in series into one TBM between two pins of an IC.

The calculation of $R_{ON,tot}$ and $V_{T1,tot}$ is shown on this example (figure 6.6) with equations (6.7) and (6.8). The parameter calculation for the second example in figure 6.7 is accordingly.

$$R_{ON,tot} = \sum R_i = R_{met1} + R_{on1} + R_{on2} + R_{met2} = 0.25\Omega + 0.5\Omega + 2.0\Omega + 0.25\Omega = 3\Omega \quad (6.7)$$

$$V_{T1,tot} = \sum V_{T,i} = V_{T11} + V_{T12} = 1V + 25V = 26V \quad (6.8)$$

The lowest failure current I_{T2} of the series elements defines the destruction limit of the complete chain. With this failure current and the voltage drop at this current the failure power of the complete chain can be calculated. If this procedure is done with several pulse lengths, the power to failure respectively the energy to failure border for different pulse durations can be obtained. The failure points for energy and/or power with respect to pulse duration need to be fitted with the E_{FAIL} respectively P_{FAIL} according to [8], [36].

For parallel elements the first failing device is the one with the lowest V_{T2} which defines the destruction limit of the parallel devices. To get the power to failure P_{FAIL} all currents through the parallel branches at this voltage drop need to be summed up and multiplied with this voltage drop. The energy to failure E_{FAIL} is found by multiplying P_{FAIL} with the pulse duration td. For each combination of several elements a new table compared to table 6.2 is created and the fitting of P_{FAIL} and E_{FAIL} can be done to get the parameters for the TBM. Additionally, the setting of trigger voltages needs to be done carefully for parallel elements. Like shown in figure 6.7 the $V_{R2,tot}$ is not equal to V_{T12}, but higher due to the additional voltage

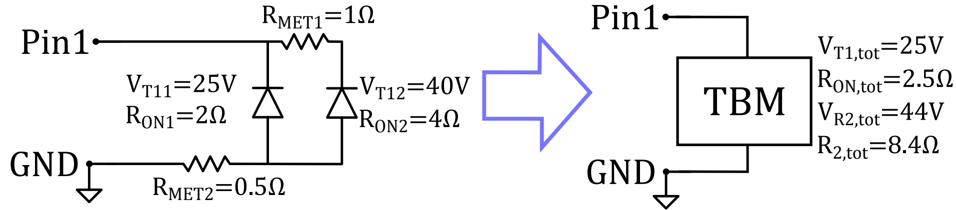


Figure 6.7: Combining several elements in series and parallel into one TBM between two pins of an IC.

drop over R_{MET2} just below V_{T12}. Alternatively the combination of TBMs can be done with transient simulations with different pulse lengths of rectangular pulses between the two pins of interest. The parameters for the single TBM between these pins can be extracted from the simulation results. This procedure is similar to doing TLP measurement with the complete IC and generating an IC-TBM out of these data.

6.1.6 Extracting parasitics of IC package

The parasitics of the IC package also influence the transient behavior. Inductivity and capacity are damping the ESD pulse on the way to the silicon chip. The parasitic inductance and capacitance can either be determined by a S-Parameter measurement or can be calculated from the physical construction. This effort is only once necessary for a certain package type. Usually, these values are already available for IBIS models or other system simulation purposes.

6.1.7 Constructing a transient behavior model for a complete IC

To get the full-chip transient behavior model all the above described elements have to be put together in the correct way. Starting from the reduced netlist with the transient behavior models of the single devices the on-chip wiring parasitics are included between the devices. The result is the complete chip transient behavior model. If the package parasitics are also included, the full-chip transient behavior model is complete. An overview of the single components for the IC-TBM is depicted in figure 6.8.

6.2 Example 1: Sensor ASIC

This section presents the proposed modeling methodology on a product to proof the applicability to complete ICs. An ASIC with three pins is chosen as device under test (DUT) which was well investigated in terms of transient behavior and ESD robustness by the author beforehand [8] and [36]. This means a sufficiently large number of TLP and GUN measurements on the complete IC are present to verify the proposed IC model with measurement data.

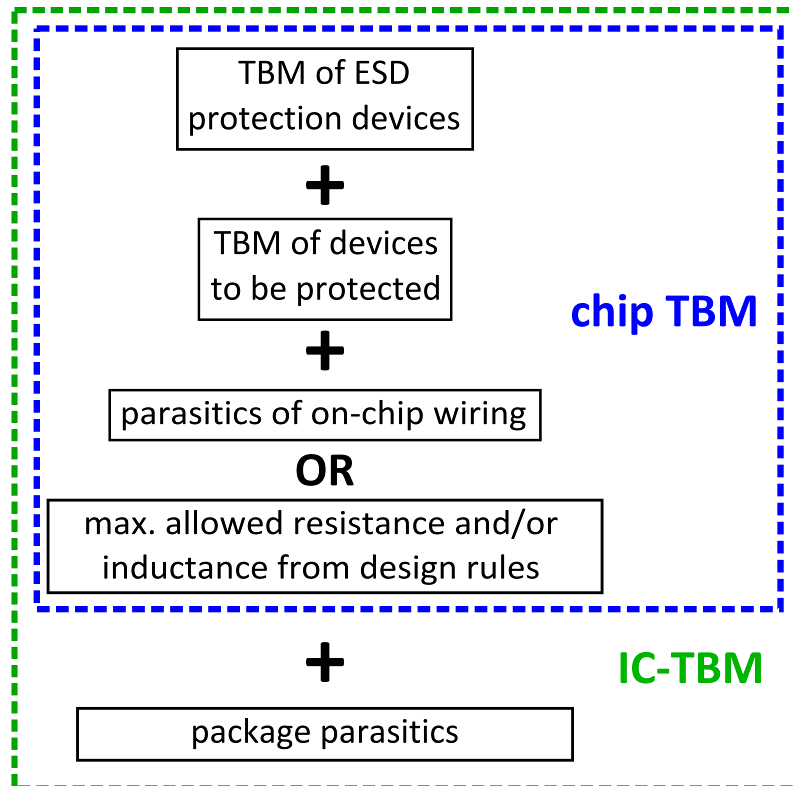


Figure 6.8: Constructing the full-chip transient behavior model for a complete IC.

6.2.1 Basic structure of the product

The first step is to find out all necessary circuit elements of the IC for the chip-TBM. As up to now the manual device selection process is the best suitable solution this is chosen for this DUT, so all necessary devices for the chip-TBM are manually extracted from the complete IC schematic.

The reduced schematic of the IC is shown in figure 6.9. In total, there are three ESD protection elements and seven elements to be protected including two resistors. The reduced schematic also contains a metal resistance extracted from the layout. In the other current paths the metal resistances are expected to be negligible and are therefore not included in the chip-TBM.

6.2.2 Generate TBM library and replace devices by TBMs

As all the necessary elements were identified in the first step these elements are measured as stand-alone devices on a test chip with TLP as described beforehand. Out of these measurements TBMs for the single devices are generated. For the sake of simplicity self-heating was neglected and only the TLP measurements with 5 ns pulse length were considered for modeling. All

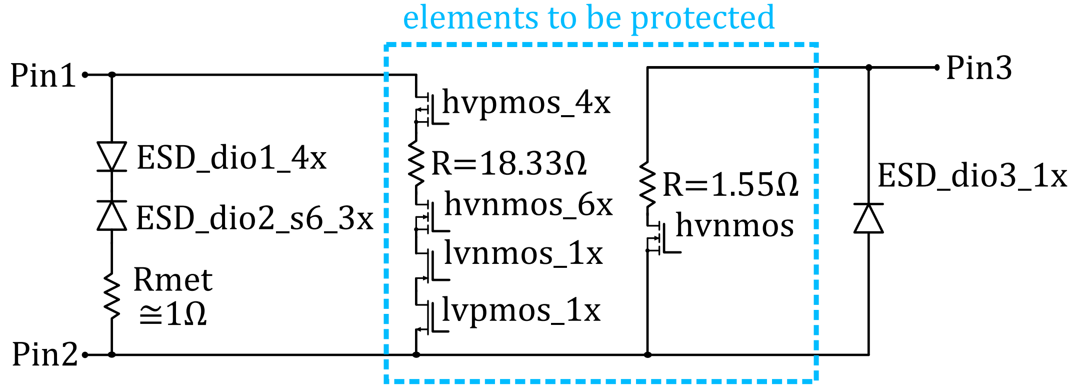


Figure 6.9: Manually reduced schematic of DUT 1 with all necessary devices for the chip-TBM.

individual devices in the reduced schematic are denoted with the size factor compared to the respective models in the TBM library, e.g. $dev1_4x$ means $dev1$ in the product is four times bigger than the model in the TBM library. This means when the device model from the TBM library is taken, it needs to be scaled with a factor of four. Scaling in area influences the dynamic on-resistance and the destruction limit.

6.2.3 Extraction of parasitic resistances from on-chip wiring

All on-chip metallization is assumed to be negligible except the wiring in one main ESD current path as it differs significantly from the testchip layout. The extraction with sheet resistances and geometrical data of the metal connections gave a resistance of roughly 1 Ω which was integrated into the chip-TBM. Due to comparably high cross sectional areas of the metal traces the inductance of them is neglected as they are expected to have minor impact on the transient behavior.

6.2.4 Combining several elements into one TBM

As pointed out in section 6.1.5 with a generic model architecture several elements can be combined into one model to reduce model complexity and protect the chip design. For this IC dedicated TBMs were created for the ESD protection devices and the devices to be protected for each pin combination respectively. The resulting chip-TBM is schematically shown in figure 6.10.

Between $Pin1$ and $Pin2$ there are two separated current paths, see figures 6.9 and 6.10. The first one close to the pins is the dedicated ESD current path with two HV-breakdown diodes in back to back connection.

The second path with the devices to be protected contains two PMOS and two NMOS transistors in stacked configuration with some series resistance (figure 6.9). For this pin-

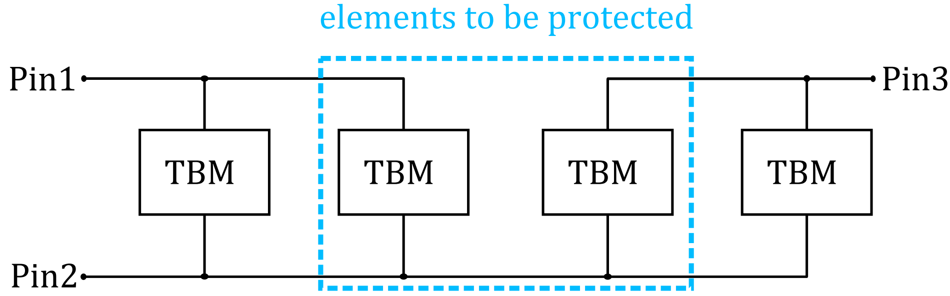


Figure 6.10: Model architecture of the chip-TBM of the DUT.

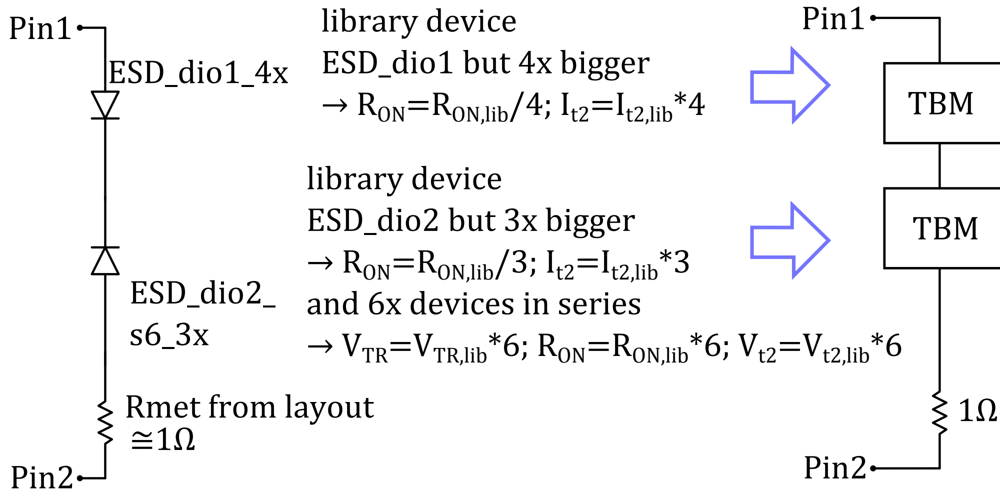
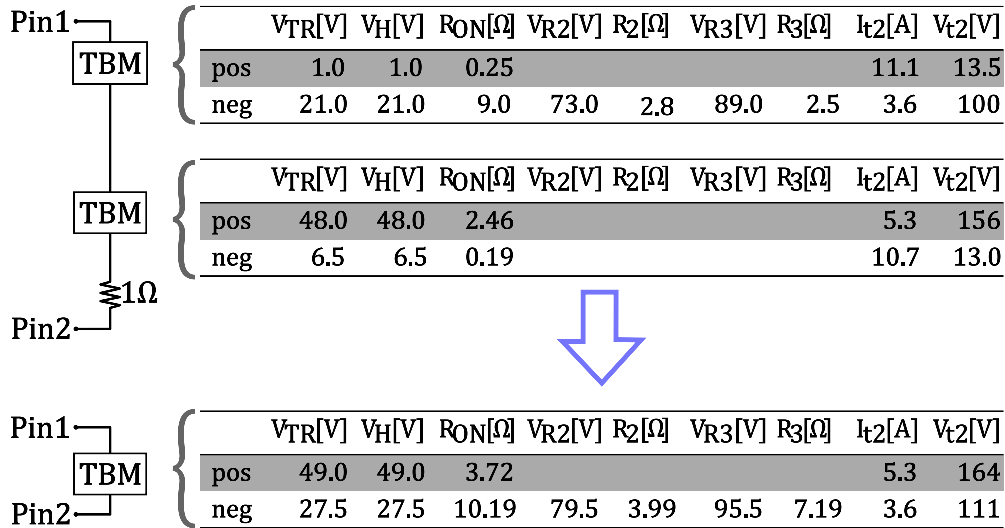


Figure 6.11: Schematic sketch of superseding nominal device models with scaled TBM models at the ESD protection path between Pin1 and Pin2 of the DUT.

combination the modeling flow for TBM scaling and device combination into one model is shown exemplary. For the dedicated ESD path the TBM scaling is shown in figure 6.11. As only one pulse length is used for the TBMs the calculation of the TBM parameters for this series connection is as follows:

All the parameters for the combined TBM are determined like described in section 6.1.5. A short summary of this procedure is given in figure 6.12. Note that for each polarity of a pin combination a dedicated TBM is generated. To make the graphics simpler to read each TBM box actually stands for two TBMs for positive and negative polarity respectively. The residual pin-combinations and current paths were processed accordingly. As found out earlier with this DUT physical fails often occur in the devices to be protected in the ESD time domain. Therefore separate TBMs were created for the intended ESD current and the devices to be protected for each pin-combination, see figure 6.10.



	V_{TR}[V]	V_H[V]	R_{ON}[Ω]	V_{R2}[V]	R_2[Ω]	V_{R3}[V]	R_3[Ω]	I_{t2}[A]	V_{t2}[V]
pos	1.0	1.0	0.25					11.1	13.5
neg	21.0	21.0	9.0	73.0	2.8	89.0	2.5	3.6	100

	V_{TR}[V]	V_H[V]	R_{ON}[Ω]	V_{R2}[V]	R_2[Ω]	V_{R3}[V]	R_3[Ω]	I_{t2}[A]	V_{t2}[V]
pos	48.0	48.0	2.46					5.3	156
neg	6.5	6.5	0.19					10.7	13.0

	V_{TR}[V]	V_H[V]	R_{ON}[Ω]	V_{R2}[V]	R_2[Ω]	V_{R3}[V]	R_3[Ω]	I_{t2}[A]	V_{t2}[V]
pos	49.0	49.0	3.72					5.3	164
neg	27.5	27.5	10.19	79.5	3.99	95.5	7.19	3.6	111

Figure 6.12: Combining several elements of the ESD protection path between Pin1 and Pin2 into one TBM.

6.2.5 Verification of the chip-TBM with measurements

In the end of the day it is of interest how good the models are matching with the real world, in this case measurements. Firstly, for ESD protection devices a comparison of TLP measurements and simulations can show if the dynamic behavior is replicated by the model. As this first DUT was treated in a simplified manner, only taking the $5ns$ TLP characterizations as basis for the models, this $5ns$ quasi-static TLP-I-V curve obtained by measurements and simulations is compared (figure 6.13). As it can be seen in the graph the chip-TBM matches well with the measurements.

Even more interesting for the system designers is the prediction accuracy of the system ESD robustness with the chip-TBM. As this DUT was well investigated by the authors beforehand it is known that this IC is sensitive on the PCB layout if the combination $Pin1$-$Pin2$ is protected with an external capacitor of 47 nF. As this sensitivity is linked with the first peak of the GUN pulse this simplified chip-TBM should be able to predict the system ESD robustness of the two different PCB variants. In a previous work a TBM for the complete IC was created based on measurements with the complete IC within the package [8]. System simulations were done to obtain the ESD robustness level according to [36]. The results are summarized in table 6.3 below.

The results show that the proposed methodology is able to create IC models which can predict the system ESD robustness with acceptable accuracy. The simulation results are a bit less accurate compared to the resource intense approach with creating IC models from characterization measurements with the complete chip. The deviation is only one simulation step size and the chip-TBM is not fully detailed, therefore this little deviation is acceptable.

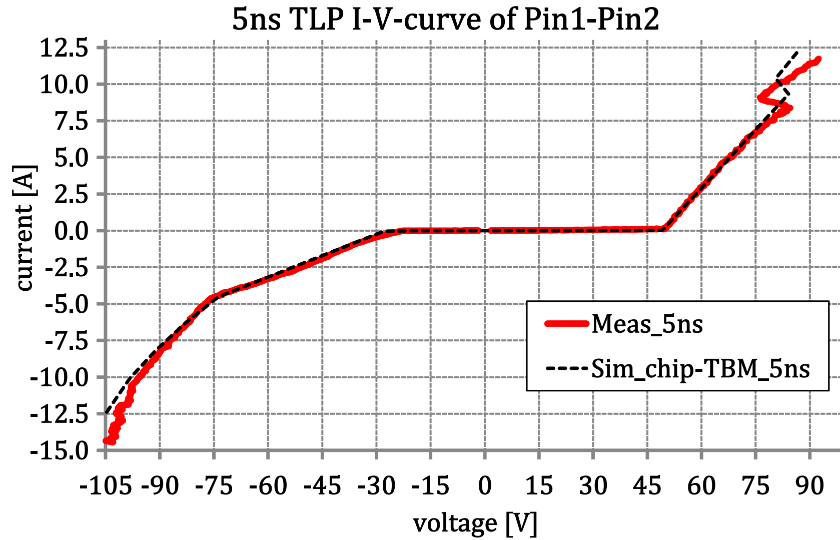


Figure 6.13: Quasi-static 5*ns* TLP-I-V curve of *Pin1-Pin2* obtained by measurements (red line) and simulation (black, dashed line).

Table 6.3: System ESD robustness with an external 47 *nF* capacitor

ESD robustness	PCB 1	PCB 2
measurements [36]	18.8 *kV*	12.2 *kV*
simulation (old) [36]	16.5 *kV*	12.5 *kV*
simulation (NEW)	16.0 *kV*	13.0 *kV*

The efforts and benefits of the proposed approach compared to previous work are summarized in table 6.4. Generally, it is to say that this methodology is feasible and can make the process to generate IC models for system ESD and electrical stress simulations much more easy.

6.3 Example 2: BCD communication IC

A second IC is chosen to further validate the proposed methodology to generate ESD models from complete ICs out of their design data. For this application example a discrete communication IC for automotive applications is chosen to validate the proposed methodology in full detail. The used communication bus is a differential one, this means two wires are used to transmit the signals (*IO1* and *IO2*) and the difference of both carries the transmitted information. The differential bus concept creates a high robustness against electromagnetic interferences and ensures high communication quality in a harsh environment. Therefore, this communication bus is widely used within cars. The interface pins (*IO1*) and (*IO2*) are routed to the PCB connector and hence relevant for system level ESD robust design.

Table 6.4: Efforts and benefits to generate the IC ESD models with different approaches

Approach	Efforts	Benefits
Old work [8], [36], section 5.2.7	• ≈ 4 engineering weeks • ≈ 100 packaged ICs	• Very accurate model
TBM-library not available	• ≈ 2 engineering weeks • ≈ 20 devices on test-chip	• Accurate model • TBM-library can also be used for further products
With TBM-library available	• ≈ 0.5 engineering weeks • No measurements needed	• Accurate model • Possibility of automation

6.3.1 Basic structure of the IC

Again the necessary devices of the complete chip schematic are selected manually. The resulting reduced schematic is shown in figure 6.3.1. The selected pins of the IC are all pins which are directly routed to the ECU connector (*IO1*, *IO2* and *VSS* resp. *GND*) and the supply pin which is connected to a capacitor externally (*VDD*). Due to the capacitor a significant ESD current can flow through this pin as it is "virtually grounded" through the capacitor for fast transients.

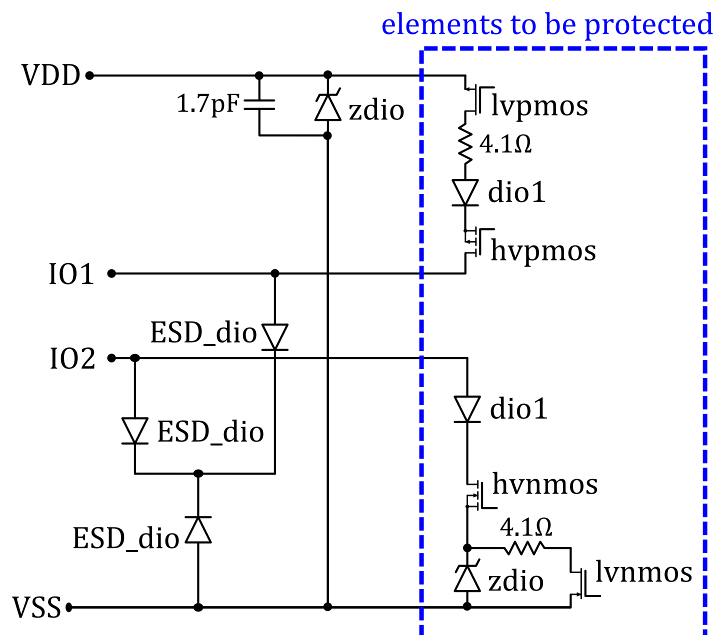


Figure 6.14: Manually reduced schematic of DUT 2 with all necessary devices for the chip-TBM.

6.3.2 Generate TBM library and substitute devices by their respective TBMs

As this IC is manufactured in a different BCD technology than DUT 1 from section 6.2 again a TBM library of all necessary elements is required. Therefore, all devices contained in the reduced schematic (figure 6.9) are measured as stand-alone devices on dedicated test-chips by means of TLP. Based on these measurements with various pulse durations the necessary parameters for individual TBMs respectively TBM-MOS are extracted. Exemplary this procedure is shown on a HV avalanche breakdown diode (*ESD_dio*) and on one HV n-channel DMOS transistor (*hvnmos*). All other device models are created accordingly.

TBM parameter extraction for a HV avalanche breakdown diode

High voltage avalanche diodes are used in this IC to protect the HV pins against ESD pulses. Therefore, the finding and setting of parameters for the TBM is shown on this example. First of all, the trigger voltage is extracted from TLP I-V-measurements with several pulse lengths ($V_T = 48V$). As a pure avalanche breakdown is not showing a snap-back phenomenon the holding voltage parameter is set equally ($V_H = V_T = 48\ V$). The R_{ON} parameters $R_a = 1574$ and $R_c = 5.662$ are found with Matlab to fit the measured behavior while R_b is set to a fixed value of $R_b = 0.5$. A fixed value of $R_b = 0.5$ does not reduce the fitting accuracy, but makes the modeling easier as $R^{0.5} = \sqrt{R}$ and the square root function is defined in Spice2g6. This enables the use of the model in all SPICE tools based on Berkeley Spice2g6.

This avalanche breakdown diode shows a special behavior in terms of reduced R_{ON} above a certain current density which was reported by Cao et.al. [62]. So the turn-on threshold for a reduced R_{ON} is a certain current $I_{R2} = 2.5\ A$ instead of the typically used voltage threshold. The threshold value is extracted from several quasi-static I-V-curves with a wide range of pulse lengths. It is also more clearly visible if the change in dynamic R_{ON} is current or voltage driven at different pulse durations. By contrast, the parallel resistance R_2 is extracted from the 5ns TLP I-V-curve only to avoid influences of the self-heating within the initial R_{ON}.The failure points I_{t2} and V_{t2} are extracted for several pulse lengths from the TLP measurements.

To detect a physical destruction the leakage current is measured at the rated AMR voltage level after each TLP pulse. The criterion for classification is an increase of more than 10 % of the leakage current. From the failure points I_{t2} and V_{t2} the power-to-failure P_f values can be calculated for the respective pulse duration *td*. With this data the fitting parameters P_a, P_b, P_c and P_d can be found.

It has to be denoted that for automated fitting, e.g. with Matlab, a weighting (e.g. $weight = 1/P_f$) is beneficial for the fit accuracy. This way the single measurement points have all the same influence on the fitting accuracy, no matter how different their values are. Otherwise high values have an high impact on the fitting parameters while the low values can have a big mismatch to the fitting function as only the absolute difference is taken into account. The proposed weighting overcomes this issue and more or less the relative deviation between

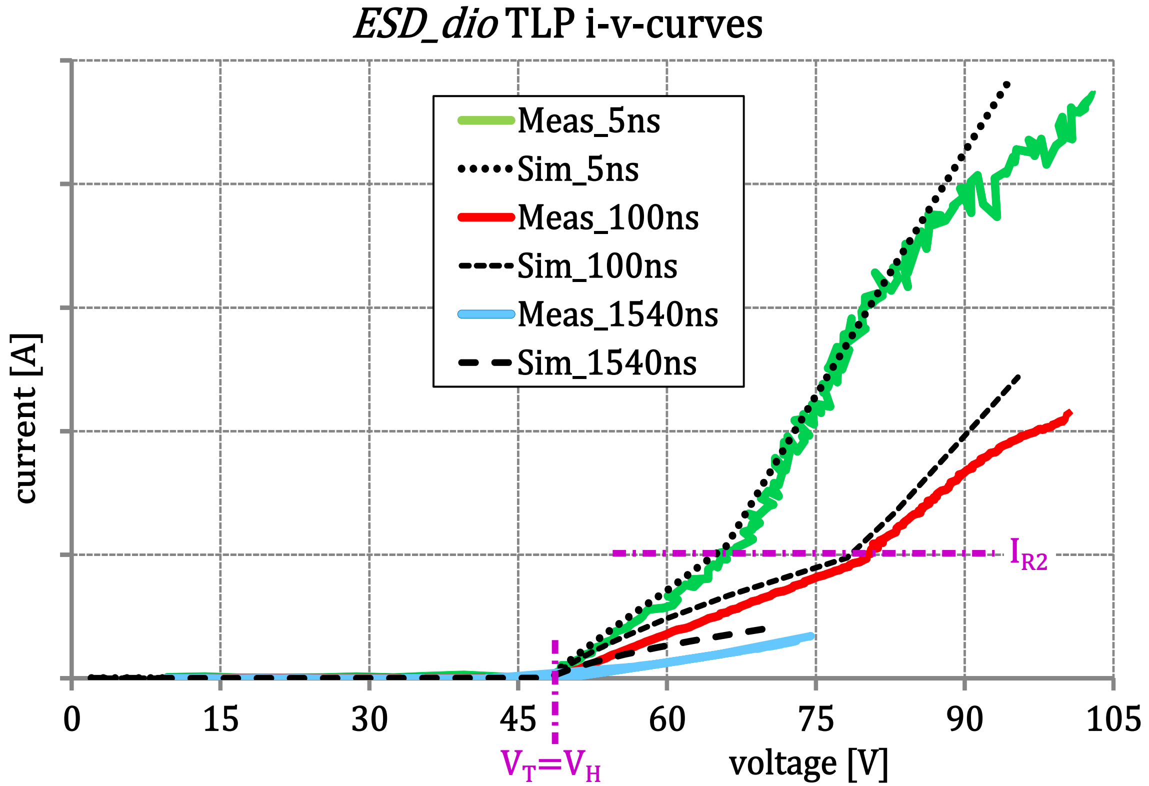


Figure 6.15: TLP i-v-curves of the HV avalanche breakdown diode *ESD_dio* and the extraction of the TBM parameters.

measured values and the fitting function is minimized. This solution is suggested for all fitting procedures as it ensures a high accuracy for the whole range of measured values.

Based on the power-to-failure P_f and the pulse duration td the energy-to-failure E_f can be calculated for different pulse durations. As the TLP pulses are nearly perfect rectangular by means of constant power during the pulse, the energy-to-failure is calculated by simply multiplying power-to-failure with the pulse duration $E_f = P_f \cdot td$. For these E_f values the fitting parameters E_a, E_b, E_c and E_d can be found with the above described procedure.

This HV breakdown diode can be typically used as ESD protection of pins with an Absolute Maximum Rating (AMR) of $V_{AMR} = 40\ V$. Therefore, this parameter is also set. In the model it is checked if the voltage drop above this device is below this value or not. If the AMR value is exceeded a flag *AMR_warning* is raised to 1 V to indicate that the IC is out of its guaranteed boundaries. It is clear that for ESD this be might often the case for ESD pulses and it is not always critical for the IC. But this flag is intended to be an information to the user that he operates the IC out of its specification and the simulated behavior is not guaranteed for all devices but rather the typical one.

All extracted parameters are summarized in table 6.5. For all empty fields the default values are taken which are also presented in this table. Additionally, in the right column the scaling

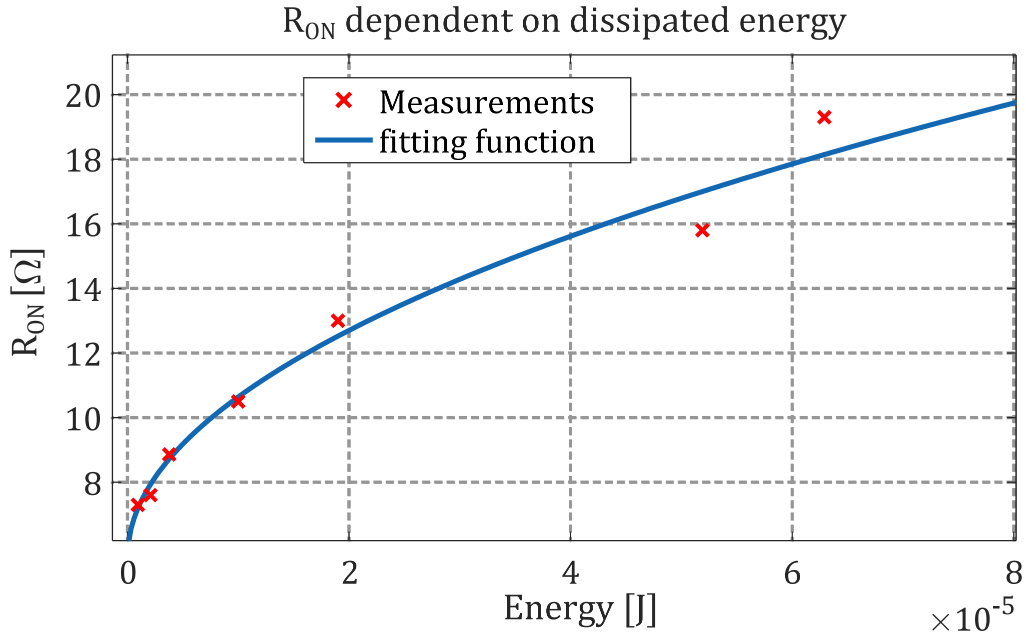


Figure 6.16: Measured values of the R_{ON} dependent on the Energy of the HV breakdown diode and the resulting fitting function $R_{ON} = 1574 \cdot Energy^{0.5} + 5.662$.

behavior is indicated with respect to changes in the device's active area A. All the voltage parameters do not scale with the device area A and hence, these cells are left empty. The other parameters either increase with the size $(1 \cdot A)$ or decrease with the size $(1/A)$. It is expected that all parameters are proportional or inversely proportional to the active area.

If all parameters are set like presented in table 6.5, the transient behavior in terms of TLP i-v-curves can be obtained by simulation. This can be done in the same way as the measurements. Starting from a low voltage level the TLP charge voltage is increased in certain steps. At each step a transient simulation is done and the current and voltage are averaged from $70\ \% - 90\ \%$ of the pulse duration. The simulated i-v-curves can be directly compared with the measured ones, see figure 6.3.2. In this figure the TLP i-v-curves with 5 ns, 100 ns and 1540 ns are plotted. A good matching of simulated curves (dashed or dotted, black lines) and measured values (colored, solid lines) is obtained. Moreover, the failure points of the 100 ns and 1540 ns curves are well met by simulations.

TBM-MOS parameter setting for HV n-channel DMOS transistor

The second application example for the parameter extraction, this time for the TBM-MOS, from TLP measurements is a high voltage DMOS transistor. This device is used several times within the communication IC and also impacts the ESD behavior of the IC. Therefore, a detailed model (TBM-MOS) is built for this device. The model parameter values are derived from TLP measurements. Most of the parameters are extracted from the quasi-static i-v-curves. First of

Table 6.5: TBM parameters for the HV breakdown diode and their scaling behavior

TBM parameter	**default value**	**value for *ESD_dio***	**scaling behavior**
V_{TR} $[V]$	53	48	
V_H $[V]$	53	48	
R_{leak} $[\Omega]$	10^8		$1/A$
R_a	$1 \cdot 10^{-19}$	1574	$1/A$
R_b	$1 \cdot 10^{-19}$	0.5	$1/A$
R_c $[\Omega]$	5.0	5.662	$1/A$
E_a	$1 \cdot 10^{-19}$	$2.01 \cdot 10^{-7}$	$1 \cdot A$
E_b	$1 \cdot 10^{-19}$	$1.96 \cdot 10^{-8}$	$1 \cdot A$
E_c $[J]$	$1 \cdot 10^{-19}$	$5.81 \cdot 10^{-9}$	$1 \cdot A$
E_d	$1 \cdot 10^{6}$	$9.30 \cdot 10^{-6}$	$1 \cdot A$
P_a	$1 \cdot 10^{-19}$		$1 \cdot A$
P_b	$1 \cdot 10^{-19}$		$1 \cdot A$
P_c $[W]$	$1 \cdot 10^{9}$		$1 \cdot A$
P_d	$1 \cdot 10^{-19}$		$1 \cdot A$
V_{R2} $[V]$	$1 \cdot 10^{3}$		
I_{R2} $[A]$	$1 \cdot 10^{3}$	2.5	$1/A$
R_2 $[\Omega]$	$1 \cdot 10^{6}$	4.0	$1/A$
V_{R3} $[V]$	$2 \cdot 10^{3}$		
R_3 $[\Omega]$	$1 \cdot 10^{7}$		$1/A$
V_{AMR} $[V]$	$2 \cdot 10^{3}$	40	
R_{sM} $[\Omega]$	$5 \cdot 10^{-6}$		$1/A$
$Q0$ $[C]$	$1 \cdot 10^{-6}$		$1 \cdot A$
I_{REC} $[A]$	$1 \cdot 10^{9}$		$1 \cdot A$

all, the trigger voltage dependent on the pulse duration is extracted.

The failure points power-to-failure and energy-to-failure are extracted similar to the beforehand described procedure for TBM, section 6.3.2. Also the fitting of P_f and E_f with respect to pulse duration is done accordingly. Solely the parameter for a maximum current density which triggers the device destruction I_{crit} is not existing in the TBM, but in the TBM-MOS. For very short pulses DMOS transistors tend to show a current limitation [26] which can be seen as a constant power-to-failure. Usually, when going to very short pulses the power-to-failure should rise rapidly according to [22] and [24]. When such a current limitation is seen for very short pulses (e.g. figure 6.3.2), this failure points shall be excluded for the fitting of power-to-failure and energy-to-failure. Instead, this current limit is set as separate failure threshold I_{crit}. Within the model both failure borders, the power-to-failure fitting function (blue,solid line) and the maximum current I_{crit} (green, dashed line) are implemented. Depending on the pulse duration only one failure border is the lowest and determines the overall failure limit of the device.

The dynamic channel current parameters C_{DG}, C_{GS}, R_{GS}, $Vd0$ and kp are extracted from

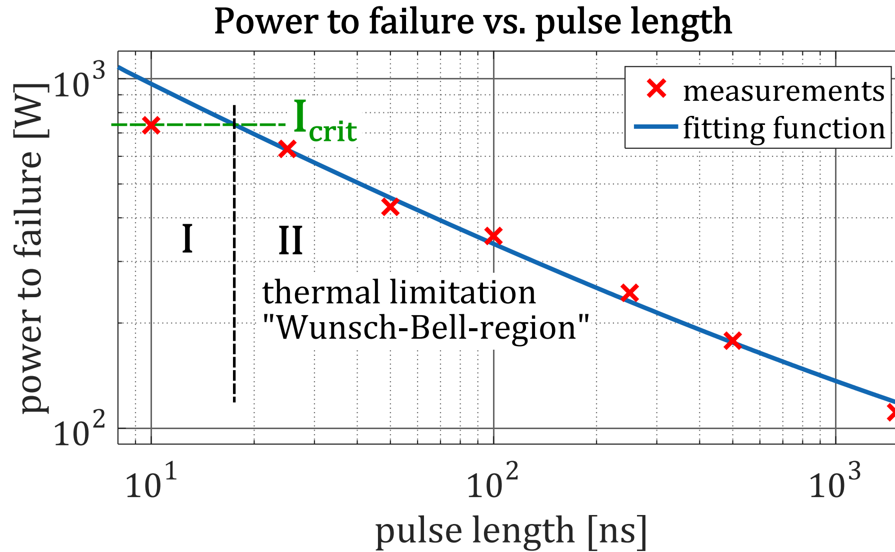


Figure 6.17: Power to failure over pulse length for the hvnmos with the fitting function for the TBM-MOS. The current limitation can be seen for very short pulses (region I) while the power to failure is thermally limited for longer pulses (classical "Wunsch-Bell-region", region II).

the transient curves of the TLP measurements. The capacitance values C_{DG} and C_{GS}, the threshold voltage $Vd0$ and the gain factor kp are set to match the initial voltage coupling from *drain* to *gate*. The gate resistor is set to match the discharge time constant of the gate voltage. The characterization was done with the gate shorted to source, the so called grounded gate NMOS configuration, and with a gate source resistance of 5 $k\Omega$ to get the characteristic behavior with different gate bias conditions.

6.3.3 Extraction of parasitic resistances from on-chip wiring

The on-chip wiring can influence the transient behavior and the failure thresholds of the IC. Therefore, the ohmic resistance of the wiring in the main ESD paths are extracted and added to the IC model. The resistance values are extracted with a commercially available tool and post-processed to get the resulting resistance values between two devices. Figure 6.3.3 presents the resulting schematic for the IC-TBM including the wiring resistance values.

6.3.4 Verification of the chip-TBM with measurements

The verification of the IC ESD model generated from design data is done by comparison of TLP measurements and simulations in terms of transient behavior and failure levels. The i-v-curves of different pulse lengths and also the transient waveforms are compared. The more interesting fact for system designers is the accuracy of the IC ESD model in system ESD simulations. Therefore, the simulated ESD robustness according to [63] is compared to failure

Table 6.6: TBM parameters for the HV NMOS and their scaling behavior

TBM-MOS parameter	**default value**	**value for *hvnmos***	**scaling behavior**
V_T $[V]$	55	36.44	
V_{Ta}	$1 \cdot 10^{-19}$	1055	
V_{Tb}	$1 \cdot 10^{-19}$	0.211	
V_{Tmax} $[V]$	$1 \cdot 10^{3}$	79	
R_{leak} $[\Omega]$	$1 \cdot 10^{8}$		$1/A$
R_a	$1 \cdot 10^{-19}$	$2.34 \cdot 10^{4}$	$1/A$
R_b	$1 \cdot 10^{-19}$	$4.02 \cdot 10^{6}$	$1/A$
R_c $[\Omega]$	0.5	1.21	$1/A$
E_a	$1 \cdot 10^{-19}$	$1.48 \cdot 10^{-3}$	$1 \cdot A$
E_b	$1 \cdot 10^{-19}$	40.86	$1 \cdot A$
E_c $[J]$	$1 \cdot 10^{-19}$	$3.22 \cdot 10^{-5}$	$1 \cdot A$
E_d	$1 \cdot 10^{6}$	$1.67 \cdot 10^{-6}$	$1 \cdot A$
P_a	$1 \cdot 10^{-19}$	$1.06 \cdot 10^{-5}$	$1 \cdot A$
P_b	$1 \cdot 10^{-19}$	$3.78 \cdot 10^{-7}$	$1 \cdot A$
P_c $[W]$	$1 \cdot 10^{9}$	$3.18 \cdot 10^{2}$	$1 \cdot A$
P_d	$1 \cdot 10^{-19}$	$3.88 \cdot 10^{3}$	$1 \cdot A$
C_{DG} $[F]$	$25 \cdot 10^{-12}$	$11.0 \cdot 10^{-12}$	$1 \cdot A$
C_{GS} $[F]$	$20 \cdot 10^{-12}$	$11.0 \cdot 10^{-12}$	$1 \cdot A$
R_{GS} $[\Omega]$	$1 \cdot 10^{8}$		$1/A$
V_{AMR} $[V]$	$2 \cdot 10^{3}$	40	
V_{d0} $[V]$	5	1.1	
kp	0.25	$1.84 \cdot 10^{-2}$	$1 \cdot A$
I_{crit} $[A]$	$2 \cdot 10^{3}$	1.1	$1 \cdot A$

levels measured in compliance with this standard. First of all, the IC with its application specific circuitry, especially the capacitors at VDD and VIO, without external components on the bus lines is tested. As a second test condition a common mode choke (CMC) is added at the bus lines and the ESD test is done again up to the physical destruction limit. With this small "test system" also the transient waveforms of current entering the system from the ESD tester and voltage at certain points in the system are measured (see section 7.4.2). The waveforms from measurement are compared with simulated ones to see the accuracy of the IC ESD model. Based on the detailed behavioral model for the CMC developed in section 4.3.3 accurate system simulations are possible with the proposed IC ESD model.

Summary

This chapter presents a novel methodology to extract behavioral ESD models for complete ICs from their design data. These simplified IC models enable system ESD robustness simulations

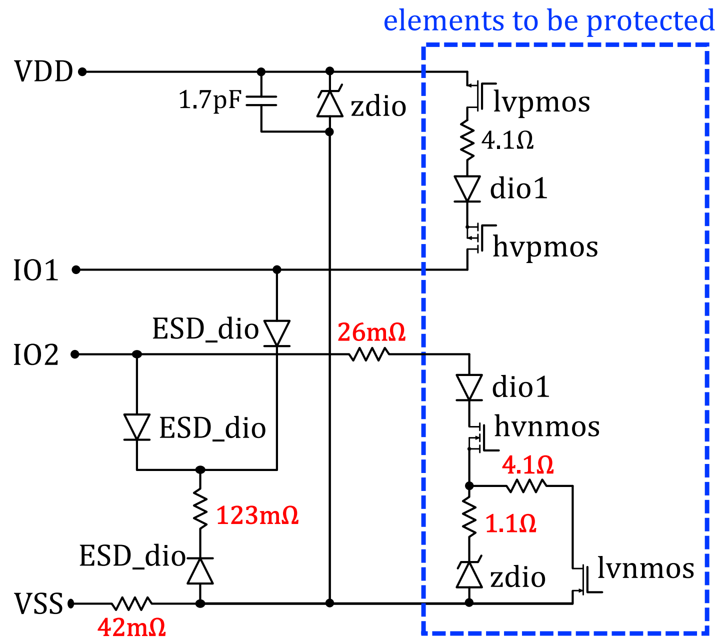


Figure 6.18: Resulting schematic of DUT 2 for the chip-TBM including resistance values of the on-chip wiring.

on PCB level during an early design phase with short simulation runs. Based on the complete schematic or netlist the necessary devices for the behavioral ESD model are identified. The manual selection process seems to be currently the most suitable one. Other selection processes are conceivable which can be automated. To develop appropriate solutions significantly more effort is needed. The manual selection is already a step forward to an efficient IC model generation for system simulations. All remaining devices are substituted by their respective black box model (TBM respectively TBM-MOS). The resistance and ideally also the inductance of the on-chip wiring is extracted from the IC layout information. These parasitic values are integrated into the reduced netlist respectively schematic. The black box modeling approach allows to combine several devices and also wiring resistances into one behavioral model. Ideally the schematic can be reduced to one instance of TBM respectively TBM-MOS for one pin-combination and polarity. A simplified IC model for system simulations, which does not contain any confidential information about the IC design respectively manufacturing processes, is created. This is highly appreciated by the IC vendors. The IC model (chip-TBM) can be combined with the package parasitic values (R, L and C) to form the ESD model for the complete IC (IC-TBM). The proposed methodology allows to generate ESD models for complete ICs without doing any measurements with the IC itself. Assuming that a TBM library is already existing for this manufacturing technology, these IC ESD models can be created very resource efficient. Such a methodology to generate IC models without measurements on the complete IC has not been reported previously. Parts of this chapter were already published in

the *IEEE Transactions on Electromagnetic Compatibility* [9]. The second application example (communication IC) for this methodology was presented at the EOS/ESD Symposium 2019 [64]. The feasibility of the proposed methodology is shown on two application examples. The accuracy of these IC models regarding system ESD robustness levels are discussed in the following chapter.

7 Measurement and simulation results

In this chapter the basic measurement techniques are described in detail. The results from measurements with different ICs at different measurement setups are presented. Additionally, the simulation setups for the different measurements are described. Selected simulation results are compared with measurements in terms of transient behavior and destruction limit.

7.1 Measurement setup TLP

The transmission line pulser (TLP) is the standard characterization tool for ESD protection devices and concepts as it delivers very well reproducible results and precise current and voltage waveform measurement. The foundation for this was laid by Maloney and Khurana in 1985, when they described the TLP measurements as basis for circuit modeling under ESD stress [16]. Since the TLP is easy to use, highly reproducibly, precise in voltage and current measurement and able to reproduce the failure signatures of ESD events, it has developed to the most used measurement tool among ESD engineers.

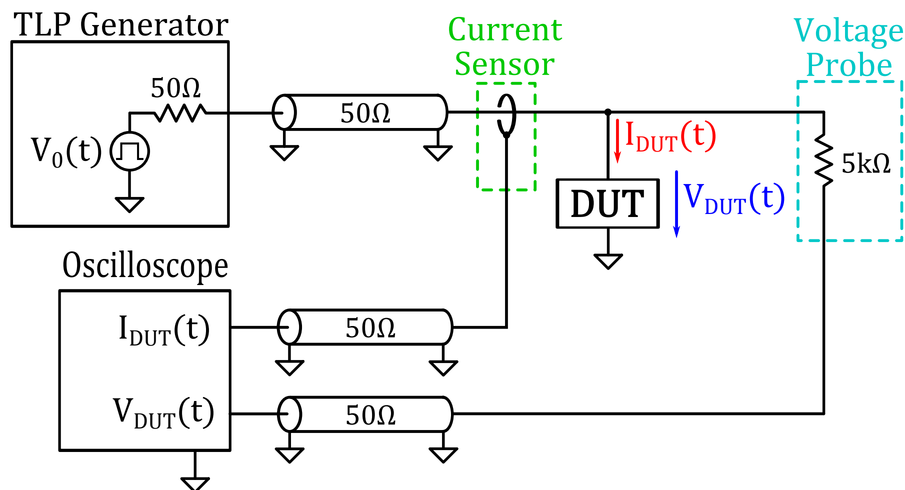


Figure 7.1: Schematic setup of a typical transmission line pulse (TLP) system [51].

Basically, the TLP is solely a 50 Ω transmission line which is charged to a certain voltage and at time *t*0 a switch is closed and the transmission line is discharged into the DUT [51]. Depending on the length of the transmission line the pulse has a certain duration *td*. TLP pulses can be considered as rectangular pulses with a constant power during the pulse. As

discharge switch usually a relay filled with mercury is used to generate steep rise times in the range of 100 *ps* or below and bounce-free switching behavior. Rise-time filters are applied to generate slower rise times of the TLP pulses if desired. During each pulse the current through the DUT I_{DUT} and the voltage drop across it V_{DUT} is measured with an oscilloscope, see figure 7.1. Historically the current and voltage values are averaged between two time points during the pulse t_1 and t_2, typically from 70 % to 90 % of the pulse duration. For ESD characterization the charging voltage is increased from one pulse to the following up to the physical destruction of the device. The physical failure is detected by an increase in leakage current which is usually measured after each TLP pulse. Moreover, the DC-I-V-curve can be measured before or after the TLP stress.

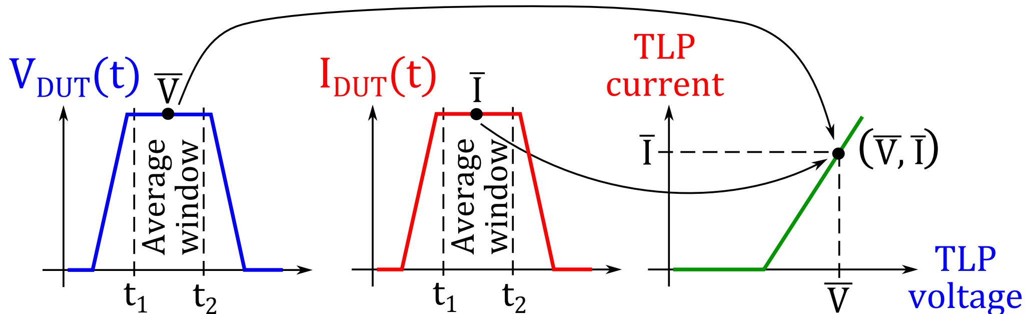


Figure 7.2: Schematic illustration of the averaging of current and voltage waveform to get a quasi-static i-v-curve, the often called TLP curve [51].

The transient waveforms are evaluated to generate the quasi-static i-v-curve by averaging the voltage and current waveforms from $t_1 = 70$ % to $t_2 = 90$ % of the pulse duration (figure 7.1). Each TLP pulse gives one point of this quasi-static i-v-curve which shows for example the clamping behavior of ESD protection devices and their destruction limit. The physical destruction is usually determined by an increased leakage current which is typically measured after each pulse.

7.2 Measurement setup HMM-TLP

As the system level ESD test results can differ significantly between different labs and ESD generators a pulse source with a higher reproducibility was developed by Cao et.al. [53]. By modification of a TLP system to a so called human metal model TLP (HMM-TLP) it can generate very reproducible current pulses which comply with the definition of the IEC 61000-4-2 [14]. Another benefit of the HMM-TLP is the applicability on wafer level which is not easy with the official ESD generators for system level ESD. This enables the characterization of ESD protection devices and concepts already on wafer level. One often discussed disadvantage of the HMM-TLP is the different source impedance of the pulse generator compared to the ESD generator which has 330 Ω. To reduce pulse reflections at the DUT a special probe with 48 Ω

series resistance is provided by the TLP manufacturer HPPI [65] for instance. This probe also increases the source impedance of the HMM-TLP of usually 50 Ω to 98 Ω which is closer to the 330 Ω of a standard conform ESD generators, but still not the same. Therefore, the results of HMM-TLP and real system ESD tests in terms of transient waveforms and destruction levels can differ. For ICs as DUT it is expected that the difference is not relevant as the IC is quite low-ohmic compared to the ESD pulse source whether it is 98 Ω or 330 Ω. The differences are more prominent at systems/DUTs with a high impedance, e.g. inductors. In general, the differences can be significant at systems where several components are combined and the current is shared between them. The measurement setup of HMM-TLP is schematically shown in figure 7.2.

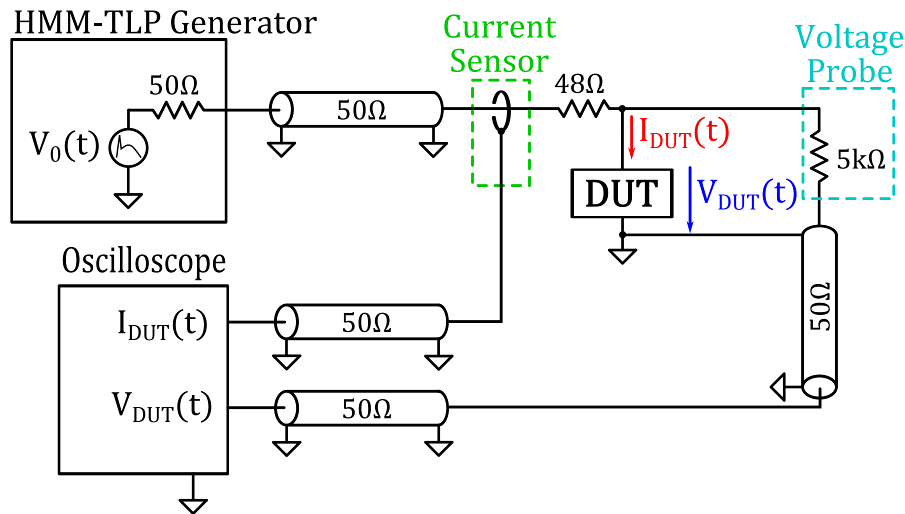


Figure 7.3: Schematic setup of a TLP system which is modified internally to deliver the ESD current pulse defined in IEC 61000-4-2 [14].

7.3 Measurement setup system level ESD test

During EMC and ESD qualification of systems and sub-systems the ESD tests are done according to the IEC 61000-4-2 [14] for general electronic products or according to ISO10605 [15] for automotive components and systems. The ESD generators which comply to these standards usually have the shape of a gun. Therefore, these tests are often called "GUN tests" in colloquial speech. The goal of the proposed modeling methodology is to predict the failure level of electronic systems and sub-systems at these tests to help the system designer in designing robust systems. So the prediction accuracy of the IC ESD models generated according to the proposed modeling methodology is compared to measured failure levels. In a first step, solely the IC is stressed up to destruction without any additional discrete components. For this case, the IC was mounted on a PCB to directly contact one of the pins with the tip of the ESD tester.

The second pin was connected to the horizontal coupling plane which is directly connected to the tester ground with a low impedance. A photograph of this test-setup is shown in figure 7.3. Secondly, the IC as DUT is combined with external components, e.g. capacitors or TVS diodes, on a dedicated PCB and this test-system is tested up to destruction. In this case also the IC is most likely to get physically damaged as it contains the most vulnerable parts of the system. The physical damage of the IC is again detected by a leakage increase of the IC after the ESD stress. The standard differentiates in hard failures (physical damage) and soft failures (system upset or resets). In this work only the hard failures without power supply were considered. As a consequence no functional tests were done during or after the ESD injection, but the leakage current was quantified. An increase of leakage current at a certain voltage or a shift in the DC I-V-curve after an ESD stress leads to the classification of a failed ESD test. This means this ESD test level is denoted as failure level or failure voltage. By contrast, the ESD test level of the beforehand test step is classified as ESD robustness level.

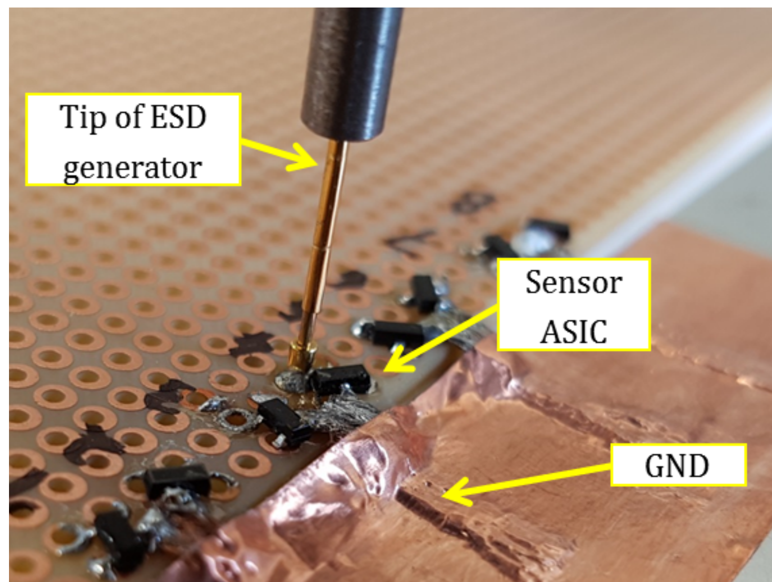


Figure 7.4: Photograph of the test setup to measure the system ESD robustness of a sensor ASIC stand-alone without additional devices.

7.4 Measurement setup PCB level

The ESD tests on system level described in the previous section focus on the destruction limit of the system. But it is also of interest if the generated IC models together with adequate ESD models of the discrete components (chapter 4) are able to predict the transient response to an ESD event correctly. As the considered systems are without power supply, the quantities of interest are the voltage and current distribution within the system. The ESD pulse itself has a very high di/dt and hence a significant amount of radiated electromagnetic waves which

exacerbates the measurement of current or voltage waveforms during ESD events. As a quasi-standard the voltage drops at the DUT during TLP tests are quantified with a high-ohmic voltage probe embedded in a 50 Ω coaxial cable environment. These voltage probes have a response characteristic which is highly linear in the frequency range up to a few GHz. The type of probes frequently used is Picoprobe Model 10 with 5 $k\Omega$ input impedance supplied by GGB industries with a frequency range specified from dc up to 5 GHz [66]. The coaxial cables already provide a good shielding against electromagnetic waves coming to the measurement line. Therefore, such RF voltage probes are used to measure certain node voltages within a system during ESD injection. A further reduction of the electromagnetic coupling from the ESD generator to the voltage probe can be obtained by using damping ferrites around the coaxial cable. This measure reduces to induced currents on the coaxial shield and hence reduce the coupled noise on the voltage signal. With these high-ohmic voltage probes the voltage drops at defined points of a system can be measured without changing the system behavior. For current sensing during ESD it is not that easy to accurately measure current flows within a system without changing the system behavior. There are several techniques discussed in literature, e.g. inductive coupling of adjacent traces to measure the current in a certain PCB line, but the result interpretation is not straightforward. Due to this reason the current sensing within a system during ESD pulses is not implemented. It is expected that the measurement of certain node voltages is enough to validate the transient models of the system components. For the sake of completeness the ESD current injected from the ESD generator into the system is measured with an inductive current clamp (Fischer Custom Communications F-65A) with an adequate high measurement bandwidth of $10kHz - 1GHz$.

7.4.1 Example 1: Sensor ASIC

First of all, a sensor ASIC was investigated in detail in terms of ESD robustness according to the Generic IC EMC Test Specification [40]. The results show a strong dependency of the system ESD robustness on the PCB layout when pin-combination *pin1-pin2* is protected with a capacitance of 47 nF. To investigate the reason for this strong sensitivity the voltage at the IC pins during an ESD injection into the system was measured. Figure 7.4.1 shows schematically the measurement setup while figure 7.4.1 shows the real setup in a photograph. The measurement results are compared with system simulation results in section 7.4.1. Due to the comparably high inductance in the path of the capacitor a very high voltage drop above this path is generated. This voltage spike is seen by the IC for a few nanoseconds. Depending on the actual layout of the PCB this peak voltage goes to a certain value at a defined ESD test voltage. Assuming that this voltage peak initiates a destructive process within the IC, differences in the system ESD robustness for different layout variants can be explained. Based on these results a recommendation for an optimized layout can be done.

The measurement of voltages at certain points within a system during ESD injection is

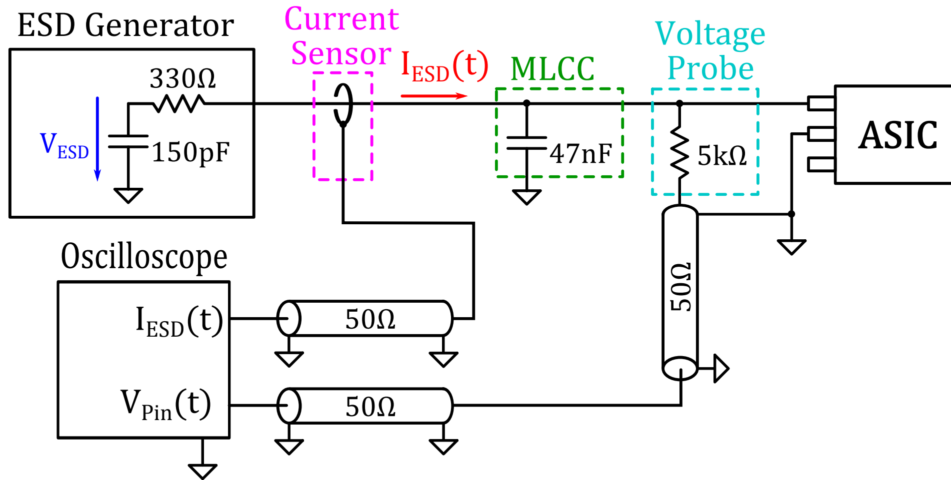


Figure 7.5: Schematic setup of the waveform measurements of a small system consisting of a sensor ASIC and a MLCC during system ESD tests.

definitely not an easy task. By contrast, one has to take care that the real voltage value is measured without any RF noise coming from the ESD generator. By design these ESD generators deliver a current pulse into the discharge point and in addition, they emit electromagnetic waves with a high field strength. This is basically wanted to check the robustness of electronic systems against these electromagetic disturbances radiated by real ESD events.

This basic intention of the test standard IEC 61000-4-2 is nowadays not always in focus when the test is applied. For the un-powered test for destruction, which is in focus of this work, the scope is to ensure that electronic components or sub-systems can survive a certain ESD threat. The goal is to guarantee that the products survive the final assembly and also repair activities outside of fully electrostatic areas, e.g. final-assembly line for cars or repair garages. To measure the current and voltage distribution during these ESD injections into electronic systems the noise coupling from the ESD generators needs to be minimized. It has been proved to be successful using high-impedance voltage probes and connect them via a coaxial cable to an oscilloscope. The oscilloscope itself is very sensitive to electromagnetic noise. Therefore, a metallic plate or shielding which is connected to ground is placed between the ESD generator and the oscilloscope. In this case the oscilloscope was placed underneath the horizontal coupling plane which is connected to the ground of the ESD generator. The voltage probes are connected by 50Ω coaxial cables to the oscilloscope. To reduce the induced noise on the cable shielding the cables are equipped with several damping ferrites.

7.4.2 Example 2: Communication-IC

Some automotive communication ICs are typically tested without external components to find their system ESD robustness according to IEC61000-4-2 [14] respectively ISO10605 [15]. For differential communication buses often common mode inductors are used to suppress common

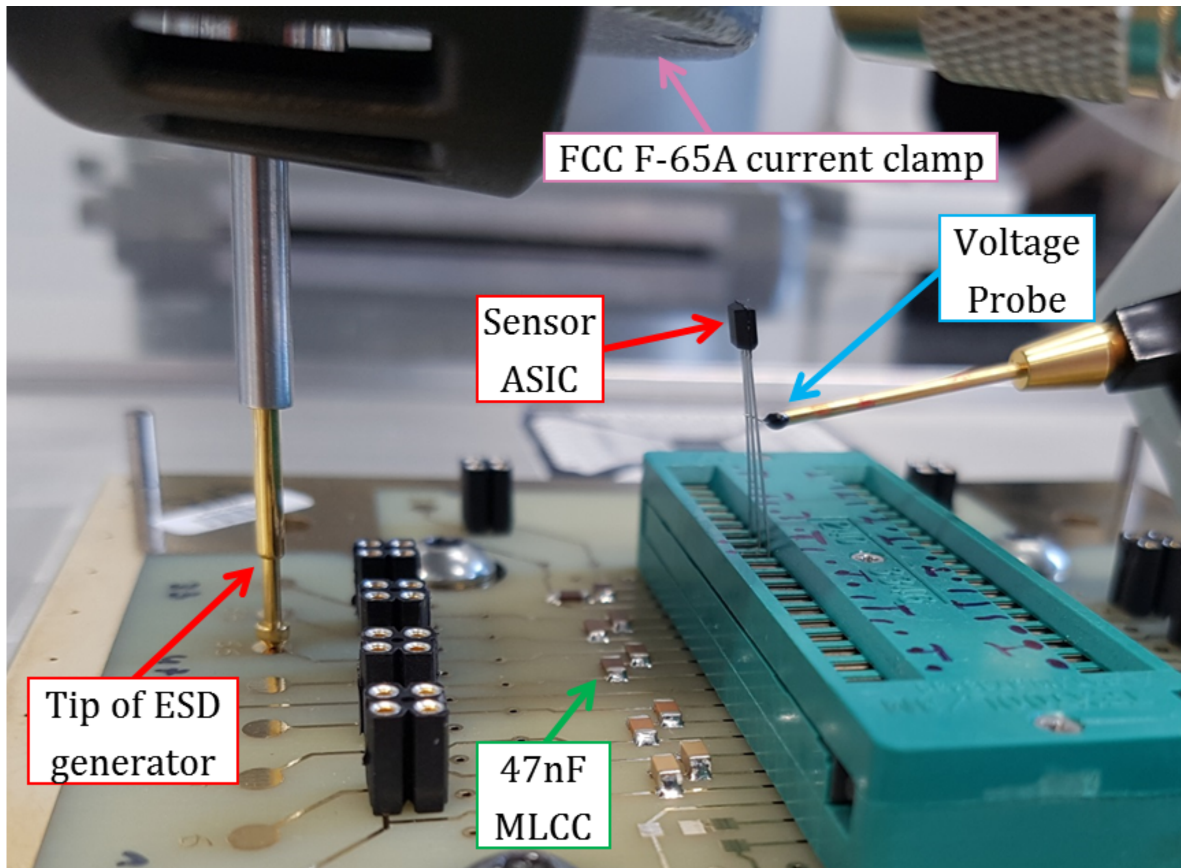


Figure 7.6: Photograph of the test setup to measure the voltage waveform during system ESD test at the pins of a sensor ASIC while it is protected with a 47 nF MLCC on the PCB.

mode currents, which makes the communication more robust and reliable. Due to this reason the transient behavior of CMCs during ESD injection was investigated and modeled (see section 4.3.3). Based on the strong saturation seen during TLP measurements (figure 4.5) it is expected that the CMC is blocking the initial peak of the ESD current while the second peak is transferred nearly unchanged to the IC.

This expectation is indorsed by simulations with the proposed CMC model including saturation, see section 4.3.3. The simulation results are confirmed by measuring certain node voltages within this system during real ESD tests. The measurement results are compared with system simulation results in section 7.6.2. The measurement setup is shown schematically in figure 7.4.2. A photograph of the realized measurement configuration is shown in figure 7.4.2. The typically used high ohmic voltage probes have a maximum voltage of $\approx 1\ kV$. Above this voltage sparks are expected to bridge the signal to the shielding and hence the voltage measurement is not possible. Therefore, the high voltages at the input of the CMC ($\approx$ ESD test voltage) cannot be measured with the available Picoprobes. Due to this reason, a comparable high ohmic probe

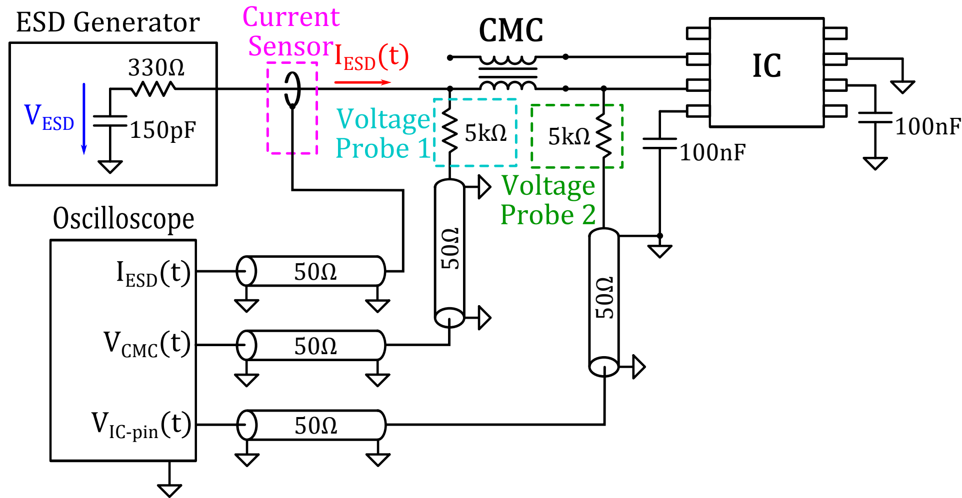


Figure 7.7: Schematic setup of the waveform measurements of a small system consisting of a communication IC and a CMC during ESD tests according to IEC61000-4-2 [14] resp. ISO10605 [15].

was built with bigger physical dimensions to increase the maximum measurement voltage, which is determined by the spark over voltage. With these custom made voltage probes the voltage can be measured accurately up to 15 kV ESD test voltage.

7.5 Simulation vs. measurement with single IC

This section presents selected results obtained by measurements with the stand-alone IC. The used measurements methods are described in the subsections beforehand. Also simulation results are presented and compared to measured values. By this, the accuracy of the proposed behavioral IC model for ESD simulations is evaluated.

7.5.1 TLP measurements: transient waveforms and TLP i-v-curve

First of all the generated IC model is compared with TLP measurement results, both in terms of transient waveforms and also the quasi-static i-v-curve. The quasi-static i-v-curve obtained by TLP measurements of a few elements are plotted and compared to measurements in figures 5.7, 5.13 and 6.3.2.

7.5.2 HMM-TLP measurements: waveforms and failure level

The proposed methodology to generate IC ESD models has the goal to enable ESD robustness design on PCB level. Electronic systems and sub-systems are qualified according to IEC 61000-4-2 or ISO106050 in terms of ESD robustness. Therefore, the accuracy of the IC model is especially of interest when such an ESD pulse is applied on the IC. The HMM-TLP is able

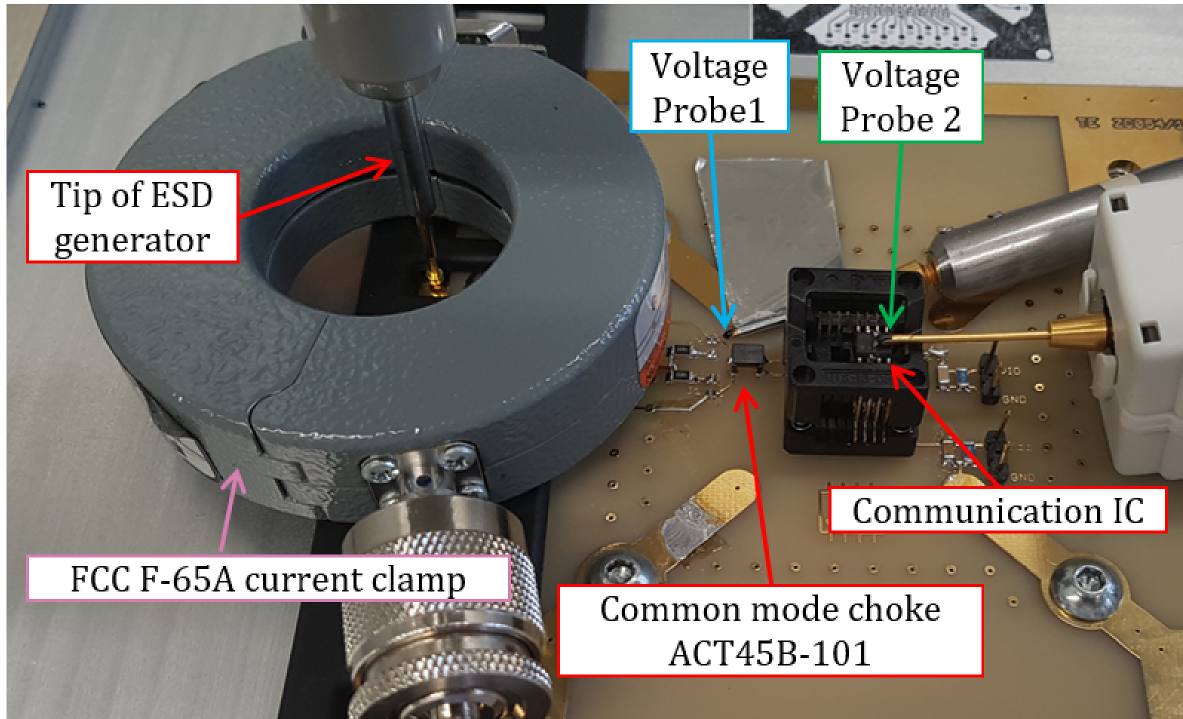


Figure 7.8: Photograph of setup to measure the waveforms within a small system consisting of a communication IC and a CMC during ESD tests according to IEC61000-4-2 [14] resp. ISO10605 [15].

to generate a current pulse compliant to IEC 61000-4-2 and offers the ability of measuring precisely the current flow and voltage drop during the pulse. This enables a fast assessment of ESD protection devices, concepts or complete ICs regarding the system ESD robustness. The transient waveforms of certain DUTs can be easily compared to simulation results as well as the DUT‘s robustness level.

This is shown exemplary with DUT1. For the complete IC a behavioral model is built with several instances of TBM for each pin-combination and polarity respectively. Details are given in section 7.6.1 and [8]. The transient waveforms of current and voltage during a HMM-TLP with 3 kV charging voltage injected into Pin1 vs. Pin3 is plotted in figure 7.5.2. The matching in the transient waveforms is acceptable. It has to be denoted that the current are shifted by 10 ns to separate the first peak from the voltage waveforms to have them separated from each other for better visibility. For the sake of compactness, the plots of the other pin-combinations are not added. The matching of measured and simulated waveforms is in good matching for all pin-combinations of this IC. Moreover, the failure levels at HMM-TLP stress are compared from measurement and simulation. The last passed ESD stress levels are shown in figure 7.5.3. The measurement results of HMM-TLP (light green bars) are quite close to simulation results (red bars) for all pin-combinations and polarities. The overall accuracy is within $\pm$ 20 %, which is highly appreciated by system designers for the prediction accuracy. To compare the

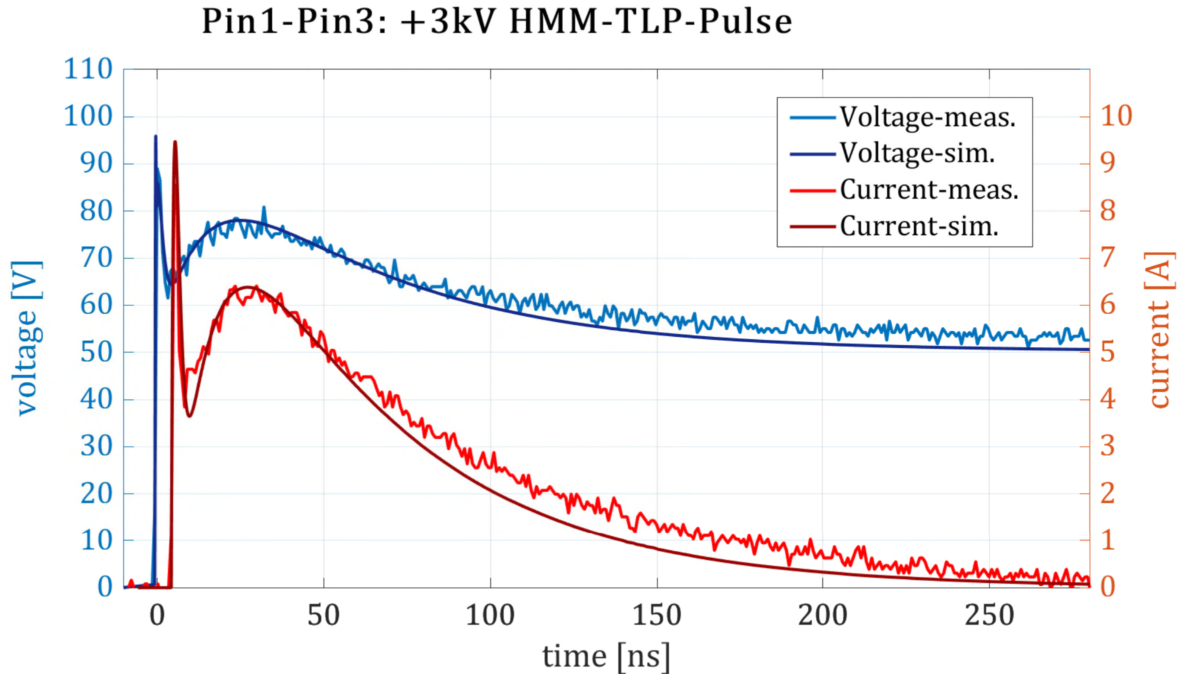


Figure 7.9: Comparison of transients waveforms obtained by measurements and simulation with DUT1 (Pin1 vs. Pin3) during HMM-TLP stress.

proposed modeling methodology with state of the art modeling methodologies additionally an IC model with the 100 ns quasi-static behavior and failure energy is included in the comparison (purple bars). The results show clearly that a transient behavior model with failure thresholds dependent on the pulse duration like TBM can predict the System ESD robustness with a higher accuracy.

7.5.3 System ESD measurements: failure level

The most important value for system designers in terms of IC model accuracy for ESD robustness design is definitely the accuracy of the IC model at ESD test according to ISO10605, IEC 61000-4-2 or IEC/TS 62228. To exclude influences of the model accuracy of external components (e.g. capacitors or PCB traces) the ESD robustness of the sensor ASIC is tested as stand-alone IC. The picture 7.3 shows that the discharge tip of the ESD generator is directly placed on one of the IC pins. The second pin for this stress combination is connected to tester ground with a very low impedance. The ESD test voltage is raised in steps of 200 V and after each stress the DC I-V-curve of the investigated pin-combination is measured. The failure level is the stress level which caused a change of more than 10 % of the leakage current below the DC breakdown voltage. Figure 7.5.3 shows the system ESD robustness of the bare IC compared to HMM-TLP and simulated robustness levels. In general, the system ESD robustness (dark green bars) is

in good agreement with the HMM-TLP results (light green bars). Also the simulated values (red bars) are within ± 20 % tolerance to the measured values. For completeness additionally simulation results with a state of the art modeling approach (100 *ns* quasi-static model) are plotted with purple bars. These results show a higher deviation from the measured values and hence confirm the higher accuracy of the proposed modeling methodology TBM.

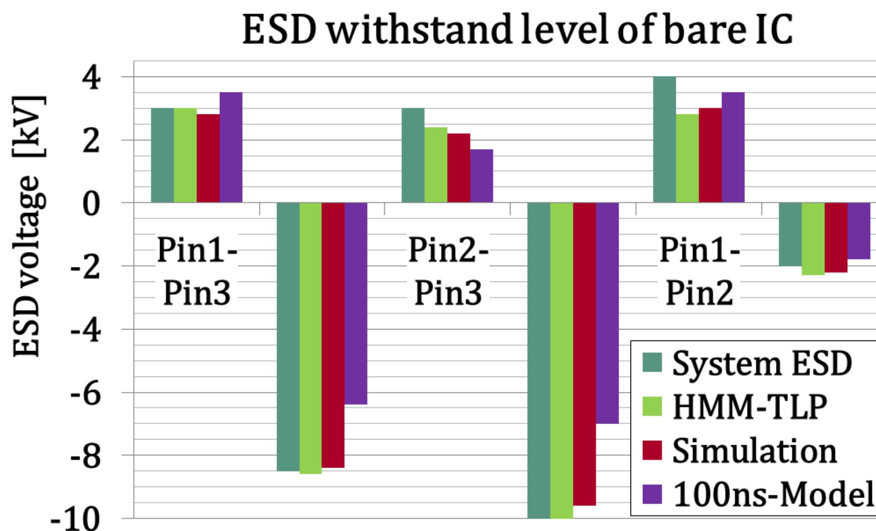


Figure 7.10: ESD failure levels of DUT1 obtained by measurement (System ESD and HMM-TLP) and simulation (TBM and 100ns-Model).

7.6 Simulations on PCB Level

To prove the accuracy of the system ESD simulations the transient waveforms are compared with measurement data. Precise system ESD simulations allow to find the weak points within a system regarding ESD robustness. Simulations with changed system designs can verify if they are likely to improve or decrease the system ESD robustness. And hence the system ESD robustness can be optimized in an early design phase.

7.6.1 Simulation setup

Precise models of all components are necessary to obtain informative results from system simulations during ESD stress pulses. Details about the simulation setups and the relevant components are presented in this section.

ESD generator model

The modeling of ESD generators for circuit level simulations is discussed in literature extensively [67], [68], [69], [70]. Precise lumped element models are presented for various ESD generator types from different vendors. For this work a circuit representation for the existing ESD generator (NoiseKen TC815-R) is taken from literature [71]. The discharge current of this model in simulation is compared to the discharge current measured in the lab. Figure 7.6.1 shows the discharge current from the ESD generator into a short circuit both from measurement and simulation. The matching of the current waveforms is good. This ensures a high comparability of the transient waveforms within systems obtained by measurements and simulations. Due to the good matching of the transient waveforms it is expected that this ESD generator model does not limit the accuracy of the system simulations.

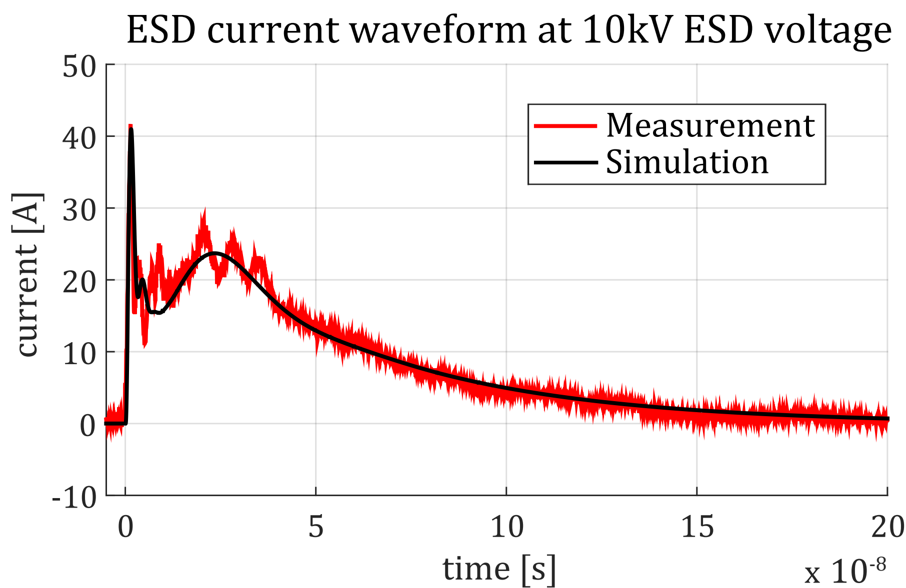


Figure 7.11: Comparison of ESD currents at $10kV$ ESD test voltage into a short from measurement and simulation.

PCB with parasitic elements

For the sake of simplicity the PCB traces are modeled with lumped element equivalent circuits. For higher accuracy the S- or Z-Parameter can be used which are obtained by measurement or by extraction with a three dimensional field solver from design data. The resistance, inductance and capacitance per unit length can be calculated with the formulas for micro-strip lines. Also simple calculation tools like the PCB toolkit provided by Saturn PCB Design, Inc. [72] can be used to get the impedance per unit length of the PCB traces. The model implementation can be done by one discrete resistor, inductor and capacitor for one PCB trace. An enhanced trace model can be built by using a few (e.g. ten) RLC-elements in series. This setup is able to

reproduce also the delay effects of PCB traces. Another possibility to model the traces is using the lossy transmission lines provided by SPICE. In this case R‘, L‘, C‘, G‘ and the length are set. Some more details about modeling the PCB traces is presented in section 4.2. For this work a series of ten RLC-elements is used to reproduce PCB traces.

Parameters of the PCB traces used in this work: $R‘ = 16.7\ m\Omega/cm$, $L‘ = 7.5\ nH/cm$, $C‘ = 0.43\ pF/cm$.

External components - capacitors

As pointed out in section 4.3.1 the parasitic series resistance and inductance of a capacitor is necessary for precise system ESD simulations. The ESL and ESR values of the discrete MLCCs are taken from an existing data base generated out of S-Parameter measurements of automotive qualified capacitors.

Parameters for the parasitic elements of the 47 nF MLCC used in this work: $ESR = 19\ m\Omega$, $ESL = 491\ pH$.

External components - CMC

Communication ICs are often used within cars to enable communication between different sub-modules, e.g. electronic control units (ECUs). As the communication pins ($BUSH$ and $BUSL$) are routed directly to the connector they are exposed to possible ESD events at the end-user respectively car repair shop. In contrast to electronic manufacturing sites, a garage is typically not an EPA and hence the voltage people can charge up electrostatically to quite high voltages ($\approx 8 - 15\ kV$). Therefore, the pins of ECUs are typically tested for their ESD robustness up to $\approx 8 - 15\ kV$. In a worst case scenario the IC pins are directly connected without any additional discrete components. For improved EMC behavior there is sometimes a CMC used on differential bus lines which is placed between the ECU connector and the IC pins. The expectation is that the inductance of the CMC damps the ESD current and hence the ESD stress is reduced at the IC side. The ferrite core and its saturation causes a less efficient damping than expected. This behavior is investigated and explained in detail in chapter 4.3.3. For this reason a detailed ESD model for the investigated CMC is generated to replicate the actual behavior of the choke during ESD tests. The model details are presented in section 4.3.3.

Transient behavior model of IC

The details on the IC models for the first DUT, a sensor ASIC, are presented in this section. This behavioral IC model is used to see the system response to an ESD pulse according to ISO10605 [15]. TLP measurements with different pulse durations on the complete IC within the package are the basis for the IC ESD model. Details on this IC model can be found in [8].

The model for the complete IC is constructed with five subcircuits ($X1...X5$) respectively TBM instances. Each subcircuit represents the behavior of the IC during ESD pulses for one

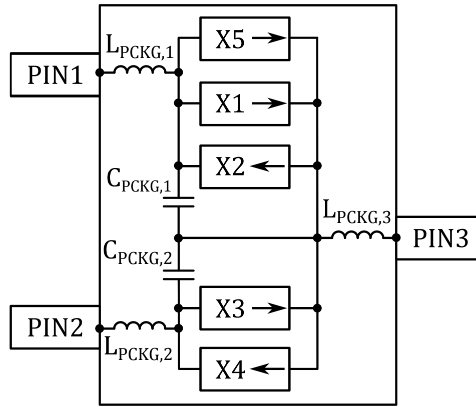


Figure 7.12: Overview of the ESD model for a complete IC (DUT1) built with several TBM instances ($X1...X5$) combined with the package parasitics.

polarity. The polarity of each TBM instance is indicated by the small arrow which shows the possible current flow. For example $pin2 - pin3$ in positive polarity is modeled with $X3$ for ESD and comparable pulses. For positive stress pulses at $pin1 - pin2$ there are two TBM instances in parallel, $X1$ and $X5$. While $X1$ mainly describes the transient current drain and voltage drop, $X5$ represents the circuit to be protected which triggers at a certain voltage drop over the ESD protection $X1$ and shows a snap-back behavior. This snap-back is already destructive at low energy levels. For very short pulses in the range of 5 ns this snap-back can be survived by the IC for a limited power level. Therefore, this special destruction behavior is modeled with two TBM instances in parallel. As shown in [8] and [36] this works well to simulate the system ESD robustness of the IC when it is protected with an external capacitor. The TBM instances are combined with parasitic inductance and capacitor values coming from the package. The values are extracted from S-Parameter measurements on the packaged IC.

The second DUT used for the measurements at PCB level is a communication IC presented in section 6.3. The IC model is created with several instances of TBM and TBM-MOS and extracted from the IC design data. No characterization measurements were done with the complete IC. Solely the single devices were characterized on a test-chip and the parameters were found for TBM respectively TBM-MOS. Based on the complete schematic of the complete IC a reduced schematic was derived with all necessary devices for the IC behavior during ESD pulses. All devices in the reduced schematic were substituted by their respective TBM or TBM-MOS. Additionally, the resistance values of the wiring between the devices were extracted from the IC layout data and added to the reduced schematic.

7.6.2 Results of system simulations

Selected results obtained by system simulations are presented here and compared to measured waveforms. The measurement setups are described in section 7.4. The single components of

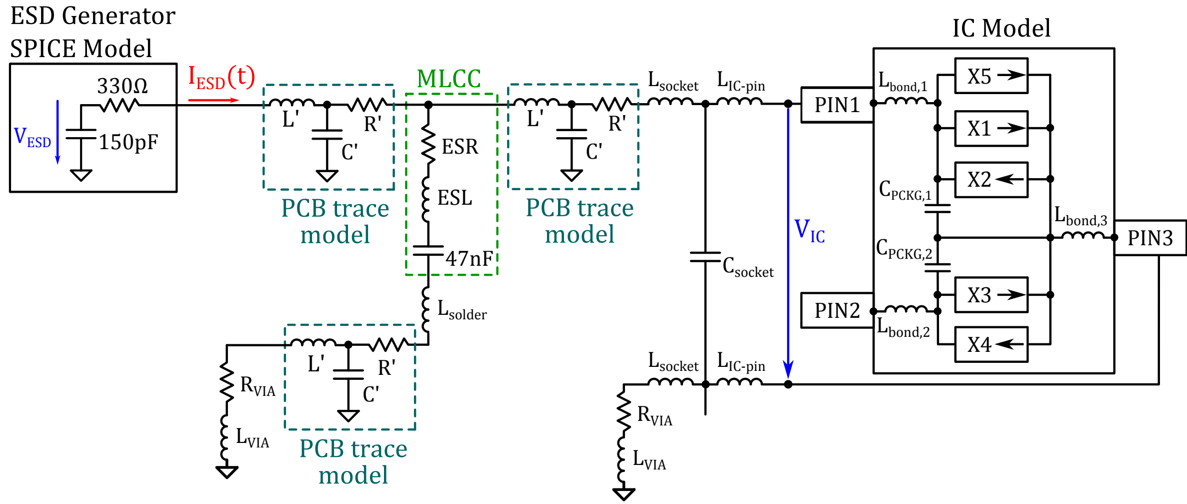


Figure 7.13: Schematic simulation setup for the configuration PCB level ESD with DUT1. An ASIC combined with an external MLCC of $47nH$ forms the system under test.

the simulation setup are described in section 7.6.1. The complete simulation setups are shown schematically in the following subsections.

Example 1: Sensor ASIC

As described in section 7.4.1 a voltage measurement directly at the IC pins was done during ESD injection into the PCB. The same ESD stress was given on the PCB in simulation. The results are discussed in detail in a conference paper presented at the ESD Forum 2017 [36]. The simulated ESD robustness levels in simulation match well with the measured values, see figure 7.6.2. The system ESD robustness of DUT1 when it is protected with varying external capacitance values was tested on two different PCBs layout variants (PCB1 in blue and PCB2 in red). At capacitance values above 10 nF the robustness values differ significantly between both PCB variants. With the detailed system simulations these differences can be reproduced. Based on these results the PCB2 was modified to improve the ESD robustness with 30 nF and 47 nF which is confirmed by simulation and measurement (green curves). To show the necessity and advances of the TBM additionally the system simulations were done with the 100 ns quasi-static IC model. The results are plotted with a black, dashed-dotted line. This IC model delivers the same results for all different PCB variants and is not able to reproduce the different ESD robustness levels for the layout variants.

The comparison of the transient waveforms shows that generally the voltage spike during the first nano-seconds of the ESD pulse is higher at PCB2 compared to PCB1 at the same ESD test level. It is understood that this ASIC is sensitive to this short voltage spike and hence the differences in ESD robustness of the two PCB layout variants can be explained.

The voltage spike is significantly higher at PCB2 than on PCB1. Therefore, the critical

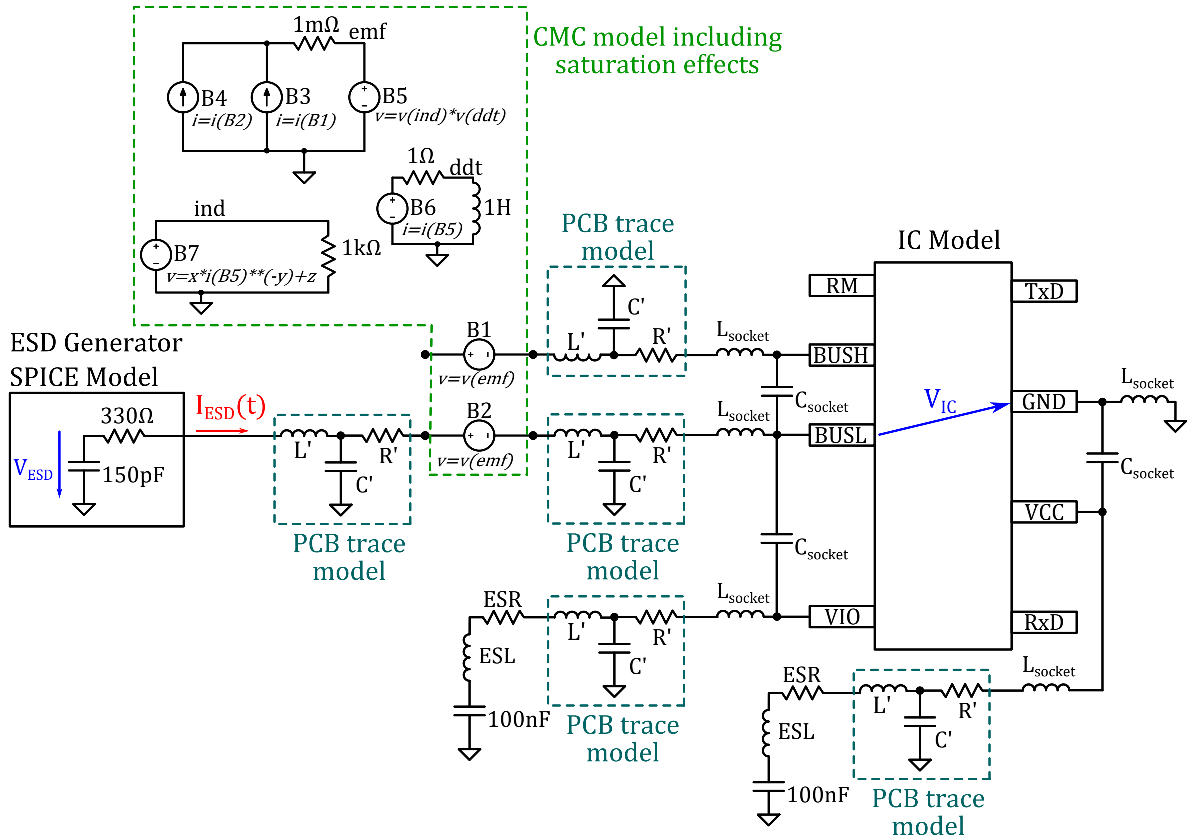


Figure 7.14: Schematic simulation setup for the configuration PCB level ESD with DUT2. A communication IC combined with a CMC forms the system.

voltage level to destroy the ASIC is reached at lower ESD test levels (see figure 7.6.2). The difference is seen in both measurement and simulation while the exact waveforms and peak values are not in good conformance. The differences can come from the over-simplified IC model. It is expected that the negligence of the electromagnetic coupling from the ESD generator to the DUT is the reason for lower peak values in simulation than in measurements. Furthermore, the waveform of the ESD current differs significantly in simulation from measurements. This points into the direction that the SPICE model for the ESD generator is not perfect enough and hence brings the differences in the voltage waveforms at the IC pins. As the modeling of the ESD generator is not in focus of this work and the differences in ESD robustness of the simulations are within a range of ± 20 % of the measured values, these differences can be accepted. Although the simulated waveforms are not in perfect match with the measurements, the reason for the "early fails" can be understood with system simulations. Moreover, the layout of PCB2 can be optimized with the help of simulations (PCB2A) and the ESD robustness with 30 nF and 47 nF capacitors is increasing significantly (green, dashed line). The enhanced ESD robustness is validated with measurements (green, solid line).

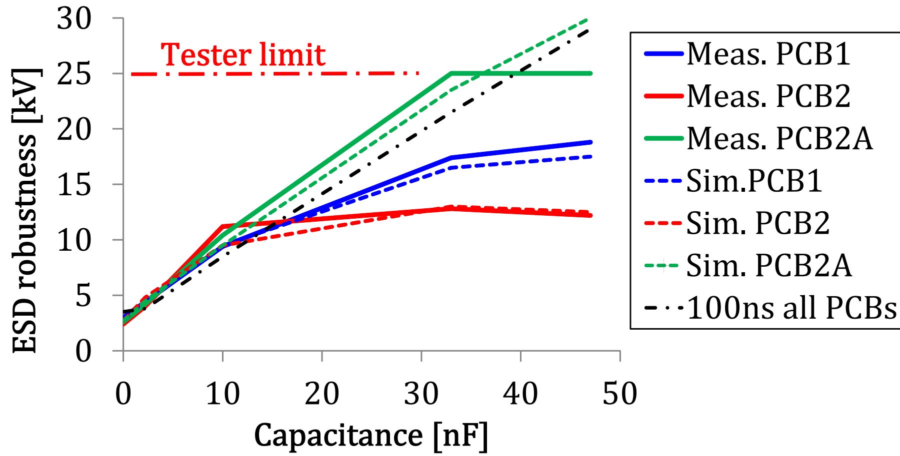


Figure 7.15: System ESD robustness of DUT1 protected with external capacitors in simulation (dotted lines) and measurements (solid lines).

Example 2: communication IC

The results of a communication IC combined with a common mode choke during system ESD stress are presented in figures 7.17 through 7.19. In the simulation setup are two of the developed models used. First, the advanced inductor model including saturation described in section 4.3.3 is used for the CMC. For the IC the model derived from the design data is used, see section 6.3. They are combined with the RLC-parasitic values of the PCB traces and an ESD generator model published by F. zur Nieden [67]. Figure 7.17 presents the current waveform delivered by the ESD generator. The measured waveform is plotted in green, the simulation with an ideal inductor model is plotted in dashed blue and the simulated waveform with the proposed inductor model including saturation is plotted in dashed-dotted red. The ideal inductor model is not able to reproduce the current waveform which is delivered from the ESD generator into the system. By contrast, the waveform of the proposed model matches well with the measured curve.

Figure 7.18 presented the voltage waveforms at the entrance of the PCB just before the common mode inductor. The proposed CMC model is able to reproduce the saturation behavior after $\approx 20\ ns$ which results in a dramatic drop in voltage. This means the CMC goes heavily into saturation and the ESD pulse is transferred nearly unchanged to the IC.

The simulated transient voltage waveforms directly at the IC pins have a good matching with the measured waveforms, see figure 7.19 for details. Additionally the failure level of the system during ESD stress is evaluated. The comparison of system ESD robustness levels of measurement and simulation are summarized in table 7.1.

The combination of precise ESD behavioral models for an IC and a CMC is able to exactly forecast the system ESD robustness. In this example the CMC effectively increases the system ESD robustness which is also visible in simulation.

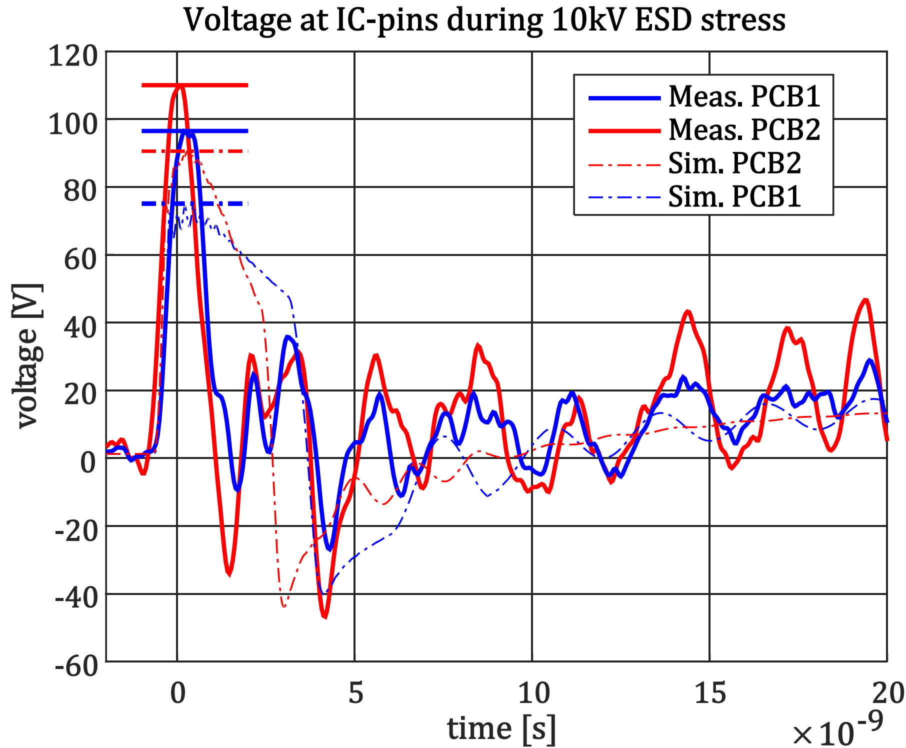


Figure 7.16: Voltage waveforms at ASIC pins (DUT1) during 10 kV ESD stress on PCB1 (blue) and PCB2 (red) obtained by measurements (solid lines) and simulations (dashed-dotted lines).

Table 7.1: System ESD robustness of the communication IC with the CMC

ESD robustness	measured	simulated
IC only	9 kV	10 kV
IC with CMC	> 17 kV	16 kV

Summary

In this section the used measurement setups are described in detail. Furthermore, the simulation setups for selected configurations are explained step by step. The simulation results are compared to measured values and waveforms. All in all, a good matching of measurement and simulation is achieved. The modeling methodologies TBM and TBM-MOS are suitable to generate simplified models of complete ICs for precise system ESD simulations. The prediction accuracy of the proposed modeling methodology in terms of system ESD robustness is within ± 20 %. This allows system designers to find unwanted low robustness levels during design phase and resolve these issues with low efforts already before the first hardware tests are done.

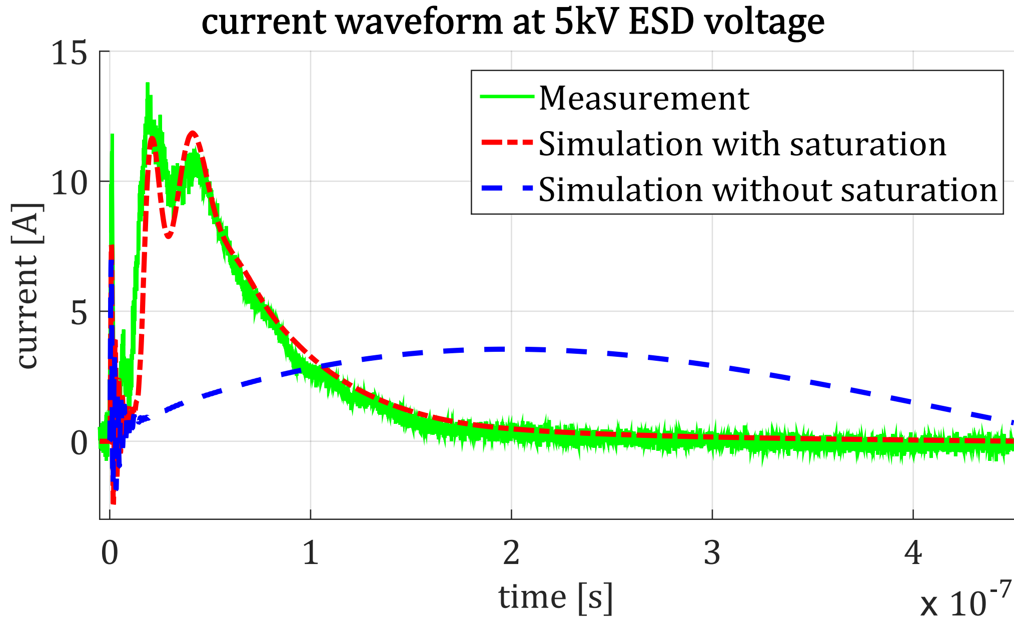


Figure 7.17: Current waveform measured at ESD generator tip with the FC-65 at 5 kV ESD voltage. Comparison of measurement (greed, solid line), simulation with proposed CMC model (red, dashed-dotted line) and basic CMC model (blue, dashed line).

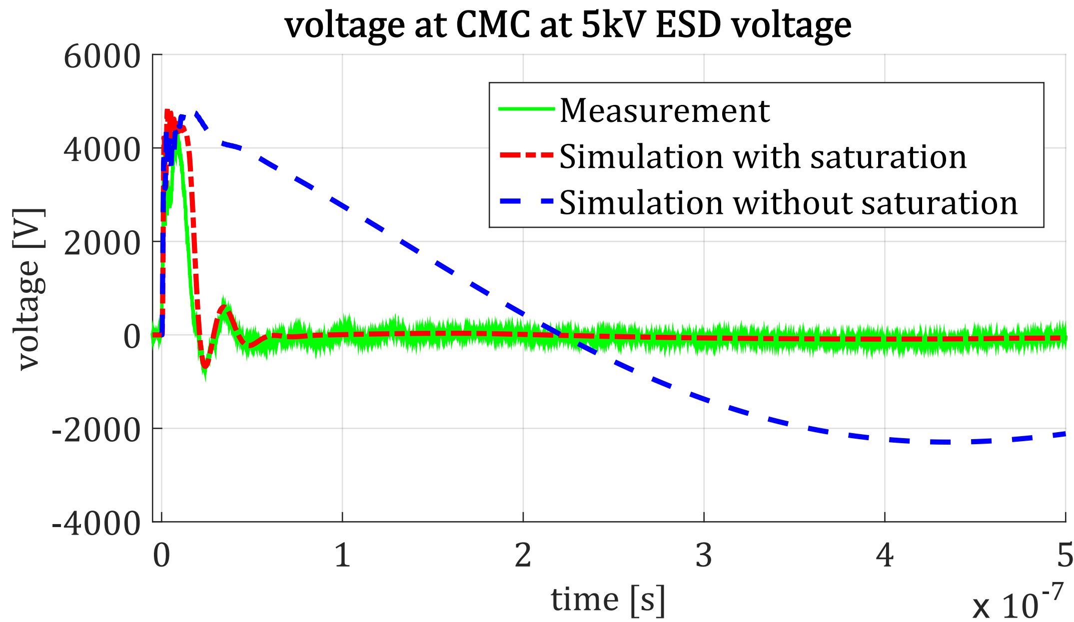


Figure 7.18: Voltage waveform at the CMC port close to the ESD generator at 5 kV ESD voltage (measurement point V1). Comparison of measurement (greed, solid line), simulation with proposed CMC model (red, dashed-dotted line) and basic CMC model (blue, dashed line).

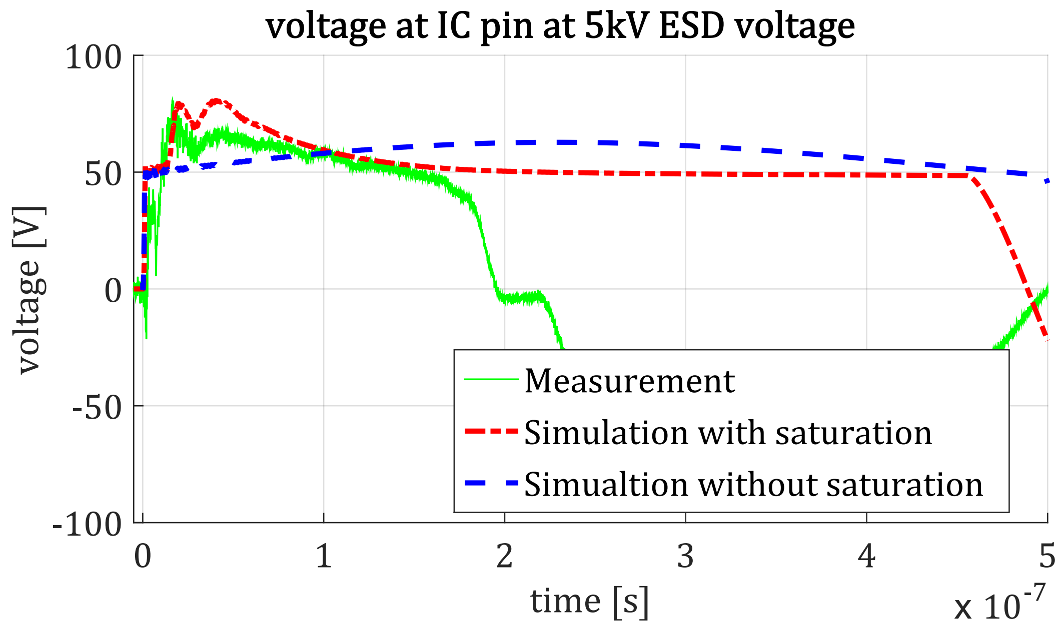


Figure 7.19: Voltage waveform at the CMC port connected to the IC at 5 kV ESD voltage (measurement point V2). Comparison of measurement (greed, solid line), simulation with proposed CMC model (red, dashed-dotted line) and basic CMC model (blue, dashed line).

8 Summary and Outlook

Designing electronic (sub-)systems, which are robust against ESD events, is still not an easy task. Furthermore, there is no standard approach available. The SEED methodology [1], [2] provided a good starting point to address the ESD robustness of systems. However, to enable SEED by simulation adequate ESD models for all components are necessary. Especially adequate models for complete ICs are often not available defeating the original idea of the SEED approach.

Overall target of this work

First of all, the development of a generic model architecture to describe the electrical behavior of commonly used protection devices during ESD events was targeted. This generic model needed to catch the quasi-static clamping behavior as well as dynamic effects, e.g. self-heating or forward recovery effects. The target simulator language was chosen to be SPICE. The implementation of time-dependent failure levels was another important requirement. A particular objective of this work was to develop a methodology for model generation which does not require measurements with the complete IC. Goal of this work was to provide a methodology which enables an efficient way to extract ESD models for complete ICs from the design data.

Achievements in modeling

To achieve the targets summarized above, the generic model architecture *TBM* was developed. This architecture is based on switches to reproduce the clamping behavior of protection devices. The behavioral TBM is independent of the used device, which makes it usable for various types of protection devices and self-protecting devices. Typical breakdown based devices (e.g. zener diodes) can be represented as well as devices with snap-back behavior like bipolar transistors. The dynamic on-resistance is modeled in a way that transient effects, like resistance increase due to self-heating or conductivity modulation, are also covered. The generic model is controlled via a compact set of parameters to reproduce all the different clamping behaviors and transient effects.

Within the model the dissipated power and energy are calculated for each point in time. Parametric equations describe the power-to-failure and energy-to-failure dependent on the stress duration. At each simulation step the actual dissipated power is compared with the power-to-failure and the energy is compared with the energy-to-failure. Thereby the thermal

destruction level can by detected. The voltage drop over the device terminals is compared to the voltage limit to detect electrically induced failures. When an excessive voltage drop or a thermal overstress is detected by the model, a flag *FAIL* is set. Additionally, the dynamic resistance is set to a low value to mimic the electrical behavior after a thermal failure.

As MOSFET devices behave quite specially in case of ESD events, a dedicated model called *TBM-MOS* was developed. The TBM-MOS is a behavioral model constructed of switches, based on the TBM. The transient turn-on of the MOSFET due to drain to gate coupling can be replicated. The decay of gate potential and hence an increase of the dynamic resistance is included. Furthermore, the avalanche breakdown regime, typically for high voltage DMOS devices, is modeled. The mechanisms for failure detection are borrowed from the TBM.

The initial *TBM* and *TBM-MOS* parameter setting can be found by measurements with the single devices (e.g. on a test-chip). To reduce the effort for complete IC models significantly, a methodology was developed in this work to derive complete IC ESD models from design data. Through this step, the numerous measurements with a complete IC (several pin-combinations with various pulse durations) are no longer needed. The IC ESD model is constructed with single device TBMs, based on the schematic of the IC. The generic architecture of the TBM allows to combine several devices, in series or parallel connection, into one single model. A very compact IC model with short simulation runs and strong IP protection is the result.

Results from modeling application

The proposed modeling methodology was tested with different examples. Two different types of ICs were used for this study. One example was a sensor ASIC to measure magnetic fields. Such sensors are widely used within cars for various applications. Combined with a few external components they need to be robust against a broad variety of pulses. The second example was a communication IC which typically needs to sustain high system level ESD events (e.g. 8 kV) without any external component. The generated models are able to reproduce the transient behavior, the quasi-static i-v-curves and the failure points derived from TLP tests for various pulse durations with good accuracy. The developed IC ESD models, combined with accurate models for the external components, are able to predict the system ESD robustness with an accuracy of $\pm$ 20 %.

Changes in the systems (e.g. PCB routing or different external components) and the resulting influence on the system ESD robustness were successfully analyzed. It was shown that the PCB routing of external capacitors can influence the ESD robustness significantly. The second example showed that external components can double the system ESD robustness, although the common mode inductor showed a very low damping performance. A widely used CMC type was used to develop a methodology for characterizing and modeling the saturation behavior of the CMC during ESD events. The generated CMC model enabled precise system ESD simulations and made it possible to successfully study the system response and destruction level in case of

ESD events.

The presented methodology for model generation proofed to be a good way to efficiently generate ESD models for complete ICs. These models combined with accurate models of the external components enable the SEED approach by simulation. This enables to detect weak points in the system ESD robustness and fix them already in the design phase. While optimizing the functional performance of the system by simulation, the required ESD robustness is maintained.

Possible extensions for the future

The presented methodology for IC ESD model generation is already a big step forward towards a systematic system design for ESD robustness.

Nevertheless, there is still some room for improvements in the future.

First of all, the existing model architectures TBM and TBM-MOS show some convergence issues under several conditions. This could be improved in future works. A possible area for improvement could be the switch devices as they have a huge difference in resistance values between on- and off-state. Several orders of magnitude difference in one domain (e.g. resistance values or voltage drops) are always a big challenge for the simulation solver.

Furthermore, spending more work in the automation of the single steps and hence the complete model generation process from design data significantly reduces the effort for model generation.

The failure detection with the power-to-failure and energy-to-failure formulas is well suited for rectangular pulses like TLP. For exponential or arbitrary pulses (i.e. real world ESD pulses) the accuracy of this method could be better. Other approaches of thermal failure detection can be more accurate. One interesting approach could be a thermal RC-network and a critical temperature for the thermal failure onset, like presented by Russ et.al. at the 2018 EOS/ESD Symposium [73].

Conclusion

This work presented a generic model architecture for modeling ESD protection devices, which is basis for a novel methodology to generate IC ESD models from design data. Up to now, these models were typically generated from measurements with the complete IC. This can be a very cumbersome process as each pin-combination needs to be measured with several pulse durations. The presented methodology does not need any measurement with the complete IC. By contrast, the proposed methodology is capable of generating the IC ESD model by processing the design data of the IC. Based on the schematic of the complete IC the necessary devices are identified and substituted by their respective TBM. The relevant wiring resistance and inductance values are extracted from the IC layout. The combination of several devices

into one TBM results in very compact behavioral ESD model for complete ICs. This reduces the effort for model generation significantly and offers the possibility of automation.

The methodology is proven with two examples of typical automotive ASICs. The dynamic behavior, failure levels of the single ICs and failure levels of small test systems are predicted with an accuracy of ± 20 %. This accuracy is highly appreciated by system designers.

Own publications

During the research for this PhD thesis selected results were published beforehand at selected conferences and the *IEEE Transactions on Electromagnetic Compatibilty.* The following table summarizes all relevant publications as first author in chronological order starting form the newest.

The paper presented at the 15th ESD Forum in 2017 received the outstanding paper award.

Year	**Conference/ Journal**	**Title**	**Ref.**
2019	EOS/ESD Symposium	*Application Example of a Novel Methodology to Generate IC Models for System ESD and Electrical Stress Simulation out of the Design Data*	[64]
2019	EOS/ESD Symposium	*Characterizing and Modelling Common Mode Inductors at high Current Levels for System ESD Simulations*	[52]
2019	IEEE Trans. on Electromag. Comp.	*Bringing the SEED Approach to the Next Level: Generating IC Models for System ESD and Electrical Stress Simulation out of Design Data*	[9]
2018	EOS/ESD Symposium	*Modeling the Transient Behavior of MOS-Transistors during ESD and Disturbance Pulses in a System with a Generic Black Box Approach*	[59]
2017	EOS/ESD Symposium	*How to build a Generic Model of complete ICs for system ESD and electrical stress simulation?*	[8]
2017	ESD Forum	*Simulation of System Level ESD robustness using advanced behavioral IC models under consideration of PCB parasitics*	[36]
2016	Smart Systems Integration	*Obstacles in Predicting ESD Robustness according to ISO10605 of Electronic Systems with Automotive Examples*	[33]

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